Multi-Level Voltage and Current Reinjection AC-DC Conversion

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ABSTRACT

This thesis describes a new concept of multi-level reinjection ac-dc conversion, its main purpose being a further reduction of the harmonic content, a solution of dynamic voltage balancing for direct series connected switching devices and an improvement of high power converter efficiency and reliability. It is a combination of the multi-level, soft switching and reinjection concepts. A variety of configurations are proposed, based on the new concept, to achieve efficient voltage and current conversion. For each configuration the firing sequences, waveform analysis, steady and dynamic performances and close-loop control strategies are presented, and particular applications suggested.

The ideal reinjection waveforms are first derived for perfect harmonic cancellation and then fully symmetrical approximations are made for more practical implementations. This is followed by a description and comparison of the generation circuits required for the implementation of the multi-level symmetrical reinjection waveforms.

A three-level voltage reinjection scheme, implemented by adding a reinjection bridge and a reinjection transformer to the standard twelve-pulse converter, is discussed in great detail, both for the series and parallel connections. This is followed by an investigation into the possible application of these converters to Back to Back VSC HVdc interconnection; the analysis is validated by EMTDC simulations.

A multi-level voltage reinjection VSC is also proposed, which uses a controllable dc voltage divider to distribute the dc source voltage to the two main bridges and produces high quality output waveforms. The voltage and current waveforms, the firing sequences and the capacitor voltage balancing are analyzed and verified by EMTDC simulations. In particular, the proposed VSC is shown to be an ideal solution for the STATCOM application.

The multi-level reinjection CSC alternative is also described and shown to exhibit an excellent performance in the STATCOM application.

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GLOSSARY

Abbreviations

ac-dc	alternative current - direct current
BGASMP-VSC	Binary Grouped Asymmetrical Switch Multi-Path VSC
BTBVSCL	Back-To-Back Voltage Source Converter Link
CSC	Current Source Converter
ESEDS	Error Square and Error derivation Square (minimization)
ESEDS-VSC	ESEDS (minimized reinjection) Voltage Source Converter
FACTS	Flexible AC Transmission System
GTO	Gate Turn Off Thyristor
HVDC	High Voltage Direct Current (transmission)
IGBT	Insulated Gate Bipolar Transistor
IGCT	Integrated Gate Commutated Thyristor
MLCR	Multi-Level Current Reinjection
MLCR-CSC	Multi-Level Current Reinjection Current Source Converter
MLVR	Multi-Level Voltage Reinjection
MLVR-VSC	Multi-Level Voltage Reinjection Voltage Source Converter
MLDC-VSC	Multi-Level Diode Clamped VSC
MLCC-VSC	Multi-Level Capacitor Clamped VSC
MLCHB-VSC	Multi-Level Cascaded H-Bridge VSC
MLASC-VSC	Multi-Level Asymmetrical Switch Clamping VSC
NPC-VSC	Neutral Point Clamped VSC
PWM	Pulse Width Modulation
PI	Proportion and Integration (controller)
PID	Proportion, Integration and Derivation (controller)
pu	per unit
STATCOM	Static Compensator
THD	Total Harmonic Distortion
VSC	Voltage Source Converter
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching

Symbols

A_{Yk}	$6k^{th}$ order harmonic amplitude of the ideal reinjection waveform to Y connection bridge (12-pulse system)
$A_{\Delta k}$	$6k^{th}$ order harmonic amplitude of the ideal reinjection waveform to Δ connection bridge
A_{ESEDSk}	$6k^{th}$ order harmonic amplitude of the ESEDS reinjection waveform to the Y connection bridge
A_{LINk}	$6k^{th}$ order harmonic amplitude of the linear reinjection waveform to the Y connection bridge
B_k	$3k^{th}$ order harmonic amplitude of the ideal reinjection waveform to a half-bridge (6-pulse system)
B_{Lk}	$3k^{th}$ order harmonic amplitude of the linear reinjection waveform to a half-bridge
B_{Sk}	$3k^{th}$ order harmonic amplitude of the ESEDS reinjection waveform to a half-bridge
H_{Li}	i^{th} level height of an m-level linear reinjection waveform
H_{Si}	i^{th} level height of an m-level ESEDS reinjection waveform
H_{6Li}	i^{th} level height of an m-level linear reinjection waveform
H_{6Si}	i^{th} level height of an m-level ESEDS reinjection waveform
I_{A1Lm}	Fundamental amplitude of converter system output line current (linear m-level reinjection for 6-pulse system)
I_{A1Sm}	Fundamental amplitude of converter system output line current (ESEDS m-level reinjection for 6-pulse system)
I_{ALmRMS}	RMS current of converter system output line current (linear m-level reinjection for 6-pulse system)
I_{ASmRMS}	RMS current of converter system output line current (ESEDS m-level reinjection for 6-pulse system)
$I_{B\Delta}$	DC side output current of the Δ connection bridge
I_{BNY}	DC side output current of the common cathode half-bridge
I_{BPY}	DC side output current of the common anode half-bridge
I_{BY}	DC side output current of the Y connection bridge
$\mathbf{I_{cap}}$	Current Vector through the $m-1$ capacitors in capacitor bank
i_{cd}	Current out of the capacitor bank
i_{ci}	Current through the i^{th} capacitor in capacitor bank
I_{ci}	DC component of the current through the i^{th} capacitor
i_{cu}	Current into the capacitor bank
I_{DSYRMS}	RMS current rating of the reinjection free-wheeling diode
I_{GSYRMS}	RMS current rating of the reinjection self-commutated switch
I_{Na}	AC output phase current of the common cathode half-bridge
I_{Pa}	AC output phase current of the common anode half-bridge

I_{SR}	Rated current of the reinjection VSC system
I_{Im}	Imaginary current component
I_{Re}	Real current component
I_{jRMS}	RMS current of the reinjection current ac component
$\mathbf{I_o}$	Three phase output current vector of the reinjection VSC
i_{Si}	Current through the i^{th} reinjection switching path
I_{Sj}	DC component of the current through the j^{th} reinjection path
I_{Ya}	AC output phase current of the Y connection bridge
$I_{\Delta a}$	AC output phase current of the Δ connection bridge
i_{Ydc}	DC side current of Y connection bridge
$i_{\Delta dc}$	DC side current of Δ connection bridge
k_j	Turns ratio of the reinjection transformer
k_n	Turns ratio of the interface transformer
k_s	Nominal leakage reactance of the interface transformer
M_{dc}	DC average component of the Y and Δ connection bridges
P	Active power
P_{ref}	Active power reference order
Q	Reactive power
Q_{ref}	Reactive power reference order
Q_{sR}	Rated reactive power of the reinjection VSC
R_L	Load resistance
S_s	Rated apparent power of the reinjection VSC
THD_{IASm}	Total harmonic distortion of converter system ac output current (ESEDS m-level reinjection for 6-pulse system)
THD_{IALm}	Total harmonic distortion of converter system ac output current (linear m-level reinjection for 6-pulse system)
THD_{I_A}	Total harmonic distortion of converter system ac output current
THD_{V_A}	Total harmonic distortion of converter system ac output voltage
THD_{lin}	Total harmonic distortion of linear reinjection converter system ac output voltage or current
THD_{sym}	Total harmonic distortion of m-level ESEDS reinjection converter system ac output voltage or current
THD_{outS}	Total harmonic distortion of ESEDS reinjection converter system ac output voltage or current (6-pulse system)
THD_{outL}	Total harmonic distortion of linear reinjection converter system ac output voltage or current (6-pulse system)
U_{dc}	DC source or capacitor bank voltage
U_{dcR}	Rated dc voltage across the dc capacitor bank
U_{jRMS}	RMS voltage of the reinjection voltage ac component
u_j	Reinjection voltage ac component

V_A	Converter system ac output phase voltage of the 12-pulse system
V_{A1}	Fundamental amplitude of converter system output phase voltage
V_{ARMS}	RMS voltage of converter system output phase voltage
V_{dc}	DC voltage across the converter bridges
V_L	Level voltage, per level voltage of the controllable voltage divider
V_{ppR}	DC voltage ripple peak to peak value at the rated current condition
V_{BPY}	DC side output voltage of the common anode half-bridge
V_{BNY}	DC side output voltage of the common cathode half-bridge
V_{Pa}	AC output phase voltage of the common anode half-bridge
V_{Na}	AC output phase voltage of the common cathode half-bridge
$\mathbf{V_o}$	Three phase output voltage vector of the reinjection VSC
$\mathbf{V_s}$	Three phase voltage vector of ac source
V_s	AC source voltage
V_{SR}	Rated voltage of the reinjection VSC system
$V_{\Delta a}$	Output phase voltage of the Δ connection bridge
V_{Ya}	Output phase voltage of the Y connection bridge
V_{Yan}	n^{th} order harmonic component of the Y connection bridge phase voltage
$V_{\Delta an}$	n^{th} order harmonic component of the Δ connection bridge phase voltage
V_{YY}	DC output voltage of the Y connection bridge
$V_{Y\Delta}$	DC output voltage of the Δ connection bridge
$\mathbf{X}_P(x)$	Ideal reinjection waveform for the common anode half-bridge
$\mathbf{X}_N(x)$	Ideal reinjection waveform for the common cathode half-bridge
$\mathbf{X}_{Ns}(x)$	ESEDS reinjection waveform for the common cathode half-bridge
$\mathbf{X}_{Ps}(x)$	ESEDS reinjection waveform for the common anode half-bridge
$\mathbf{X}_Y(x)$	Ideal reinjection waveform for the Y connection bridge
$\mathbf{X}_\Delta(x)$	Ideal reinjection waveform for the Δ connection bridge
$\mathbf{X}_{Ys}(x)$	ESEDS approximation of the ideal reinjection waveform to Y bridge
$\mathbf{X}_{\Delta s}(x)$	ESEDS approximation of the ideal reinjection waveform to Δ bridge
X_s	Leakage reactance of the reinjection VSC interface transformer
δ_i	Adjustment of the on-state interval for i_{th} reinjection path
θ	Power angle of the reinjection VSC system
ϕ	Phase displacement between the ac source and VSC output voltages

Chapter 1

INTRODUCTION

For a number of advantages such as fast dynamic response, better power factor, control flexibility of active and reactive power, capability of connecting to strong or weak (even passive) networks, the high power self-commutated ac-dc converters are required as the high power controllers by industrial applications and power transmission systems. Because of the high powers involved, the need to keep power losses down forces these converters to be directly connected to the high voltage level grids. The ratings of these converters have to match the high capacity demand for the particular applications, and their performances have to be of high standard to ensure power quality and system operation efficiency and safety.

The ratings and switching characteristics of high power self-commutated switching devices have improved greatly in the last two decades, typical present ratings on the market being 3.3kV/1.2kA (Eupec), 4.5kv/2kA (Fuji), 5.2kV/2kA (ABB) for the insulated gate bipolar transistors (IGBT) and 5.5kV/2.3kA (ABB), 6kV/6kA (Mitsubishi) for the integrated gate commutated thyristors (IGCT) [1]-[4]. Because the press pack IGBT, GTO and IGCT behave as short-circuit after being destroyed, these power switches are suited to the provision of redundant series connection in the stack to form reliable high voltage rating valves; examples are the IGCT modules and the press pack IGBT (4.5kV/2kA (Fuji), 5.2kV/2kA (ABB)) modules. The availability of these powerful devices has permitted the development of self-commutated high power converters (80MVA, 100MVA,160MVA) for power transmission applications [5]-[11].

The continuing demand for higher power ratings, performance improvement and cost reduction, besides the advances in power semiconductor switching devices, has resulted in significant innovations in converter design, such as multi-level converter topologies, soft switching and converter control strategies during the 80's and 90's. The research focus has been on increasing converter power ratings taking into account the available power switch ratings, enhancing performance, suppressing harmonic distortion, improving dynamic responses, and reducing power losses.

1.1 MULTI-LEVEL CONVERSION FOR HIGH POWER APPLICATIONS

The voltage and current ratings of the gate commutated power semiconductor devices, mainly insulated gate bipolar transistors (IGBT) and integrated gate commutated thyristors (IGCT), are advancing towards the levels of the high power line commutated thyristors [1]. The power rating of a six-pulse 3-phase bridge converter built up with 6 power switches of 6kV/6kA rating devices is about 10MVA. Either bridge combinations or device combinations in series and parallel have to be adopted for higher power rating applications.

The maximum power ratings of lower voltage ac-dc self-commutated converters are limited by the efficiency requirements and practical current ratings of power components such as cables and transformers. For power rating over 5MVA, medium and high voltage converters are preferred, because they achieve significant energy savings and better thermal performance of power components.

As explained earlier present IGCT and press pack IGBT power switch devices are suitable to form reliable higher voltage valve ratings. The series-connected power switch valves can be fired either synchronously or asynchronously. The synchronous control is used in two level schemes, while the asynchronous control is used in multi-level schemes.

The synchronous control of the direct series connection of power switches (switching from off-state to on-state under rated voltage or from on-state to off-state under rated current and voltage) presents the following problems.

Static balancing, which can be solved by connecting large resistors in parallel with each switch, though this causes some extra power losses.

Dynamic balancing, a more serious and difficult problem to solve. Ideally all switches in the series connection should commutate with the same dynamic behaviour, otherwise the switch that turns off first or turns on last would have to sustain all the voltage. However, it is not realistic and economical for practical power switches to switch in exactly the same manner. By selecting devices with close switching delays as well as connecting snubbers, the situation can be improved, but which increases spare parts for maintenance greatly, slows down the switching process and reduces the efficiency.

High dV/dt**,** because in a two level synchronous control high voltage converter every switching action results in the full voltage changing in a few micro-seconds, i.e. a dV/dt higher than 1-10GV/s is produced. That will cause serious interference and possibly components insulation damage.

Therefore the synchronous control of the direct series connection of high power switches is not suitable for high power and high voltage conversion applications. Instead the

emergence of the multi-level topologies and the use of asynchronous firing control of the direct series connected switching devices provides an effective solution.

In the multi-level Voltage Source Converter (VSC) topologies, the direct series connected power switches are controlled asynchronously to improve the voltage balance under dynamic conditions, while the steady-state voltage equally sharing is achieved with the assistance of switching device voltage clamping. By the use of an appropriate control sequence for the power switches in the series connection, the output waveforms are improved thus reducing the harmonic distortion; moreover, because the change of state is done level by level, the dV/dt is greatly reduced.

Different multi-level Voltage Source Converter configurations have been proposed [12]-[19], and appropriate control strategies developed. These are of three types [20]-[22]: diode clamped VSC (or neutral point clamped (NPC) VSC for 3-level VSC) [12]-[14]; capacitor clamped VSC (flying or floating capacitor clamped VSC) [15, 23, 24]; and cascaded multi-cell VSC (cascaded H-bridge VSC) [18, 25, 26]. The multi-level concept was mainly developed for VSC, and very few of multi-level CSC configurations have been reported so far [27]-[29].

The complexity is increased sharply as the level number increases, (i.e. a large number of clamping diodes or of high capacity floating clamping capacitors is required when the level number is large in high voltage applications). Capacitor voltage imbalance occurs in the diode clamped multi-level configuration, and thus the level number is limited to a relative low value, which results in the use of PWM techniques to suppress the harmonics further.

Multi-level converter topologies have been around for more than twenty five years. They first appeared in the form of cascade full-bridge cells connected with separated power sources. In the early 1980's the diode clamped multi-level converter was introduced [12], though initially restricted to a three level converter and known as the neutral point clamped (NPC) topology. Its extension to general high level was published in 1992 [13]. The capacitor clamped multi-level converter topology was introduced in the early 90's [15, 23].

All these multi-level converters possess the following advantages:

1. Generation of better step output waveforms with very low harmonic distortion and lower dV/dt;

2. Steady and dynamic equal voltage sharing of the series connected switching devices achieved by the asynchronous firing control and voltage clamping;

3. Use of lower switching frequencies and thus reduced switching losses.

Each topology has some advantages and disadvantages as listed below:

(i) Diode clamped VSC's

Advantages

- Control flexibility of inductive and capacitive power flow;
- When the number of levels is high enough, harmonic distortion can meet the critical standards under fundamental switching, i.e. without the need for PWM, thus reducing the switching losses;
- Under appropriate control both sides of a back-to-back inter-connector can share the dc capacitor bank as a dc voltage divider.

Disadvantages

- The clamping diodes required are nearly proportional to the level number square;
- When the level number is higher than three, the converter can not control the real power flow between ac and dc sides on its own, because only when the power angle is exactly equal to $\pm 90^o$ ensures that every capacitor is charged and discharged equally to maintain capacitor voltage balance;
- The unequal power rating of the power switches introduces design and maintenance difficulties.
- The clamping nature of the topology makes it difficult to add redundant switches to increase reliability.

(ii) Capacitor clamped VSC's

Advantages

- Control flexibility of inductive and capacitive power flow;
- When the number of levels is high enough, for inductive and capacitive reactive power flow control application, the harmonic distortion can be kept within the standards under fundamental switching frequency;
- The availability of switching combination redundancy for generating the most of output levels provides flexible control of the clamping capacitor current and thus keeps the clamping capacitor voltage at the required level; thus this type of converter is suitable for active and reactive power control applications;

Disadvantages

- The clamping capacitors required are nearly proportional to the level number square;
- Complicated control strategies are required to ensure that the capacitor voltages are maintained at the required level when the converter is used to control the active power flow.

- As the load current passes through the clamping capacitors the current rating of the clamping capacitor is higher, and that limits the converter rating for high power applications.

(iii) Cascaded H-bridge VSC's

Advantages

- The provision of three possible output levels from an H-bridge cell permits using fewer cells to form high level number conversion and without the need for clamping diodes or capacitors;
- When the number of cells is high enough, the harmonic distortion meets the critical standards;
- Because each basic cell is identical, it is easy to form a high power VSC with the modularized cells; therefore, the manufacturing and maintenance costs can be significantly reduced.

Disadvantages

- For real power conversion the dc sources need to be isolated, and thus its application in this area is somewhat limited.
- For an application as a back-to-back connection the isolated dc sources can not be shared by the two converters unless they are switched synchronously.

The above advantages and disadvantages show that present multi-level configurations are attractive for high power and high voltage applications; however for very high power conversions, further research is needed.

1.2 SOFT SWITCHING FOR HIGH POWER CONVERTERS

The soft switching concept has attracted a great deal of interest in the last two decades, because it has the great potential to enhance the performance and reduce the switching losses of the power electronic switches. Soft switching and PWM techniques have been successfully applied to the dc-ac-dc conversion for low power supplies (with power rating range from a few watts to 100 kilo-watts) to increase the switching frequency, reduce the switching power losses and achieve high density power conversion in volume and weight [30]-[37].

The application of soft switching to ac-dc converters, recognized in the late 1980's [38], is much more complex due to the bidirectional power flow, modulation with multi-frequency involved, wide range of load conditions and the inherent sinusoidal current waveform. That means that the ZVS (zero voltage switching) and/or ZCS (zero current switching) soft switching conditions must be provided to all the switches in the

converter for load current conditions varying from zero to peak value and for different output frequencies.

In the last twenty years, over a hundred new resonant and quasi-resonant soft switching topologies [39]-[46] have been proposed for ac-dc power conversion such as motor drive, induction heating, power line conditioner and so on. The power ratings of the soft switching converters developed for induction motor drive applications are from a few watts to 1MVA [47, 48].

In these proposed topologies, the soft switching networks consisting of inductors, capacitors, diodes and self-commutated switches are added to the conventional hard switching converters. Most of the proposed soft switching circuits are based on LC resonance to provide the Zero Voltage Switching (ZVS) and/or Zero Current Switching (ZCS) condition. In the resonant and quasi-resonant soft switching converter, the current in a switch and/or the voltage across a switch are forced to be close to zero by creating a resonance at the beginning of the switching process, and during the switching process; this reduces the di/dt in the switch device which is turning on, and the dv/dt across the device which is turning off.

The various soft switching techniques used for ac-dc converters can be classified based on the location of the soft switching components, as the component ratings and costs depend on whether they are part of the main power flow path or not.

1). **Load resonant converter:** An LC resonant tank is added to the ac side output power path in series, parallel, or a series/parallel combination to obtain the ZVS and/or ZCS condition.

2). **Resonant dc Link converter:** The resonant network is connected between the dc source and the converter bridge, and it is active for every switching action in the converter bridge to create the ZVS or ZCS condition.

3). **Transition resonant pole converter:** The resonant networks, added to the converter bridges, are active to create the condition of ZVS or ZCS only when the switching state of each main bridge switch is changing.

The first and second types are not appropriate for high power ac-dc converters, because the soft switching resonant components are connected in the main power transfer path. Instead the soft switching techniques for high power converters ought to present the following features:

- Ideally the components added to the high power converter to achieve soft switching should be activated only during the switching transition intervals and should ensure that the circulating energy involved is as low as possible and completely decoupled from the main power transfer to the load.

- For economy, the parasitic capacitance of the devices and the stray inductance of the circuitry should be part of the resonant scheme; however, the circulating energy involved should be sufficient to create the soft switching conditions (ZVS or ZCS) reliably, irrespective of the variations in the load level.

- The main switch voltage and current waveform changes, which are caused by the circulation of energy used for soft switching, ought to be insignificant, so that the main switch device ratings are not increased.

- The soft switching network should be activated by the converter firing control signals to ensure that the soft switching conditions occur at the appropriate time intervals.

Some recent publications have proposed soft switching circuits for multi-level conversion topologies [49]-[55]; these are all for voltage source converters and use the transition resonant soft switching principle. The 3-level 3-phase soft switching converter proposed in [56] is a typical NPC (neutral point clamped) converter which includes two Auxiliary Resonant DC link (ARDCL) snubbers to provide ZVS soft switching conditions.

Although these multi-level soft switching converters achieve switching power losses reduction and harmonic distortion suppression by using higher switching frequency, even for the relative low level number, they become very complicated and costly. Moreover the soft switching circuit proposed in [56] is not appropriate for high power application because two self commutated power switches are added to the main power flow path. For ratings over 10MVA, the switching frequency can not be very high, and to suppress the harmonic distortion either higher level numbers or costly filters have to be used, thus making the converter system very complicated. Therefore there is room for further development of the soft switching techniques for high power applications.

The soft switching of the multi-level reinjection converters proposed in this thesis is not based on the power device switching transitions taking place under resonant conditions. Instead, the use of forced clamping or blocking provides the zero voltage or zero current switching conditions. The forced clamping or blocking are provided by the reinjection components, which are used to supply variable dc voltage or current levels (the zero voltage level corresponding to forced clamping and the zero current level corresponding to forced blocking). These ZVS or ZCS conditions are synchronized with the firing control of the main switches; they are also of controllable duration, such that the zero voltage or zero current conditions are established before the switching action takes place, and terminated after the switching dynamic process finishes.

The proposed soft switching conditions are of two types, i.e. a zero voltage switching condition is provided to the voltage source converter topology, and a zero current switching condition is applied to the current source topology.

For the multi-level voltage reinjection VSC topology the reinjection components used to provide the ZVS conditions are not connected in the main power transferring paths and therefore their current ratings are low. The proposed scheme uses the on-state of the reinjection switching devices to clamp the main power switching devices that are changing their switching state. Under this type of ZVS, the dynamic voltage sharing of the direct series connected power switches under synchronous control is not a problem; the energy stored in the snubbers and parasitic capacitors of the power switches can be recovered without losses, and thus the snubbers will be very simple and inexpensive. Also the bridge type converter can be designed as a standardized unit with the appropriate voltage and current ratings without concern for dynamic voltage balancing of the direct series connected power switch devices and parasitic energy absorbtion. Another positive effect is that there is no risk of short-circuiting the dc power source in the commutation between the two main bridge arm valves in a phase leg (or a phase pole), i.e. there is no need for a dead interval between switching off one of the main valves in the same pole or phase-leg and switching on another. The reliability of the high power converter is thus increased.

Similarly for the proposed multi-level current reinjection CSC topology, the reinjection components used to provide the soft switching conditions are of low voltage ratings. The proposed scheme uses the reinjection power switches to provide the zero current conditions for the main power switches. Again this type of ZCS is totally different from the present resonant soft switching techniques. Under this type of ZCS, the energy stored in the inductors and stray inductance is gradually returned to the system, and thus the interface between the CSC and the ac power system can be very simple and implemented economically.

1.3 REINJECTION CONVERSION FOR HARMONIC ELIMINATION

1.3.1 Harmonic Injection and Ripple Reinjection

The concept of **harmonic injection** for harmonic reduction in power converters was first proposed by Bird [57] in 1969. In his paper the third harmonic was used to modify the rectifier current waveform in order to reduce the ac side current harmonic content. The harmonic reduction by **triple-harmonic injection** was further generalized by Ametani in 1972 [58]. He demonstrated the effects caused by individual harmonic (3, 5, 7, 9 order harmonics) injections; and concluded that the third harmonic is the most suitable general purpose injection current, and the ninth harmonic the most appropriate for the reduction of the higher order harmonics. He also extended the harmonic injection concept to the variety of the six-pulse current source type configurations. The harmonic injection concept presents the following problems for practical application:

- The need to provide a controllable current source for the triple harmonic current

injection;

- The difficulty to adjust the amplitude and the phase of the injection harmonic current to suit each particular operating condition, as well as synchronizing it with the supply frequency;

- The difficulty to ensure the required harmonic reduction under different operation conditions;

- The inefficiency of the triple harmonic power injection.

The first problem was particularly important due to the difficulty of building a fully controllable current source power supply in 1960's and 1970's. The frequency, amplitude and phase controllable requirements made the concept difficult to implement practically, and thus the harmonic injection concept did not get developed further till 1980.

The concept was developed to a practically applicable stage by J.F. Baird and J. Arrillaga [59]. Some extra components, mainly power switches, were used to generate a step-waveform to approximate the required harmonic current injection, and employed the dc side ripple voltage to realize the natural commutation for the extra power switches. In this scheme the ac current waveforms and the dc voltage waveform are both improved. The dc ripple voltage is re-rectified and added to the dc output to improve the dc output voltage waveform. The **dc ripple reinjection**, the name used for the new concept, overcomes most of the difficulties mentioned above. There is no need to build a controllable current source supply; the amplitude of the reinjection current is automatically adjusted via the way that the fixed portion of the dc current is used to form the reinjection current; the synchronization with the main power supply, frequency and the phase adjustments are automatically achieved via ripple controlled commutation of the added power diodes.

The **ripple reinjection** concept was further developed by J. Arrillaga and M. Villablanca in early 90's, using some extra thyristors to generate a multi-level reinjection current. The amplitude of the multi-level reinjection current is matched to the operating conditions, the frequency and phase are synchronized with the power supply through the added thyristor firing control and the ripple voltage under the natural commutation. Based on the fixed amplitude relation between the dc current and reinjection current the optimum harmonic reduction for all the operation conditions is ensured. As a result the ac current waveform and dc voltage waveform are further improved, and 12-pulse, 18-pulse, 24-pulse, 36-pulse and 48-pulse equivalent high pulse conversion have been demonstrated in [60]-[67]. Therefore line commutated thyristor converters complemented by the ripple reinjection circuit are very effective and can be potential alternatives to multi-pulse conversion based on phase-shifted transformers [68, 69].

An alternative solution to reduce the harmonic distortion was proposed by K. Oguchi. In his proposed converter configurations, the ac outputs of the bridges are combined by harmonic cancelling reactors instead of phase shift transformers. By adding some extra switches and harmonic cancelling reactors, multi-step voltage and current waveforms are obtained at the ac output terminals [29, 70]. Configurations for 18-step [71], 36-step [72], 60-step [73] and 48/72-step [74] have been proposed.

1.3.2 Voltage and Current Reinjection ac-dc Conversion

The voltage and current ratings of the self-commutated power switches (mainly GTO's and IGBT's) are advancing to those of the thyristors, and their switching on/off time is reduced to a few microseconds under rated voltage and current conditions. These switching devices can be used to generate the reinjection waveform without the limitation of the natural commutation conditions.

By using these switches to generate the required waveforms the reinjection concept can be extended to a variety of power converters, without the need for the ripple voltage to provide the commutating voltage; thus the **voltage or current reinjection** concept based on providing appropriate reinjection voltage or current waveforms to the conventional bridges becomes a promising technique for harmonic reduction. By the combination of the **reinjection, soft switching and multi-level conversion** concepts the **multi-level reinjection ac-dc conversion** is a promising alternative for high power and high voltage applications.

The original **harmonic injection and ripple reinjection** concepts were developed for harmonic distortion reduction and the third and ninth harmonic currents were found to be the most suitable injection currents [58], however this reference did not indicate the optimum injection current for harmonic cancellation. In references [65, 67], the reinjection current was determined with the help of a phasor diagram. Although these papers show that the harmonics of the modified waveform are reduced to a low level, they provide no theoretical explanation and evidence that the proposed reinjection waveform has been optimized subject to some specific restrictions.

The **reinjection conversion concept** differs from the conventional ac-dc conversion in that the voltage or current supplied to each bridge is maintained constant; in the reinjection converter the voltage or current applied to the main bridges varies periodically, even though the dc voltage or current remains constant. Therefore the varying reinjection waveforms applied to the bridges have to be optimized for the harmonic suppression and converter performance improvement.

In this thesis the **ideal reinjection** waveforms for perfect harmonic cancellation are first derived; and then the **fully symmetrical reinjection** waveform approximations are proposed to simplify the requirements applied to the dc voltage or current source.

For practical implementation and high performance the reinjection waveforms are approximated by multi-level fully symmetrical reinjection waveforms with or without zero voltage or current level for soft switching. These waveforms can be produced in two different ways:

1. An ac voltage or current waveform is added both in the forward and reverse direction to the dc voltage or current applied to the two main bridges respectively;

2. A dc voltage or current divider is controlled periodically to adjust the portion of the dc voltage or current distributed to the two main bridges.

In the first alternative the reinjection circuitry is powered by the dc source and a reinjection transformer is used to isolate the reinjection waveform ac component from the dc supply [75]-[78]. To simplify the reinjection transformer, the level number of this type of reinjection converters is limited; however this type of reinjection converter can still produce high pulse equivalent ac output waveforms due to the multiplicative effect of the current or voltage reinjection. **ESEDS** (minimization of Error Square and Error Derivative Square) **symmetrical reinjection** waveforms are used by this configuration without exact soft switching conditions but switching on-off under very low voltage or current stress.

The second solution is based on the property that the fully symmetrical reinjection waveforms to the two main bridges add to a dc waveform; therefore a dc voltage or current controllable divider can be used to generate the reinjection waveforms for the two main bridges. The required reinjection waveforms are then approximated by the multi-level reinjection waveforms. The aim of the **linear reinjection** approximation is to use the same rating switches and capacitors (or equal turns windings). To achieve the soft switching, a zero level voltage or current is provided for a time interval, in which the main bridge switching actions take place.

The provision of zero voltage switching condition in the MLVR-VSC (Multi-Level Voltage Reinjection Voltage Source Converter) enables the series connected switches of every main bridge arm to be controlled synchronously without dynamic equal voltage sharing problems (the main difficulty of the direct series connected power switches being used in high power and high voltage applications). Thus the direct series connected switches in the main bridges are of the same power rating and each of the main bridges operates as a conventional six-pulse converter. The simpler structure and control requirements of the main bridge make the converter system more compact and cost effective. Moreover, the lack of clamping for the direct series connection of power switches simplifies the addition of redundant switches to increase the converter reliability.

Similarly the provision of zero current switching condition in the MLCR-CSC (Multi-Level Current Reinjection Current Source Converter) enables the series connected

switches of every main bridge arm to be controlled synchronously as for the series connected thyristor arms of line commutated converters (in which the thyristors turn off after its current decreases to zero). Therefore the well developed techniques of thyristor series connection used in high power conversion can be extended to the reinjection ac-dc self-commutated switch converters.

The ac capacitors, required by self-commutated current source converters to absorb the inductive energy stored in ac side inductance during the switching off process, can be very large. Although their size can be reduced by using PWM techniques, the reduction factor is related to the switching frequency, which can not be very high for high power application. In general the main problem of self-commutated current source converters without zero current switching is their interfacing with the ac power system; that is why FACTS devices do not use self-commutated CSC (Current Source Converter) and HVDC prefers thyristor CSC to self-commutated CSC, although the self-commutated CSC can offer excellent performance.

The provision of ZCS to the MLCR CSC makes it look like a thyristor converter as far as the interface with ac power system is concerned, but with four quadrant operation capability. Therefore the MLCR CSC could be a promising alternative for FACTS and HVDC transmission applications.

1.4 THESIS OUTLINE

This thesis consists of 9 chapters. The present chapter has given a brief review of the multi-level conversion, soft switching and the ripple reinjection concepts. The multi-level voltage and current reinjection concept is also introduced briefly.

Chapter 2 derives the **ideal reinjection** waveforms for 12-pulse and 6-pulse ac-dc conversion configurations based on the harmonic cancellation principles. The two approximations of the ideal reinjection waveforms under restriction of full symmetry are derived to simplify the requirement applied to the dc voltage and current sources. The **multi-level full symmetrical reinjection** waveforms are proposed for practical implementations.

Chapter 3 introduces and analyzes the multi-level reinjection VSC with a reinjection transformer based on the **ESEDS reinjection** waveform. The series and parallel connected bridge schemes are analyzed.

Chapter 4, 5 and 6 are concerned with the **MLVR-VSC** (Multi-Level Voltage Reinjection Voltage Source converters). Chapter 4 describes the topological structures of the reinjection voltage generation circuits; Chapter 5 analyzes the voltage and current waveforms and the component ratings of the MLVR-VSC; Chapter 6 discusses the issue of the dc capacitor voltage balance of the MLVR-VSC.

Chapter 7 describes the results of simulation studies of the MLVR-VSC and ESEDS-VSC using the PSCAD/EMTDC package. The particular applications considered are the STATCOM for the MLVR-VSC and BTBVSCL (Back-To-Back VSC Link) for ESEDS-VSC respectively.

Chapter 8 gives a brief description of the **MLCR-CSC** (Multi-Level Current Reinjection Current Source Converter). The possible topological structures and an example MLCR-CSC simulation study are presented.

Chapter 9 summaries the general conclusion of the thesis and makes suggestions for further work.

Chapter 2

PRINCIPLES OF THE REINJECTION CONCEPT

2.1 INTRODUCTION

There are many applications requiring electrical power conversion from dc to ac or from ac to dc. The three phase converters formed by solid state self-commutated switches are widely used in the power range from a few kVA to more than 100MVA.

The converters are divided into the categories of Voltage Source Converters (VSC) and Current Source Converters (CSC) based on their dc side voltage and current characteristics. The VSC dc side voltage is stable and nearly constant, while the CSC dc side current is stable and nearly constant.

For high power applications parallel or series connections of the three phase bridges are adopted commonly. The dc side voltage across a bridge (for VSC) or the dc side output current from a bridge (for CSC) are maintained constant in the conventional configurations, because the dc side voltage and current, or a portion of them, are directly applied to the bridges. The constant dc voltage or dc current are converted by the switching action in the bridges into ac voltage or current waveforms with a large amount of harmonic distortion.

The reinjection concept differs from the conventional VSC or CSC in that the voltage applied, or the current supplied, to a bridge varies periodically even though the dc voltage or current remains stable and almost constant. A periodically varying waveform is supplied to the bridge and used to shape the ac side voltage or current into the specified waveforms. High power converters consist of more than one full or half bridges, the most commonly used being the 6-pulse and 12-pulse configurations. In these configurations the individual bridges are supplied by differently varying waveforms to obtain the specified ac voltage or current waveforms on their ac sides. By appropriate combinations of these waveforms, under the ideal conditions, all the specified harmonics can be cancelled and thus sinusoidal waveforms provided at the converter system output terminals.

Based on the reinjection concept the voltage or current waveforms applied to their main bridges are modified from constant to periodically varying, however these periodically

varying waveforms, the reinjection waveforms, need to be optimized subject to some specified restrictions.

The **Ideal Reinjection** waveforms to achieve perfect harmonic cancellation are first derived for the 6-pulse and 12-pulse configurations respectively; to simplify the requirements applying to the dc source, two approximations are made to the ideal reinjection waveforms, i.e. the fully symmetrical **ESEDS** (minimization of Error Square and Error derivation Square) and **Linear Reinjection**.

Finally multi-level fully symmetrical reinjection approximations are made to the ESEDS and Linear Reinjection waveforms for practical implementation. From these multi-level reinjection waveforms a new concept, the **Multi-Level Voltage or Current Reinjection conversion** emerges.

Based on this concept new schemes, the MLVR (Multi-Level Voltage Reinjection) VSC (Voltage Source Converters) and MLCR (Multi-Level Current Reinjection) CSC (Current Source Converters), combine the reinjection and multi-level conversion concepts as well as soft switching techniques to provide a solution for high power ac-dc conversion. These new configurations produce high quality ac output waveforms with negligible harmonic distortion, low dV/dt and dI/dt stress on both ac and dc sides, and reduce switching losses by using low switching frequency and soft switching; and thus are suitable for high voltage and high power applications.

2.2 ANALYSIS OF HARMONIC CANCELLATION CONDITIONS

The power switches in every arm of the six-pulse converter are switched to on state for one third of the fundamental period (120^o pattern) or for half the period (180^o pattern).

Because the condition in which both arms of a bridge leg are off-state causes uncertainty in the output voltage, the 180^o pattern is used by most VSC's. Because the power switch can only keep in on-state under forward voltage, and the two power switches connected to a common node can not be in on state at the same time, the 120^o pattern is used by the most CSC's. The following analysis is therefore developed under the 120^o and 180^o switching patterns for CSC and VSC respectively.

2.2.1 Harmonic Cancellation for 12-pulse VSC

The bare 12-pulse VSC configuration, shown in Figure 2.1, consists of two three phase full bridges and two interface transformers. The two interface transformers are commonly arranged in Y/Y and Y/Δ connections, and their primary windings (ac power side) are connected in series to produce an ac output voltage which is the sum of the two interface primary winding voltages. The turns ratios are $k_n : 1$ and $k_n : \sqrt{3}$ for the Y/Y and Y/Δ connection transformers respectively. In Figure 2.1 the GTO symbols

represent ideal power switches with bidirectional blocking and unidirectional current passing ability, the diodes are ideal diodes and the interface transformers are ideal transformers.

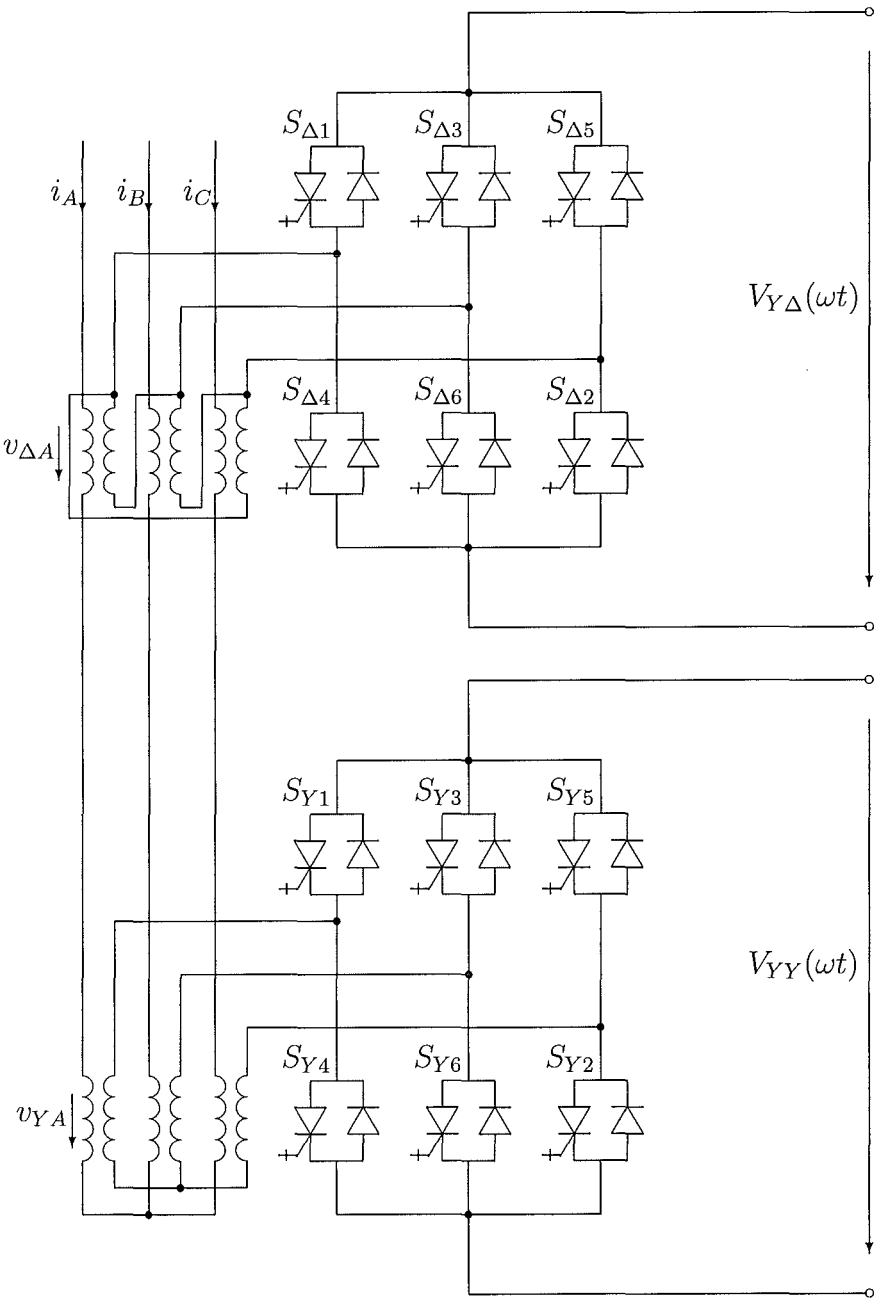


Figure 2.1 The 12-pulse VSC configuration

The voltages supplied to the dc terminals are $V_{YY}(\omega t)$ and $V_{Y\Delta}(\omega t)$ for the bridges connected to the Y/Y and Y/Δ connected transformers respectively. The 180^o pattern is used to fire the two bridges:

arm S_{Y1} is switched to on-state at $\omega t = \cdots, 0,\ 2\pi,\ 4\pi,\ \cdots,$
and arm S_{Y4} at $\omega t = \cdots,\ \pi,\ 3\pi,\ 5\pi,\ \cdots.$
Similarly arm $S_{\Delta 1}$ is switched to on-state at $\omega t = \cdots,\ \pi/6,\ 13\pi/6,\ 25\pi/6,\ \cdots,$
and arm $S_{\Delta 4}$ at $\omega t = \cdots,\ 7\pi/6,\ 19\pi/6,\ 31\pi/6,\ \cdots.$

The secondary winding voltages of the two interface transformers on the bridge side are given by

$$V_{Ya}(\omega t) = \begin{cases} V_{YY}(\omega t)/3 & 0 < \omega t < \pi/3 \\ 2V_{YY}(\omega t)/3 & \pi/3 < \omega t < 2\pi/3 \\ V_{YY}(\omega t)/3 & 2\pi/3 < \omega t < \pi \\ -V_{YY}(\omega t)/3 & \pi < \omega t < 4\pi/3 \\ -2V_{YY}(\omega t)/3 & 4\pi/3 < \omega t < 5\pi/3 \\ -V_{YY}(\omega t)/3 & 5\pi/3 < \omega t < 2\pi \end{cases} \tag{2.1}$$

$$V_{\Delta a}(\omega t) = \begin{cases} 0 & 0 < \omega t < \pi/6 \\ V_{Y\Delta}(\omega t) & \pi/6 < \omega t < 5\pi/6 \\ 0 & 5\pi/6 < \omega t < 7\pi/6 \\ -V_{Y\Delta}(\omega t) & 7\pi/6 < \omega t < 11\pi/6 \\ 0 & 11\pi/6 < \omega t < 2\pi \end{cases} \tag{2.2}$$

If $V_{YY}(\omega t) = V_{dc} + A_{Ym}\cos(m\omega t) + B_{Ym}\sin(m\omega t)$
$V_{Y\Delta}(\omega t) = V_{dc} + A_{\Delta m}\cos(m\omega t) + B_{\Delta m}\sin(m\omega t),$
the Fourier components of the Y/Y connected transformer secondary winding voltage $V_{Ya}(\omega t)$ are given by

$$\begin{aligned} V_{Yan} &= \frac{2}{\pi}\Big[\int_0^{\pi} \frac{V_{YY}(\omega t)}{3}\sin(n\omega t)d\omega t + \int_{\frac{\pi}{3}}^{\frac{2\pi}{3}} \frac{V_{YY}(\omega t)}{3}\sin(n\omega t)d\omega t\Big] \\ &= V_{dcYan} + V_{cosYan} + V_{sinYan} \end{aligned} \tag{2.3}$$

$$V_{dcYan} = \frac{4[1-(-1)^n]}{3n\pi} V_{dc}\cos^2(\frac{n\pi}{6}) \tag{2.4}$$

$$V_{cosYan} = \begin{cases} \frac{[1-(-1)^{n+m}]A_{Ym}}{3\pi}[\frac{2n}{n^2-m^2} + \frac{1}{n+m}\cos(\frac{(n+m)\pi}{3}) + \frac{1}{n-m}\cos(\frac{(n-m)\pi}{3})] & (m \neq n) \\ 0 & (m = n) \end{cases} \tag{2.5}$$

$$V_{sinYan} = \begin{cases} \frac{[1+(-1)^{n+m}]}{3\pi}B_{Ym}[\frac{1}{n+m}\sin(\frac{(n+m)\pi}{3}) - \frac{1}{n-m}\sin(\frac{(n-m)\pi}{3})] & (m \neq n) \\ \frac{1}{3\pi}B_{Ym}[\frac{4\pi}{3} - \frac{(-1)^m}{2m}\sin(\frac{m\pi}{3})] & (m = n) \end{cases} \tag{2.6}$$

Similarly the Fourier components of the Y/Δ connected transformer secondary winding

voltage $V_{\Delta a}(\omega t)$ are given by

$$V_{\Delta an} = \frac{2}{\pi}\int_{\frac{\pi}{6}}^{\frac{5\pi}{6}} V_{Y\Delta}(\omega t)\sin(n\omega t)d\omega t = \quad V_{dc\Delta an} + V_{cos\Delta an} + V_{sin\Delta an} \tag{2.7}$$

$$V_{dc\Delta an} = \frac{2[1-(-1)^n]}{n\pi} V_{dc}\cos(\frac{n\pi}{6}) \tag{2.8}$$

$$V_{cos\Delta an} = \begin{cases} \frac{[1-(-1)^{n+m}]}{\pi} A_{\Delta m}[\frac{1}{n+m}\cos(\frac{(n+m)\pi}{6}) + \frac{1}{n-m}\cos(\frac{(n-m)\pi}{6})] & (m \neq n) \\ 0 & (m = n) \end{cases} \tag{2.9}$$

$$V_{sin\Delta an} = \begin{cases} \frac{[1+(-1)^{n+m}]}{\pi} B_{\Delta m}[\frac{1}{n+m}\sin(\frac{(n+m)\pi}{6}) - \frac{1}{n-m}\sin(\frac{(n-m)\pi}{6})] & (m \neq n) \\ \frac{1}{\pi}B_{\Delta m}[\frac{2\pi}{3} + \frac{1}{m}\sin(\frac{m\pi}{3})] & (m = n) \end{cases} \tag{2.10}$$

The three components of V_{Yan}(equation 2.3), i.e. V_{dcYan} (corresponding to the bridge voltage dc component V_{dc}), V_{cosYan} (corresponding to the bridge voltage ac component $A_{Ym}\cos(m\omega t)$) and V_{sinYan} (corresponding to the bridge voltage ac component $B_{Ym}\sin(m\omega t)$) given by equations 2.4 to 2.6 possess the following characteristics.

The Fourier expression of V_{dcYan} indicates that the harmonics produced by the dc component are of orders $n = 6l \pm 1$ $(l = 1, 2, \cdots)$.

The harmonic spectrum of V_{cosYan} depends on the frequency of the corresponding bridge voltage component $A_{Ym}(m\omega t)$; if $m = 6k$ $(k = 1, 2, \cdots)$,

$$\begin{aligned} V_{cosYan} &= \frac{[1-(-1)^n]}{3\pi} A_{Ym}[\frac{2n}{n^2-36k^2} + \frac{1}{n+6k}\cos(\frac{n\pi}{3}) + \frac{1}{n-6k}\cos(\frac{n\pi}{3})] \\ &= \frac{[1-(-1)^n]}{3\pi} A_{Ym}[\frac{2n}{n^2-36k^2} + \frac{2n}{n^2-36k^2}\cos(\frac{n\pi}{3})] \\ &= \frac{4n[1-(-1)^n]}{3\pi(n^2-36k^2)} A_{Ym}\cos^2(\frac{n\pi}{6}) \end{aligned} \tag{2.11}$$

Equation 2.11 indicates that its harmonic components are of the same orders as those of V_{dcYan}. This means that by choosing the appropriate amplitude of $A_{Ym}\cos(m\omega t)$ and frequency factor $m = 6k$ $(k = 1, 2, \cdots)$, the harmonic components of the secondary winding voltage part $V_{dcYa}(\omega t)$ can be modified, i.e. harmonics of some orders can be decreased while those of other orders increased.

V_{sinYan}, contains even order harmonics, which is undesirable, and therefore the voltage across the bridge connected to the Y/Y transformer will not include the component $B_{Ym}\sin(m\omega t)$.

Similarly, the three components of $V_{\Delta an}$, i.e. $V_{dc\Delta an}$ (corresponding to the bridge voltage dc component V_{dc}), $V_{cos\Delta an}$ (corresponding to the bridge voltage ac compo-

nent $A_{\Delta m}\cos(m\omega t)$) and $V_{sin\Delta an}$ (corresponding to the bridge voltage ac component $B_{\Delta m}\sin(m\omega t)$) given by equations 2.8 to 2.10 possess the following characteristics.

The Fourier expression of $V_{dc\Delta an}$ indicates that the harmonics are of orders $n = 6l \pm 1$ $(l = 1, 2, \cdots)$.

The spectrum of $V_{cos\Delta an}$ depends on the frequency of the corresponding bridge voltage component $A_{\Delta m}(m\omega t)$; if $m = 6k$ $(k = 1, 2, \cdots)$,

$$\begin{aligned} V_{cos\Delta an} &= \frac{[1-(-1)^n]}{\pi} A_{\Delta m}[\frac{(-1)^k}{n+6k}\cos(\frac{n\pi}{6}) + \frac{(-1)^k}{n-6k}\cos(\frac{n\pi}{6})] \\ &= \frac{(-1)^k[1-(-1)^n]}{\pi} A_{\Delta m}[\frac{1}{n+6k} + \frac{1}{n-6k}]\cos(\frac{n\pi}{6}) \\ &= \frac{2n(-1)^k[1-(-1)^n]}{\pi(n^2-36k^2)} A_{\Delta m}\cos(\frac{n\pi}{6}) \end{aligned} \tag{2.12}$$

Equation 2.12 indicates that its harmonic components are of the same orders as those of $V_{dc\Delta an}$. This means that by choosing the appropriate amplitude of $A_{\Delta m}\cos(m\omega t)$ and frequency factor $m = 6k$ $(k = 1, 2, \cdots)$, the harmonic components of the secondary winding voltage part $V_{dc\Delta a}(\omega t)$ can be modified , i.e. harmonics of some orders can be decreased while those of other orders increased.

$V_{sin\Delta an}$ also contains even order harmonics, and therefore the voltage across the bridge connected to the Y/Δ connection transformer will not include the component $B_{\Delta m}\sin(m\omega t)$.

In the conventional 12-pulse configuration the harmonics of order $n = 6(2l-1) \pm 1$ $(l = 1, 2, \cdots)$ of the Y/Y and Y/Δ interface transformer winding voltages $V_{Ya}(\omega t)$ and $V_{\Delta a}(\omega t)$ are out of phase by 180^o; while the harmonics of order $n = 12l \pm 1$ $(l = 1, 2, \cdots)$ are in phase. If the voltage across the bridge connected to the Y/Y transformer is

$$V_{YY}(\omega t) = V_{dc} + \sum_{k=1}^{\infty} A_{Yk}\cos(6k\omega t) \tag{2.13}$$

and the voltage across the bridge connected to the Y/Δ transformer is

$$V_{Y\Delta}(\omega t) = V_{dc} + \sum_{k=1}^{\infty} A_{\Delta k}\cos(6k\omega t) \tag{2.14}$$

and if the corresponding winding voltages $V_{Ya}(\omega t)$ and $V_{\Delta a}(\omega t)$ only include harmonics of order $n = 6(2l-1) \pm 1$ $(l = 1, 2, \cdots)$, then the combination of the winding voltages on the interface transformer primary side will produce harmonic distortion-free voltage waveforms. To achieve this goal the relation between the dc component and ac components of the bridge voltages is given by the equations

$$\sum_{k=1}^{\infty} \frac{A_{Yk}}{(12l \pm 1)^2 - 36k^2} = \frac{V_{dc}}{(12l \pm 1)^2} \qquad l = 1, 2, \cdots \tag{2.15}$$

$$\sum_{k=1}^{\infty} \frac{(-1)^k A_{\Delta k}}{(12l \pm 1)^2 - 36k^2} = \frac{V_{dc}}{(12l \pm 1)^2} \qquad l = 1, 2, \cdots \tag{2.16}$$

For the cancellation of the primary side harmonics of orders $n = 6(2l-1) \pm 1$ ($l = 1, 2, \cdots$), the relation $(-1)^k A_{\Delta k} = A_{Yk}$ ($k = 1, 2, \cdots$) must be satisfied. Therefore the condition for harmonic cancellation in the 12-pulse reinjection VSC is simplified to that of Equation 2.15.

2.2.2 Harmonic Cancellation for 12-pulse CSC

The 12-pulse CSC configuration, shown in Figure 2.2, consists of two three phase full bridges and an interface transformer connected in $Y/(\Delta - Y)$ or $\Delta/(\Delta - Y)$ (i.e. the secondary Y and Δ windings are connected to the two three-phase bridges individually). In Figure 2.2 the GTO symbols represent ideal switches with bidirectional voltage blocking and unidirectional current passing ability; the interface transformer is also ideal, the turns ratios being $k_n : 1$ and $k_n : \sqrt{3}$ for the ac system side windings to the Y connection windings and Δ connection windings respectively.

The currents supplied to the Y and Δ connected bridges from their dc sides are denoted $I_{BY}(\omega t)$ and $I_{B\Delta}(\omega t)$ respectively. The 120^o pattern is used to control the firing of the bridges, arm $S_{\Delta 6}$ being switched to on-state at $\omega t = 0, 2\pi, 4\pi, \cdots$ and switched to off-state at $\omega t = \cdots, 2\pi/3, 8\pi/3, 14\pi/3, \cdots$. Similarly arm $S_{\Delta 1}$ is switched to on-state at $\omega t = \cdots, \pi/3, 7\pi/3, 13\pi/3, \cdots$ and to off-state at $\omega t = \cdots, \pi, 3\pi, 5\pi, \cdots$.

The currents in the two secondary windings of the interface transformer on the bridge dc sides are given by

$$I_{\Delta a}(\omega t) = \begin{cases} I_{B\Delta}(\omega t)/3 & 0 < \omega t < \pi/3 \\ 2I_{B\Delta}(\omega t)/3 & \pi/3 < \omega t < 2\pi/3 \\ I_{B\Delta}(\omega t)/3 & 2\pi/3 < \omega t < \pi \\ -I_{B\Delta}(\omega t)/3 & \pi < \omega t < 4\pi/3 \\ -2I_{B\Delta}(\omega t)/3 & 4\pi/3 < \omega t < 5\pi/3 \\ -I_{B\Delta}(\omega t)/3 & 5\pi/3 < \omega t < 2\pi \end{cases} \tag{2.17}$$

$$I_{Ya}(\omega t) = \begin{cases} 0 & 0 < \omega t < \pi/6 \\ I_{BY}(\omega t) & \pi/6 < \omega t < 5\pi/6 \\ 0 & 5\pi/6 < \omega t < 7\pi/6 \\ -I_{BY}(\omega t) & 7\pi/6 < \omega t < 11\pi/6 \\ 0 & 11\pi/6 < \omega t < 2\pi \end{cases} \tag{2.18}$$

By comparing Equations 2.1 and 2.2 with Equations 2.17 and 2.18, and using the duality existing between VSC and CSC, the analytical results for the 12-pulse reinjection VSC

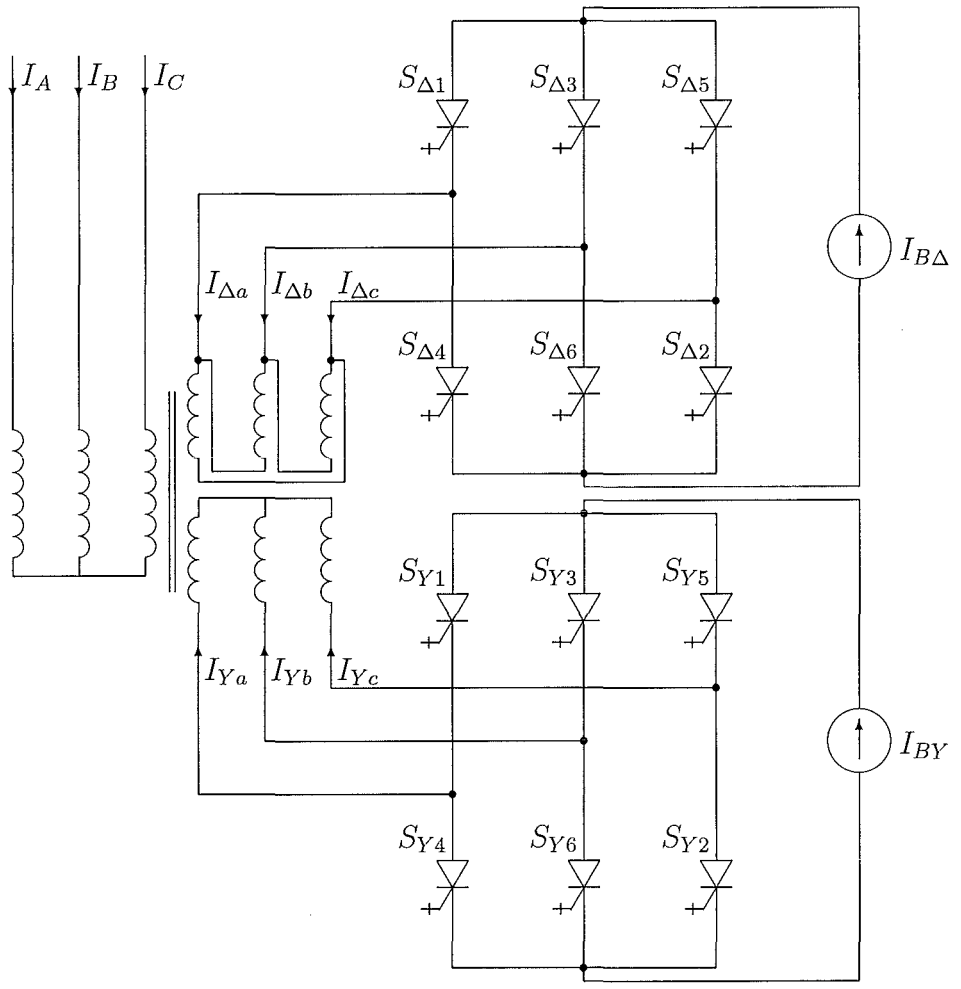


Figure 2.2 The 12-pulse CSC configuration

can be extended to 12-pulse reinjection CSC. Therefore if the current supplied to the bridge connected to Y connection windings is

$$I_{BY}(\omega t) = I_{dc} + \sum_{k=1}^{\infty} A_{Yk} \cos(6k\omega t) \tag{2.19}$$

and the current supplied to the bridge connected to Δ connection windings is

$$I_{B\Delta}(\omega t) = I_{dc} + \sum_{k=1}^{\infty} A_{\Delta k} \cos(6k\omega t) \tag{2.20}$$

The corresponding winding currents $I_{Ya}(\omega t)$ and $I_{\Delta a}(\omega t)$ only include harmonics of orders $n = 6(2l-1) \pm 1$ $(l = 1, 2, \cdots)$. Thus the ac side winding current is the combination of the currents coupled from the converter side winding currents, and by

the cancellation of the harmonics of order $n = 6(2l-1) \pm 1$ $(l = 1, 2, \cdots)$ a harmonic distortion-free current waveform is achieved at the output terminals. To obtain this ideal waveform the relation between the dc and ac components of the bridge currents are given by the equations

$$\sum_{k=1}^{\infty} \frac{(-1)^k A_{Yk}}{(12l \pm 1)^2 - 36k^2} = \frac{I_{dc}}{(12l \pm 1)^2} \qquad l = 1, 2, \cdots \tag{2.21}$$

$$\sum_{k=1}^{\infty} \frac{A_{\Delta k}}{(12l \pm 1)^2 - 36k^2} = \frac{I_{dc}}{(12l \pm 1)^2} \qquad l = 1, 2, \cdots \tag{2.22}$$

2.2.3 Harmonic Cancellation for 6-pulse CSC

To simplify the description the 6-pulse CSC configuration is treated as two 3-phase half bridges and an interface transformer connected in $\Delta/(Y-Y)$ (the secondary Y windings connected to the two three phase half bridges individually). Figure 2.3 shows this configuration. The primary windings are connected in Δ to form a free path for triplen harmonic currents, and the line current, which is the sum of two winding currents, should become a harmonic free waveform by the perfect harmonic cancellation.

The currents supplied to the two half bridges from the dc side are $I_{BPY}(\omega t)$ and $I_{BNY}(\omega t)$ respectively. The 120^o pattern is used to control the firing of the switches in the two half bridges. If arm S_1 is switched to on-state at $\omega t = \cdots, -\pi/3, 5\pi/3, 11\pi/3, \cdots$ and to off-state at $\omega t = \cdots, \pi/3, 7\pi/3, 13\pi/3, \cdots$, and arm S_4 is switched to on-state at $\omega t = \cdots, 2\pi/3, 8\pi/3, 14\pi/3, \cdots$ and to off-state at $\omega t = \cdots, 4\pi/3, 10\pi/3, 16\pi/3, \cdots$, I_{Pa} and I_{Na}, the currents in the interface transformer windings, are given by

$$I_{Pa}(\omega t) = \begin{cases} 0 & -4\pi/3 < \omega t < -\pi/3 \\ I_{BPY}(\omega t) & -\pi/3 < \omega t < \pi/3 \\ 0 & \pi/3 < \omega t < 5\pi/3 \end{cases} \tag{2.23}$$

$$I_{Na}(\omega t) = \begin{cases} 0 & -2\pi/3 < \omega t < 2\pi/3 \\ I_{BNY}(\omega t) & 2\pi/3 < \omega t < 4\pi/3 \\ 0 & 4\pi/3 < \omega t < 8\pi/3 \end{cases} \tag{2.24}$$

If $\quad I_{BPY}(\omega t) = I_{dc} + A_{PYm}\cos(m\omega t) + B_{PYm}\sin(m\omega t)$
and $\quad I_{BNY}(\omega t) = I_{dc} + A_{NYm}\cos(m\omega t) + B_{NYm}\sin(m\omega t)$,
the Fourier components of the converter side phase current $I_{Pa}(\omega t)$ are given by

$$\begin{aligned} I_{Pan} &= \int_{-\pi/3}^{\pi/3} \left[\frac{I_{dc} + A_{PYm}\cos(m\omega t)}{\pi} \cos(n\omega t) + \frac{B_{PYm}\sin(m\omega t)}{\pi} \sin(n\omega t) \right] d\omega t \\ &= I_{dcPan} + I_{cosPan} + I_{sinPan} \qquad n = 1, 2, \cdots \end{aligned} \tag{2.25}$$

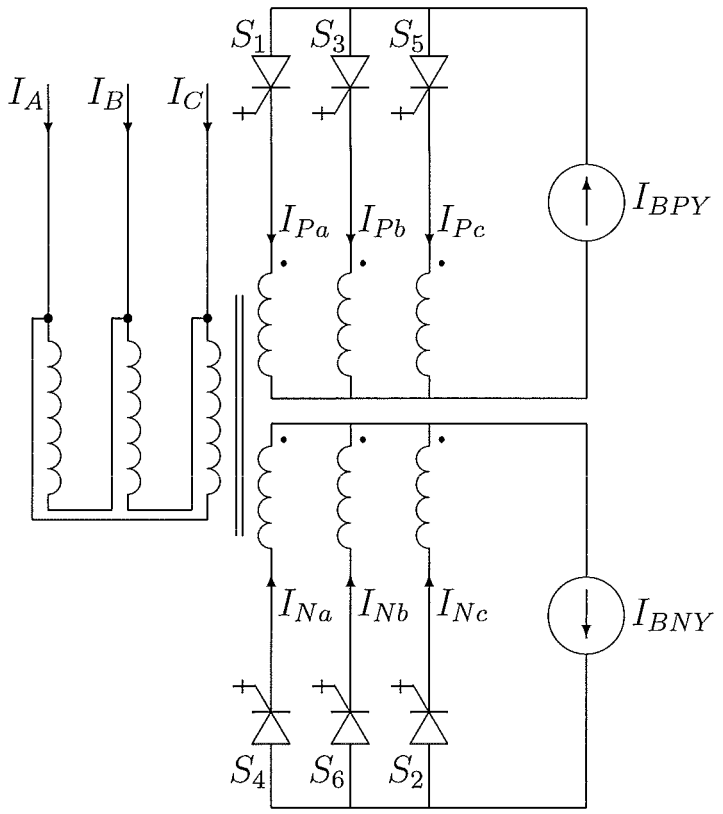


Figure 2.3 The 6-pulse CSC configuration

where

$$I_{dcPan} = \begin{cases} \frac{2}{n\pi} I_{dc} \sin(\frac{n\pi}{3}) & n = 1, 2, \cdots \\ \frac{1}{3} I_{dc} & n = 0 \end{cases} \tag{2.26}$$

$$I_{cosPan} = \begin{cases} \frac{1}{\pi} A_{PYm} [\frac{1}{n+m} \sin(\frac{(n+m)\pi}{3}) + \frac{1}{n-m} \sin(\frac{(n-m)\pi}{3})] & (m \neq n) \\ \frac{1}{\pi} A_{PYm} [\frac{1}{n+m} \sin(\frac{(n+m)\pi}{3}) + \frac{\pi}{3}] & (m = n) \end{cases} \tag{2.27}$$

$$I_{sinPan} = \begin{cases} \frac{1}{\pi} B_{PYm} [\frac{1}{n-m} \sin \frac{(n-m)\pi}{3} - \frac{1}{n+m} \sin \frac{(n+m)\pi}{3}] & (m \neq n) \\ \frac{1}{\pi} B_{PYm} [\frac{\pi}{3} - \frac{1}{n+m} \sin \frac{(n+m)\pi}{3}] & (m = n) \end{cases} \tag{2.28}$$

And the Fourier components of the winding current $I_{Na}(\omega t)$ are given by

$$\begin{aligned} I_{Nan} &= \int_{2\pi/3}^{4\pi/3} \Big[\frac{I_{dc} + A_{NYm} \cos(m\omega t)}{\pi} \cos(n\omega t) + \frac{B_{NYm} \sin(m\omega t)}{\pi} \sin(n\omega t) \Big] d\omega t \\ &= I_{dcNan} + I_{cosNan} + I_{sinNan} \qquad n = 1, 2, \cdots \end{aligned} \tag{2.29}$$

where

$$I_{dcNan} = \begin{cases} \frac{2(-1)^n}{n\pi} I_{dc} \sin(\frac{n\pi}{3}) & n = 1, 2, \cdots \\ \frac{1}{3} I_{dc} & n = 0 \end{cases} \tag{2.30}$$

$$I_{cosNan} = \begin{cases} \frac{1}{\pi} A_{NYm} [\frac{(-1)^{n+m}}{n+m} \sin(\frac{(n+m)\pi}{3}) + \frac{(-1)^{n-m}}{n-m} \sin(\frac{(n-m)\pi}{3})] & (m \neq n) \\ \frac{1}{\pi} A_{NYm} [\frac{(-1)^{n+m}}{n+m} \sin(\frac{(n+m)\pi}{3}) + \frac{\pi}{3}] & (m = n) \end{cases} \tag{2.31}$$

$$I_{sinNan} = \begin{cases} \frac{1}{\pi} B_{NYm} [\frac{(-1)^{n-m}}{n-m} \sin(\frac{(n-m)\pi}{3}) - \frac{(-1)^{n-m}}{n+m} \sin(\frac{(n+m)\pi}{3})] & (m \neq n) \\ \frac{1}{\pi} B_{NYm} [\frac{\pi}{3} - \frac{(-1)^{n+m}}{n+m} \sin(\frac{(n+m)\pi}{3})] & (m = n) \end{cases} \tag{2.32}$$

The three components of I_{Pan} in equation 2.25, i.e. I_{dcPan} (corresponding to the bridge current dc component I_{dc}), I_{cosPan} (corresponding to the bridge current ac component $A_{PYm} \cos(m\omega t)$) and I_{sinPan} (corresponding to the bridge current ac component $B_{PYm} \sin(m\omega t)$) given by Equations 2.26 to 2.28 possess the following characteristics.

The Fourier expression of I_{dcPan} indicates that the harmonics are those excluding the orders $n = 3l$ $(l = 1, 2, \cdots)$.

The spectrum of I_{cosPan} depends on the frequency of the corresponding bridge side reinjection current component $A_{PYm} \cos(m\omega t)$; if $m = 3k$ $(k = 1, 2, \cdots)$,

$$\begin{aligned} I_{cosPan} &= \begin{cases} \frac{1}{\pi} A_{PYm} [\frac{(-1)^k}{n+3k} \sin(\frac{n\pi}{3}) + \frac{(-1)^k}{n-3k} \sin(\frac{n\pi}{3})] & (m \neq n) \\ \frac{1}{\pi} A_{PYm} [\frac{(-1)^k}{n+3k} \sin(\frac{n\pi}{3}) + \frac{\pi}{3}] & (m = n) \end{cases} \\ &= \begin{cases} \frac{(-1)^k}{\pi} A_{PYm} \frac{2n}{n^2 - 9k^2} \sin(\frac{n\pi}{3}) & (n \neq m) \\ \frac{A_{PYm}}{3} & (n = m) \end{cases} \end{aligned} \tag{2.33}$$

Equation 2.33 indicates that its spectrum consists of the same harmonic orders as those of I_{dcPYan} except for the orders $n = m = 3k$. That implies that by choosing the appropriate amplitude of A_{Ym} and a frequency factor $m = 3k$ $(k = 1, 2, \cdots)$, the harmonics of the winding current part $I_{dcPa}(\omega t)$ can be modified by the part $I_{cosPa}(\omega t)$.

The I_{sinPan} term generated by the bridge current component $B_{PYm} \sin(m\omega t)$, can not reduce any harmonics of the winding current $I_{dcPa}(\omega t)$ because all the harmonics of the same order are out of phase by 90^o.

Similarly, the three components of I_{Nan}, i.e. I_{dcNan} (corresponding to the bridge current dc component I_{dc}), I_{cosNan} (corresponding to the bridge current ac component $A_{NYm} \cos(m\omega t)$) and I_{sinNan} (corresponding to the bridge current ac component $B_{NYm} \sin(m\omega t)$) given by Equations 2.30 to 2.32 possess the following characteristics.

The Fourier expression of I_{dcNan} indicates that the I_{dcNan} harmonics are those excluding the orders $n = 3l$ $(l = 1, 2, \cdots)$.

The spectrum of I_{cosNan} depends on the frequency of the corresponding bridge current component $A_{NYm}\cos(m\omega t)$; if $m = 3k$ $(k = 1, 2, \cdots)$,

$$I_{cosNan} = \begin{cases} \frac{1}{\pi}A_{NYm}[\frac{(-1)^n}{n+3k}\sin(\frac{n\pi}{3}) + \frac{(-1)^n}{n-3k}\sin(\frac{n\pi}{3})] & (n \neq 3k) \\ \frac{1}{\pi}A_{NYm}[\frac{(-1)^n}{n+3k}\sin(\frac{n\pi}{3}) + \frac{\pi}{3}] & (n = 3k) \end{cases}$$
$$= \begin{cases} \frac{(-1)^n}{\pi}A_{NYm}\frac{2n}{n^2-9k^2}\sin(\frac{n\pi}{3}) & (n \neq m) \\ \frac{A_{NYm}}{3} & (n = m) \end{cases} \tag{2.34}$$

Equation 2.34 indicates that its spectrum consist of the same harmonic order components as those of I_{dcNan}. That means that by choosing the appropriate amplitude of A_{NYm} and a frequency factor $m = 3k$ $(k = 1, 2, \cdots)$, the harmonics of the winding current part $I_{dcNa}(\omega t)$ can be modified too.

The term I_{sinNan} caused by the bridge current component $B_{NYm}\sin(m\omega t)$, can not reduce the harmonic amplitude of the winding current component I_{dcNa} due to their harmonics of the same orders being out of phase by 90^o. Therefore the bridge reinjection current will not include component $B_{NYm}\sin(m\omega t)$.

Based on the analysis above, to ensure harmonic cancellation, if the currents supplied to the two bridges are

$$I_{BPY}(\omega t) = I_{dc} + \sum_{k=1}^{\infty} A_{PYk}\cos(k\omega t) \tag{2.35}$$

$$I_{BNY}(\omega t) = I_{dc} + \sum_{k=1}^{\infty} A_{NYk}\cos(k\omega t) \tag{2.36}$$

the Fourier components of the winding currents $I_{Pa}(\omega t)$ and $I_{Na}(\omega t)$ are given by

$$I_{Pa}(\omega t) = \frac{1}{3}I_{dc} + \sum_{n=1}^{\infty}\frac{2I_{dc}}{n\pi}\sin(\frac{n\pi}{3})\cos(n\omega t)$$
$$+ \sum_{n=1,\ n\neq 3k}^{\infty}\left[\sum_{k=1}^{\infty}\frac{2(-1)^k nA_{PYk}}{\pi(n^2-9k^2)}\sin\frac{n\pi}{3}\cos(n\omega t)\right] + \sum_{k=1}^{\infty}\frac{A_{PYk}}{3}\cos(3k\omega t) \tag{2.37}$$

$$I_{Na}(\omega t) = \frac{1}{3}I_{dc} + \sum_{n=1}^{\infty}\frac{2(-1)^n I_{dc}}{n\pi}\sin(\frac{n\pi}{3})\cos(n\omega t)$$
$$+ \sum_{n=1,\ n\neq 3k}^{\infty}\left[\sum_{k=1}^{\infty}\frac{2(-1)^n nA_{NYk}}{\pi(n^2-9k^2)}\sin(\frac{n\pi}{3})\cos(n\omega t)\right] + \sum_{k=1}^{\infty}\frac{A_{NYk}}{3}\cos(3k\omega t) \tag{2.38}$$

By comparing Equations 2.37 and 2.38, as the primary winding current is $I_{\Delta A}(\omega t)/k_n = I_{PYa}(\omega t) - I_{NYa}(\omega t)$ (k_n being the turns ration of the interface transformer), this current will not include a dc component or even order harmonics, if $A_{NYk} = -A_{PYk}$ for $k = (2j-1)$ $(j = 1, 2, \cdots)$; while $A_{NYk} = A_{PYk}$ for $k = 2j$ $(j = 1, 2, \cdots)$; i.e. when k is an odd number, the phase displacement between $A_{PYk}\cos(3k\omega t)$ and $A_{NYk}\cos(3k\omega t)$ is 180^o; and if k is an even number, $A_{PYk}\cos(3k\omega t)$ and $A_{NYk}\cos(3k\omega t)$ are in phase. Under the conditions of $A_{NYk} = -A_{PYk}$ for $k = (2j-1)$ $(j = 1, 2, \cdots)$, and $A_{NYk} = A_{PYk}$ for $k = 2j$ $(j = 1, 2, \cdots)$, the primary winding current $I_{\Delta A}(\omega t)$ is given by

$$\begin{aligned} I_{\Delta A}(\omega t)/k_n &= I_{PYa}(\omega t) - I_{NYa}(\omega t) \\ &= \sum_{k=1}^{\infty} \frac{2[1-(-1)^k]A_{PYk}}{3}\cos(3k\omega t) + \sum_{n=1}^{\infty} \frac{2[1-(-1)^n]}{n\pi} I_{dc}\sin(\frac{n\pi}{3})\cos(n\omega t) \\ &\quad + \sum_{n=1, n\neq 3k}^{\infty} \left[\sum_{k=1}^{\infty} \frac{2n[1-(-1)^n](-1)^k A_{PYk}}{\pi[n^2-9k^2]} \sin(\frac{n\pi}{3})\cos(n\omega t) \right] \end{aligned} \tag{2.39}$$

If the last two parts in Equation 2.39 cancel each other, i.e.

$$\sum_{k=1}^{\infty} \frac{(-1)^k A_{PYk}}{(6l \pm 1)^2 - 9k^2} = \frac{I_{dc}}{(6l \pm 1)^2} \qquad (l = 1, 2, \cdots) \tag{2.40}$$

the primary winding current $I_{\Delta A}(\omega t)$ only includes the triple harmonics of orders $n = 3(2j-1)$ $(j = 1, 2, \cdots)$. Because the triple harmonics in balanced three phase system are all in phase, the output current, $I_{\Delta A}(\omega t)$, i.e. the primary side line currents of the interface transformer are pure sinusoidal fundamental waveforms. Equation 2.40 is the harmonic cancellation condition for 6-pulse reinjection CSC.

2.2.4 Harmonic Cancellation for 6-pulse VSC

The 6-pulse reinjection VSC configuration, shown in Figure 2.4, consists of an extra 3-phase bidirection controllable half bridge, a three phase full bridge and an interface transformer which is connected in Y/Y. The extra three phase half bridge is added to short circuit the secondary windings to provide zero voltage across the secondary windings while both arms in a phase leg are in off-state. The secondary windings of the interface transformer are connected in Y to provide a common terminal for the application of the reinjection voltage across the three windings simultaneously. The primary windings are also connected in Y to produce line voltages which are the sum of two winding voltages and thus cancel the harmonics in the phase winding voltages. The three phase full bridges can be treated as two half bridges which control the dc voltage applied to the secondary windings in the forward and reverse directions, i.e. the controllable power switches in these two half bridges forces the secondary windings to be connected to either terminals of the dc side voltage sources ($V_{BPY}(\omega t)$

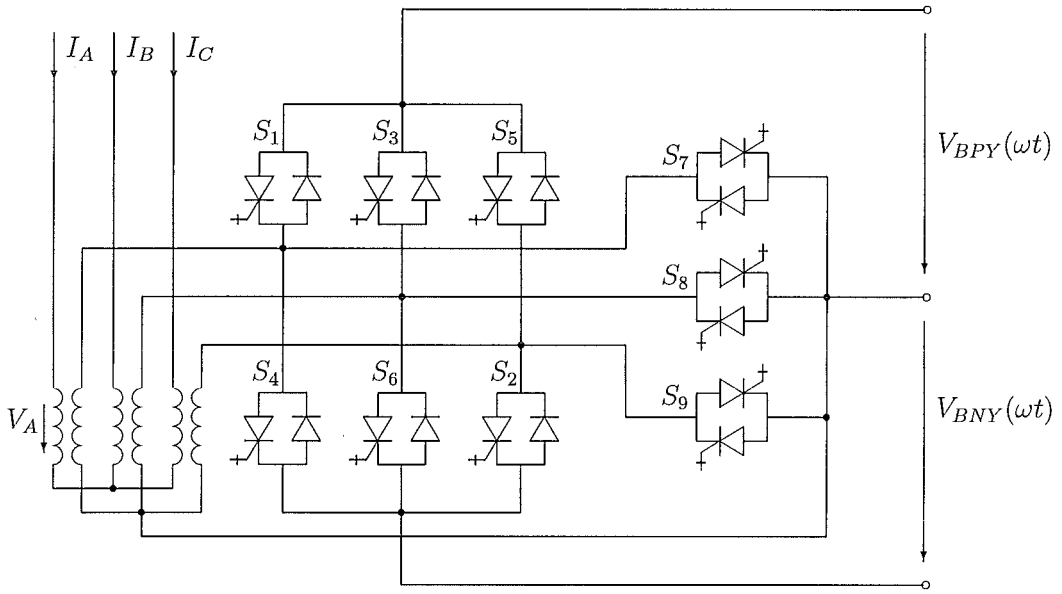


Figure 2.4 The 6-pulse VSC configuration

and $V_{BNY}(\omega t)$). When the two controllable switches in one leg are in off-state, the free wheeling diodes will provide the current path for the winding current; however when the winding current is zero, the winding will be in the open-circuiting state. When the windings are connected by the free wheeling diodes, there are two possible free wheeling paths and the open-circuiting state for the secondary windings will cause uncertainty in the winding voltage. To eliminate this uncertainty the power switches in the extra half bridge are used to short-circuit the secondary windings to force the voltages across the windings to be zero.

The dc side voltage sources denoted $V_{BPY}(\omega t)$ and $V_{BNY}(\omega t)$ are controllable voltage sources. The 120^o pattern is used to fire the power switches in the two half bridges, whereas the 60^o pattern is used to fire the bidirectional GTO pairs in the extra half bridge.

If the switch arm S_1 is switched to on-state at

$$\omega t = \cdots, -\pi/3,\ 5\pi/3,\ 11\pi/3,\ \cdots$$

and to off-state at

$$\omega t = \cdots,\ \pi/3,\ 7\pi/3,\ 13\pi/3,\ \cdots;$$

the switch arm S_4 is switched to on-state at

$$\omega t = \cdots,\ 2\pi/3,\ 8\pi/3,\ 14\pi/3,\ \cdots$$

and to off-state at *5pt

$$\omega t = \cdots,\ 4\pi/3,\ 10\pi/3,\ 16\pi/3,\ \cdots;$$

the bidirectional GTO pair S_7 is switched to on-state at

$$\omega t = \cdots,\ -2\pi/3,\ \pi/3,\ 4\pi/3,\ 7\pi/3,\ \cdots$$

and to off-state at

$$\omega t = \cdots,\ -\pi/3,\ 2\pi/3,\ 5\pi/3,\ 8\pi/3,\ \cdots;$$

V_{Pa} and V_{Na}, the forward and reverse voltages across the secondary winding phase 'a' of the interface transformer, are given by

$$V_{Pa}(\omega t) = \begin{cases} 0 & -4\pi/3 < \omega t < -\pi/3 \\ V_{BPY}(\omega t) & -\pi/3 < \omega t < \pi/3 \\ 0 & \pi/3 < \omega t < 5\pi/3 \end{cases} \tag{2.41}$$

$$V_{Na}(\omega t) = \begin{cases} 0 & -2\pi/3 < \omega t < 2\pi/3 \\ -V_{BNY}(\omega t) & 2\pi/3 < \omega t < 4\pi/3 \\ 0 & 4\pi/3 < \omega t < 8\pi/3 \end{cases} \tag{2.42}$$

By comparing Equations 2.41 and 2.42 with Equations 2.23 and 2.24, based on the duality between VSC and CSC, the analysis results for the 6-pulse reinjection CSC can be extended to the 6-pulses reinjection VSC. Therefore if the voltage applied to the two half bridge converters are

$$V_{BPY}(\omega t) = V_{dc} + \sum_{k=1}^{\infty} A_{PYk} \cos(3k\omega t) \tag{2.43}$$

and

$$V_{BNY}(\omega t) = V_{dc} + \sum_{k=1}^{\infty} A_{NYk} \cos(3k\omega t) \tag{2.44}$$

the primary winding voltage V_A only includes triple harmonics of orders $n = 3(2j - 1)$ $(j = 1, 2, \cdots)$. Thus for the balanced 3-phase system the output voltages, $V_{AB} = V_A - V_B$, $V_{BC} = V_B - V_C$, $V_{CA} = V_C - V_A$, i.e. the line voltages are harmonic free waveforms. To achieve these results the harmonic cancellation condition is also

$$\sum_{k=1}^{\infty} \frac{(-1)^k A_{PYk}}{(6l \pm 1)^2 - 9k^2} = \frac{V_{dc}}{(6l \pm 1)^2} \qquad (l = 1, 2, \cdots) \tag{2.45}$$

2.3 REINJECTION WAVEFORMS FOR 12-PULSE SYSTEM

2.3.1 Ideal Reinjection for 12-Pulse System

Based on the analysis of the previous section, the harmonic cancellation condition of the 12-pulse reinjection conversion system is in the same form for VSC and CSC, thus by using M_{dc} as the dc source level instead of V_{dc} and I_{dc} it can be written as

$$\sum_{k=1}^{\infty} \frac{A_{Yk}/M_{dc}}{(12l \pm 1)^2 - 36k^2} = \frac{1}{(12l \pm 1)^2} \qquad l = 1, 2, \cdots \tag{2.46}$$

which constitute a set of linear algebraic equations [i.e. an infinite number of equations $(l = 1, 2, \cdots)$] for determining infinite variables $(A_k = A_{Yk}/M_{dc} \quad k = 1, 2, \cdots)$.

In practice the very high order harmonics are negligible and thus the number of equations can be reduced. If the harmonics in the output waveform of orders higher than $(12m+1)$ are ignored, the equation number is reduced to $2m$. With these $2m$ equations, the $2m$ or less variables $(A_k, \quad k = 1, 2, \cdots, n \leq 2m)$ can be determined.

The numerical solutions of A_k, $k = 1, 2, \cdots, n \leq 2m$ for a sufficiently large value of the number m can be approximately expressed by the explicit formulas below.

$$A_k = \frac{A_{Yk}}{M_{dc}} = \frac{2[2(-1)^k - \sqrt{3}]}{(2 - \sqrt{3})(36k^2 - 1)} \approx \frac{14.9282(-1)^k - 12.9282}{36k^2 - 1} \quad k = 1, 2, \cdots \tag{2.47}$$

and

$$\frac{A_{\Delta k}}{M_{dc}} = (-1)^k \frac{A_{Yk}}{M_{dc}} \approx \frac{14.9282 - 12.9282(-1)^k}{36k^2 - 1} \qquad k = 1, 2, \cdots \tag{2.48}$$

Based on the numerical results of A_k, the normalized reinjection voltage or current waveforms, $\mathbf{X}_Y(x) = 1 + \sum_{k=1}^{\infty} A_k \cos(6kx)$ and $\mathbf{X}_\Delta(x) = 1 + \sum_{k=1}^{\infty} (-1)^k A_k \cos(6kx)$ applied or supplied to the Y-connection and Δ-connection bridges are shown in Figures 2.5 (a) and (b) respectively.

The two waveforms possess the following important characteristics:

1. Zero values appear at the points where the switches in the bridge are turned on and off;

2. The derivatives of the waveforms are limited, particularly around the zero values where the power switches change their states;

3. The two waveforms add to a dc level with very low amplitude ripple as shown in Figure 2.5(c).

The first characteristic indicates the possibility of achieving ZVS (zero voltage switching) or ZCS (zero current switching). The second ensures operation at low dV/dt

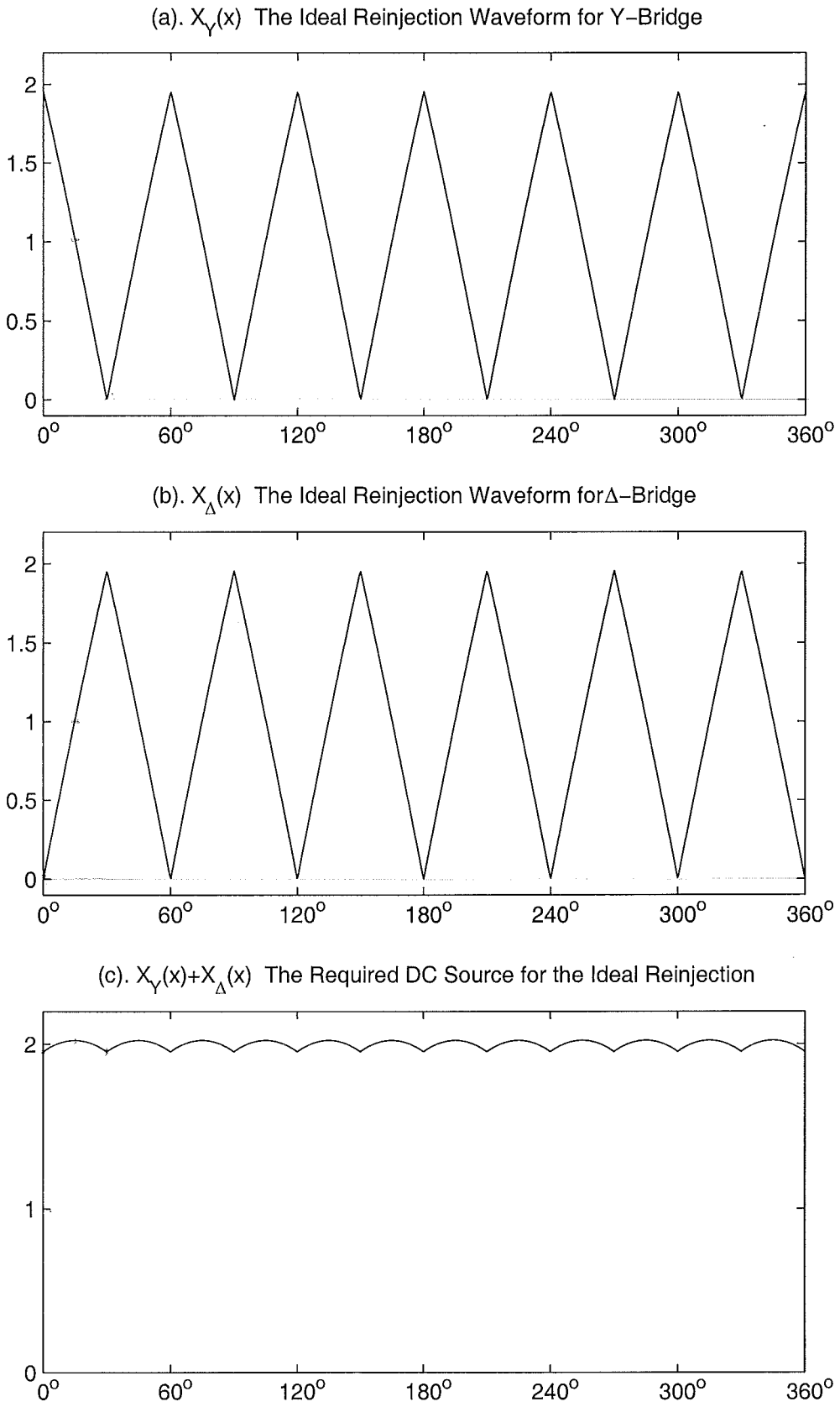


Figure 2.5 The Ideal Reinjection Waveforms

or dI/dt conditions. The third implies that the two bridges must be supplied by a dc source with a specified controllable ripple. However in practice it is difficult to generate such ripple and thus further simplification is needed.

Assuming that the ideal reinjection waveforms can be supplied to the two bridges, the voltage waveforms of the 12-pulse Voltage Reinjection converter are shown in Figure 2.6, where

- (a) V_{YY}/V_{dc}, Voltage ratio between the voltage across the Y/Y connection bridge, V_{YY}, and its mean voltage V_{dc};
- (b) $V_{Y\Delta}/V_{dc}$, Voltage ratio between the voltage across the Y/Δ connection bridge, $V_{Y\Delta}$, and its mean voltage V_{dc};
- (c) V_{Ya}/V_{dc}, Voltage ratio between the ac output voltage of the Y/Y connection bridge, V_{Ya}, and its dc side mean voltage V_{dc};
- (d) $V_{\Delta a}/V_{dc}$, Voltage ratio between the ac output voltage of the Y/Δ connection bridge, V_{Ya}, and its dc side mean voltage V_{dc};
- (e) $V_A/[k_n V_{dc}]$, Voltage ratio between the ac output voltage of the MLVR system V_A, and the normalized voltage $k_n V_{dc}$ (k_n is the turns ratio of the interface transformer);
- (f) The spectrum of the output voltage V_A.

The Waveforms in Figure 2.6 show that the two bridge ac output waveforms contain harmonics, but the converter system ac output waveform is pure sinusoidal due to the harmonic cancellation of the two bridge output waveforms.

The current waveforms of the Current Reinjection converter can be directly obtained from Figure 2.6 by the duality between the VSC and CSC.

2.3.2 Symmetrical Reinjection for 12-pulse System

To overcome the difficulty of providing a ripple controllable dc power source the reinjection waveform has to be fully symmetrical. The reinjection waveforms in Figures 2.5 (a) and (b) are symmetrical about the vertical axis, but not about any one of the cross points of the waveform with its dc average. Therefore the sum of the reinjection waveforms to the Y and to the Δ connection bridges is not a constant dc. The use of fully symmetrical waveforms with minimum errors with respect to the ideal reinjection waveforms will simplify the requirement applied to the dc supply without causing significant harmonic distortion at the converter ac output.

Based on the conditions of minimizing the harmonic distortion and simplifying the practical implementation, the following two types of waveforms are derived.

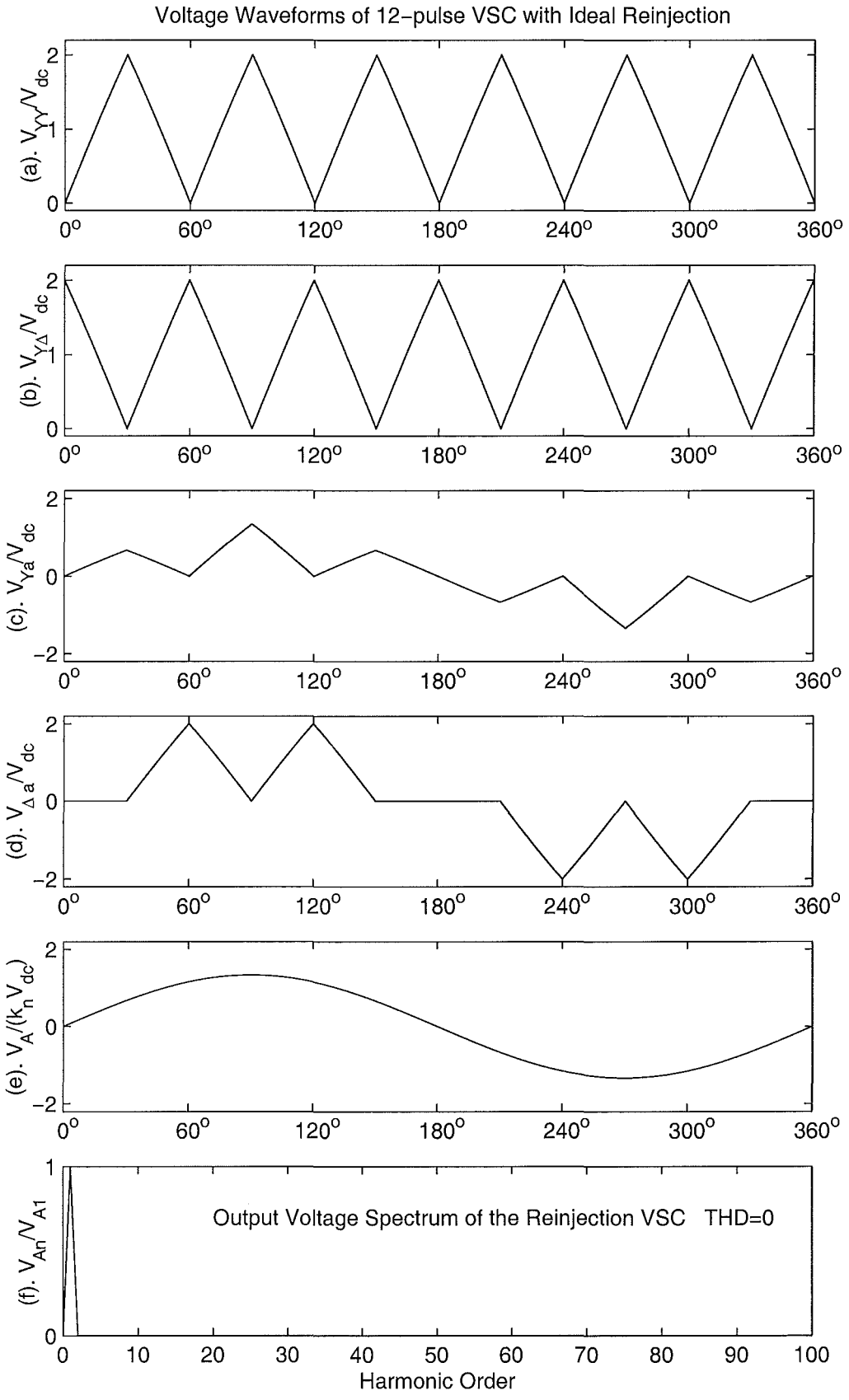


Figure 2.6 The Voltage Waveforms of 12-pulse VSC with Ideal Reinjection

- A waveform that minimizes the integration of the error square and the error derivative square (ESEDS), is the optimal approximation of the ideal reinjection waveform under the symmetry restriction.
- A linearly raising and linearly falling waveform, which provides constant derivative and linear voltage or current increment and decrement, is the simplest for practical implementation.

The ESEDS symmetrical waveform, $\mathbf{X}_{Ys}(x)$, is obtained by solving the minimization:

$$min\left\{\int_0^{\pi/6}\left[[\mathbf{X}_Y(x)-\mathbf{X}_{Ys}(x)]^2+\left(\frac{d[\mathbf{X}_Y(x)-\mathbf{X}_{Ys}(x)]}{dx}\right)^2\right]dx + \int_0^{\pi/6}\left[[\mathbf{X}_\Delta(x)-\mathbf{X}_{\Delta s}(x)]^2+\left(\frac{d[\mathbf{X}_\Delta(x)-\mathbf{X}_{\Delta s}(x)]}{dx}\right)^2\right]dx\right\}$$

under the conditions of symmetry and area equality between the two groups of curves, i.e.

$$\mathbf{X}_{Ys}(x)+\mathbf{X}_{\Delta s}(x)=2 \qquad for \quad 0<x<\pi/6\ ;$$

$$and \quad \int_0^{\pi/12}\mathbf{X}_{Ys}(x)dx=\int_0^{\pi/12}\mathbf{X}_Y(x)dx, \qquad \int_{\pi/12}^{\pi/6}\mathbf{X}_{Ys}(x)dx=\int_{\pi/12}^{\pi/6}\mathbf{X}_Y(x)dx,$$

$$\int_0^{\pi/12}\mathbf{X}_{\Delta s}(x)dx=\int_0^{\pi/12}\mathbf{X}_\Delta(x)dx, \qquad \int_{\pi/12}^{\pi/6}\mathbf{X}_{\Delta s}(x)dx=\int_{\pi/12}^{\pi/6}\mathbf{X}_\Delta(x)dx$$

Based on the numerical results of the symmetrical waveforms, $\mathbf{X}_{Ys}$ and $\mathbf{X}_{\Delta s}$ the Fourier components of the ESEDS symmetrical waveform $\mathbf{X}_{Ys}(x)$ is approximately given by an explicit formula

$$A_{ESEDSk}=\frac{(7+4\sqrt{3})[1-(-1)^k]}{(36k^2-1)}\approx\frac{13.9282[1-(-1)^k]}{36k^2-1} \qquad k=1,2,\cdots \tag{2.49}$$

Waveform $\mathbf{X}_{Ys}(x)$ is shown in Figure 2.7(a) and waveform $\mathbf{X}_{\Delta s}$ can be obtained by the application of the 30^o phase displacement between them.

The linear symmetrical waveform is shown in 2.7(b), its spectrum given by

$$A_{LINk}=\frac{4[1-(-1)^k]}{k^2\pi^2}\approx\frac{0.4053[1-(-1)^k]}{k^2} \qquad k=1,2,\cdots \tag{2.50}$$

It is clear that the ESEDS symmetrical waveform is very close to the linearly rising and linearly falling waveform.

Figure 2.7(c) shows that the difference between the ESEDS symmetrical waveform $\mathbf{X}_{Ys}(x)$ and the linear symmetrical waveforms is very small, the maximum absolute

value being below 0.025. Therefore the simple and easy to implement linear symmetrical waveform, is a favourable approximation for the reinjection conversion.

The ESEDS and Linear Symmetrical Reinjection waveforms shown in Figure 2.7 (a) and (b) not only possess the advanced characteristics of the ideal reinjection waveforms (limited rising and falling derivative and starting from and stopping at zero values) but also can be supplied by a constant dc power source. The cost of the approximation is a slight harmonic distortion at the converter ac output terminals. The harmonic spectrum and the THD (total harmonic distortion) for the ESEDS symmetrical reinjection waveforms are given by the following expressions.

$$\frac{V_{Asym-n}}{V_{Asym-1}} = \frac{\frac{1}{12k\pm1} - \frac{\pi(2+\sqrt{3})}{12(12k\pm2)}}{1+\frac{\pi(\pi-3)(2+\sqrt{3})}{72}} \approx \frac{0.9774625}{12k\pm1} - \frac{0.95502838}{12k\pm2} \quad n = 12k\pm1, \quad k = 1,2,\cdots \tag{2.51}$$

$$THD_{VAsym} = \sqrt{\frac{2(2+\sqrt{3})\pi^2}{72+\pi(\pi-3)(2+\sqrt{3})} - 1} \approx 1.0167787\% \tag{2.52}$$

When the ESEDS symmetrical reinjection waveforms are supplied to the two bridges, the 12-pulse MLVR converter voltage waveforms are shown in Figure 2.8, where

- (a) V_{YY}/V_{dc}, Voltage ratio between the voltage across the Y/Y connection bridge, V_{YY}, and its mean voltage V_{dc};
- (b) $V_{Y\Delta}/V_{dc}$, Voltage ratio between the voltage across the Y/Δ connection bridge, $V_{Y\Delta}$, and its mean voltage V_{dc};
- (c) V_{Ya}/V_{dc}, Voltage ratio between the ac output voltage of the Y/Y connection bridge, V_{Ya}, and its dc side mean voltage V_{dc};
- (d) $V_{\Delta a}/V_{dc}$, Voltage ratio between the ac output voltage of the Y/Δ connection bridge, V_{Ya}, and its dc side mean voltage V_{dc};
- (e) $V_A/[k_nV_{dc}]$, Voltage ratio between the ac output voltage of the MLVR system V_A, and the normalized voltage k_nV_{dc} (k_n is the turns ratio of the interface transformer);
- (f) The spectrum of the output voltage V_A.

The harmonic spectrum and the THD (total harmonic distortions) for the linear symmetrical reinjection waveforms are given by the following expressions.

$$\frac{V_{Alin-n}}{V_{Alin-1}} = \frac{1}{n^2} \qquad n = 12k\pm1, \qquad k = 1,2,\cdots \tag{2.53}$$

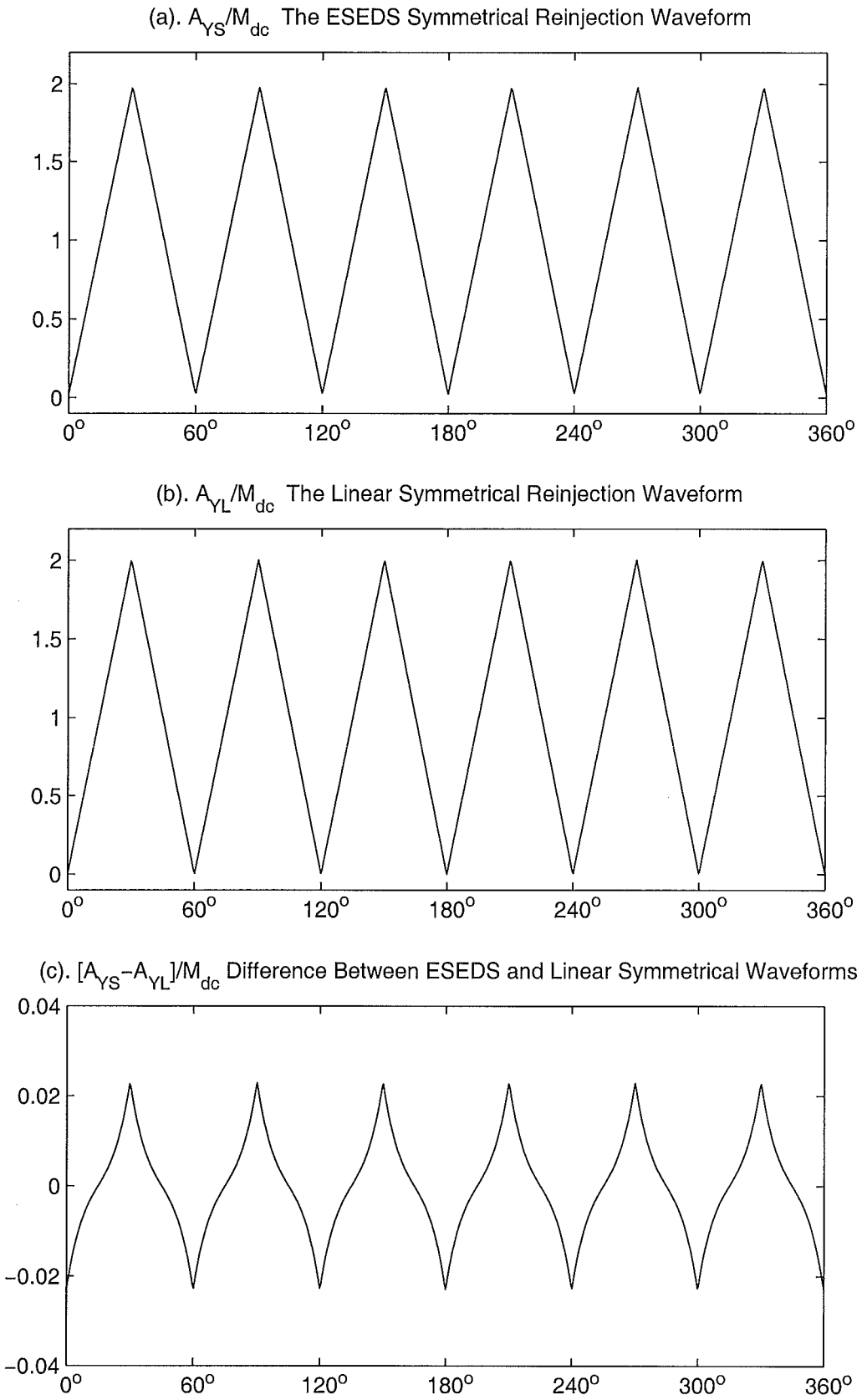


Figure 2.7 The ESEDS and Linear Symmetrical Reinjection Waveforms

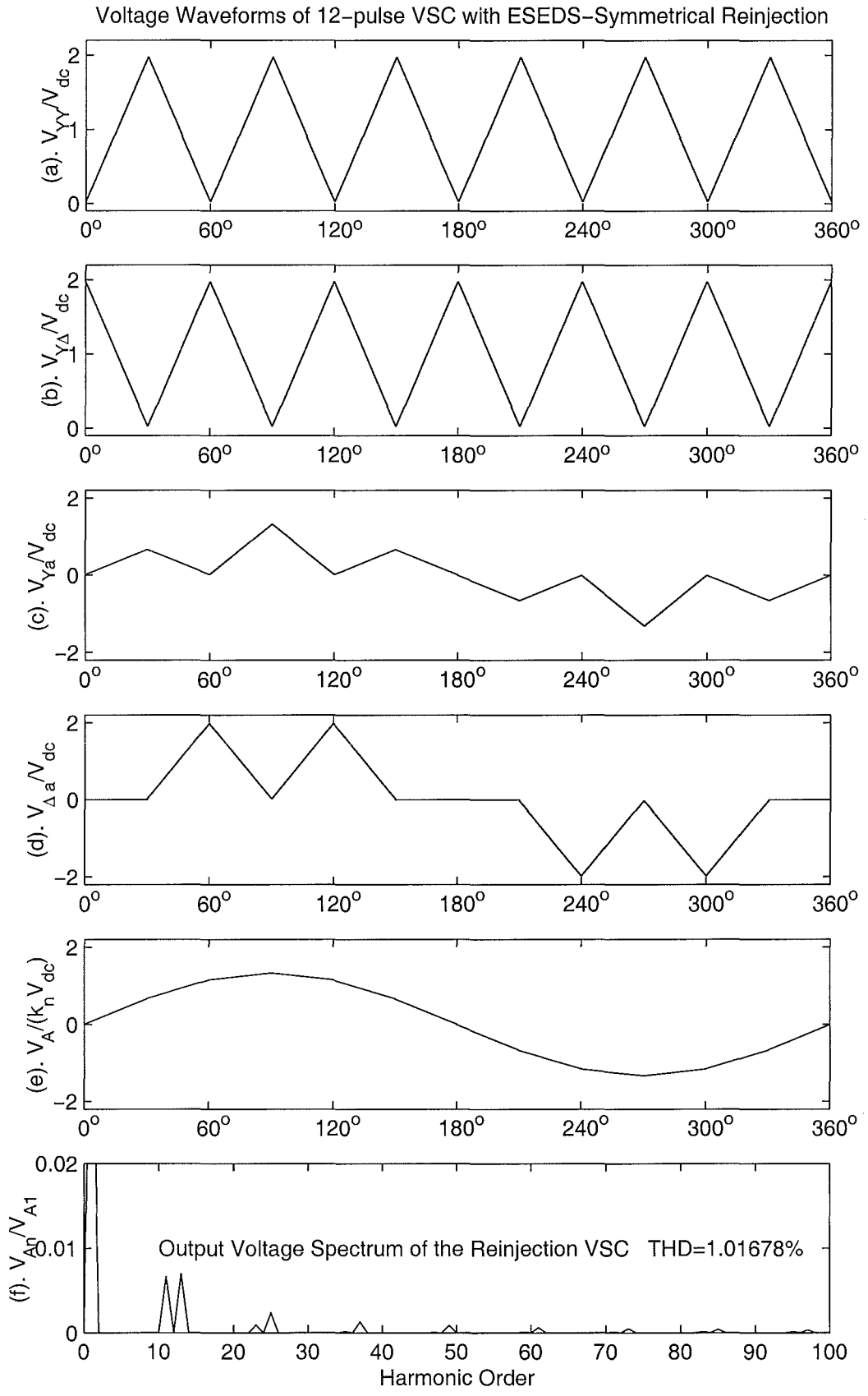


Figure 2.8 Voltage Waveforms 12-pulse VSC with ESEDS Reinjection

$$THD_{VAlin} = \sqrt{\sum_{k=1}^{\infty} \frac{1}{(12k-1)^4} + \sum_{k=1}^{\infty} \frac{1}{(12k+1)^4}}$$
$$= \sqrt{\frac{\pi^4(40+23\sqrt{3})}{8 \times 12 \times 81} - 1} \approx 1.05532\% \tag{2.54}$$

When the linear symmetrical reinjection waveforms are supplied to the two bridges, the 12-pulse MLVR converter voltage waveforms are shown in Figure 2.9, where

- (a) V_{YY}/V_{dc}, Voltage ratio between the voltage across the Y/Y connection bridge, V_{YY}, and its mean voltage V_{dc};
- (b) $V_{Y\Delta}/V_{dc}$, Voltage ratio between the voltage across the Y/Δ connection bridge, $V_{Y\Delta}$, and its mean voltage V_{dc};
- (c) V_{Ya}/V_{dc}, Voltage ratio between the ac output voltage of the Y/Y connection bridge, V_{Ya}, and its dc side mean voltage V_{dc};
- (d) $V_{\Delta a}/V_{dc}$, Voltage ratio between the ac output voltage of the Y/Δ connection bridge, V_{Ya}, and its dc side mean voltage V_{dc};
- (e) $V_A/[k_n V_{dc}]$, Voltage ratio between the ac output voltage of the MLVR system V_A, and the normalized voltage $k_n V_{dc}$ (k_n is the turns ratio of the interface transformer);
- (f) The spectrum of the output voltage V_A.

2.3.3 Multi-Level Reinjection for 12-Pulse System

The multi-level conversion concept can be adopted to generate the required reinjection waveforms approximately. The generation of multi-level linear or ESEDS symmetrical reinjection waveforms to the two bridges can be obtained from a controllable voltage or current three terminal divider (two static and one movable), which is powered by a constant dc source. The two static terminals are connected to the two bridges respectively, while the movable terminal is connected to a common node of the two other terminals of the two bridges. This topological arrangement is based on the requirement of the symmetrical reinjection waveforms to the two bridges. The possible levels provided by the divider then can be supplied to the two bridges by controlling the movable terminal of the divider, while the sum of the voltages or currents supplied to the two bridges is always equal to the dc power source. If the zero voltage or current level supplied to the bridge occurs when there are power switches turning on and off, the soft switching condition is achieved. Thus the reinjection, multi-level and soft switching concepts are combined together to form a high performance conversion system suitable for high power and high voltage applications.

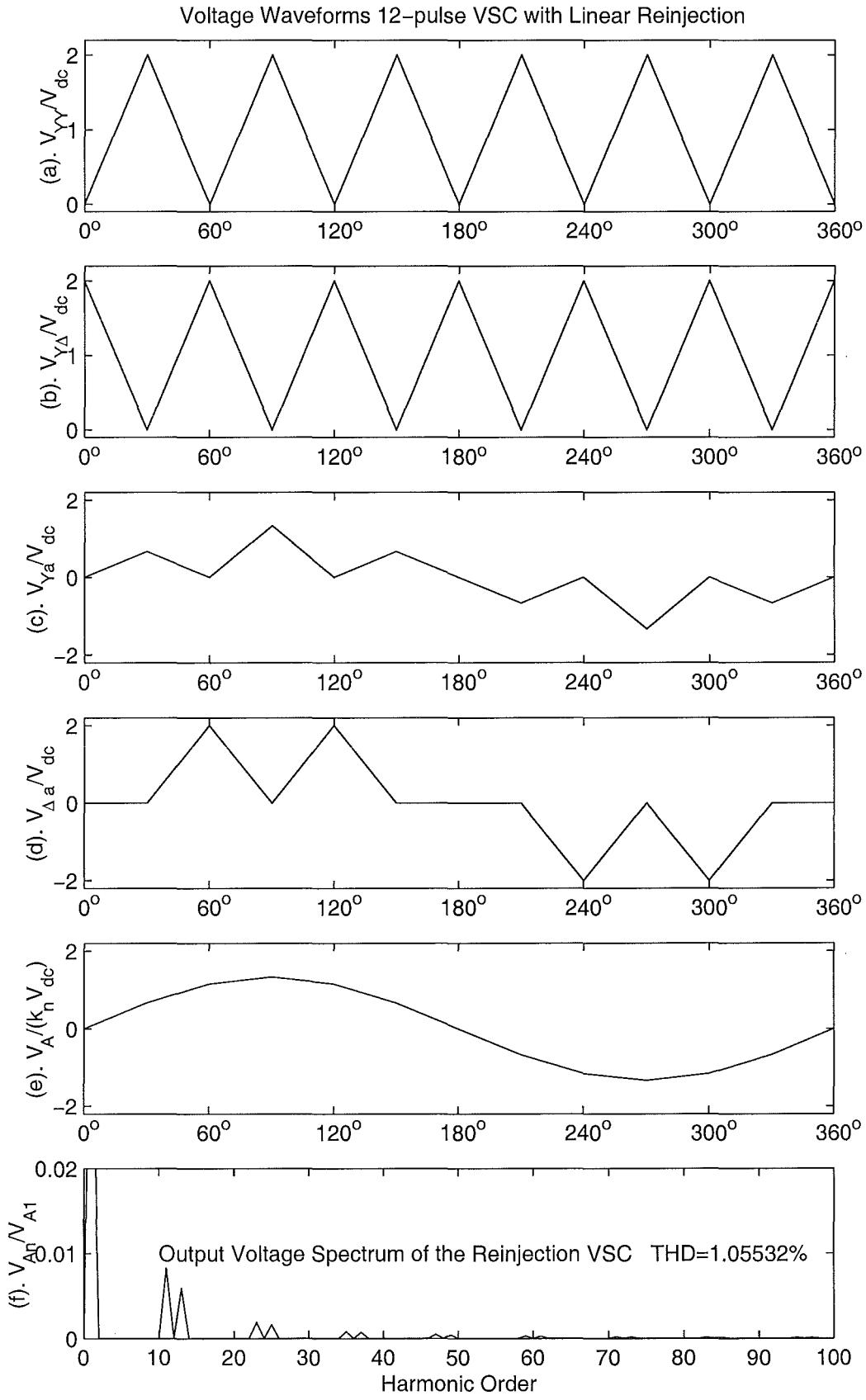


Figure 2.9 Voltage Waveforms of 12-pulse VSC with Linear Reinjection

The multi-level symmetrical reinjection waveforms generated by ideal switches and an ideal dc power source are step waveforms. The width and height of every step in the multi-level symmetrical step reinjection waveforms can be decided based on the following considerations:

a. simplicity of implemention, i.e. equal level width and equal increment;
b. minimum harmonic distortion caused by the multi-level approximation;
c. sufficient zero width for the power valves to switch under zero voltage or current.

The ESEDS symmetrical waveforms shown in (a) and (b) of Figure 2.10 are divided into m equal length portions from 0 to $\pi/6$, the height of the corresponding step waveform being determined by the area equivalent principle, i.e. for any interval the corresponding area is the same for the step symmetrical waveform and the ESEDS symmetrical waveform. These step waveforms are supplied to the two main bridges to generate an ac output waveform with minimum THD under the symmetrical restriction. Although the zero voltage switching is not provided, as the level number m increases, the level height decreases and the power valves switch under very low voltage or current stress. If the m heights are denoted by H_{Si} $i = 1, 2, \cdots, m$, from 0 to $\pi/6$, they are given by

$$H_{Si} = 1 + 14.4195m \sin(\frac{\pi}{12m}) \sin\left[\frac{(2i-1)\pi}{12m} - \frac{\pi}{12}\right] \qquad i = 1, 2, \cdots, m \tag{2.55}$$

The linear symmetrical waveforms are converted to the symmetrical step waveform, shown in (a) and (b) of Figure 2.11, with m levels in the interval from $-\frac{\pi}{12(m-1)}$ to $\frac{\pi}{6} - \frac{\pi}{12(m-1)}$, almost in the same way. The only difference arises from the starting and stopping points of the zero level soft switching region, the $\pi/6$ radians interval being divided into $(m-1)$ sections of equal width. The first interval starts at $-\frac{\pi}{12(m-1)}$ and stops at $\frac{\pi}{12(m-1)}$, with zero level height; the second interval starts at $\frac{\pi}{12(m-1)}$ and stops at $\frac{3\pi}{12(m-1)}$, with level height $\frac{2}{m-1}$; $\cdots$; the i^{th} interval starts at $\frac{(2i-3)\pi}{12(m-1)}$ and stops at $\frac{(2i-1)\pi}{12(m-1)}$, with level height $\frac{2(i-1)}{m-1}$; $\cdots$; the m^{th} interval starts at $\frac{(2m-3)\pi}{12(m-1)}$ and stops at $\frac{(2m-1)\pi}{12(m-1)}$, with level height $\frac{2(m-1)}{m-1}$. The heights of the m levels are given by

$$H_{Li} = \frac{2(i-1)}{m-1} \qquad i = 1, 2, \cdots, m \tag{2.56}$$

The linearly increasing waveform with zero level switching simplifies the implementation by using the same type of components throughout the divider.

When the two bridges are supplied with the ESEDS symmetrical step-waveforms, the waveforms at their ac sides and the converter output terminals, are shown in Figures 2.10 (c), (d) and (e), and Figure 2.10 (f) shows the reinjection converter system output waveform spectrum.

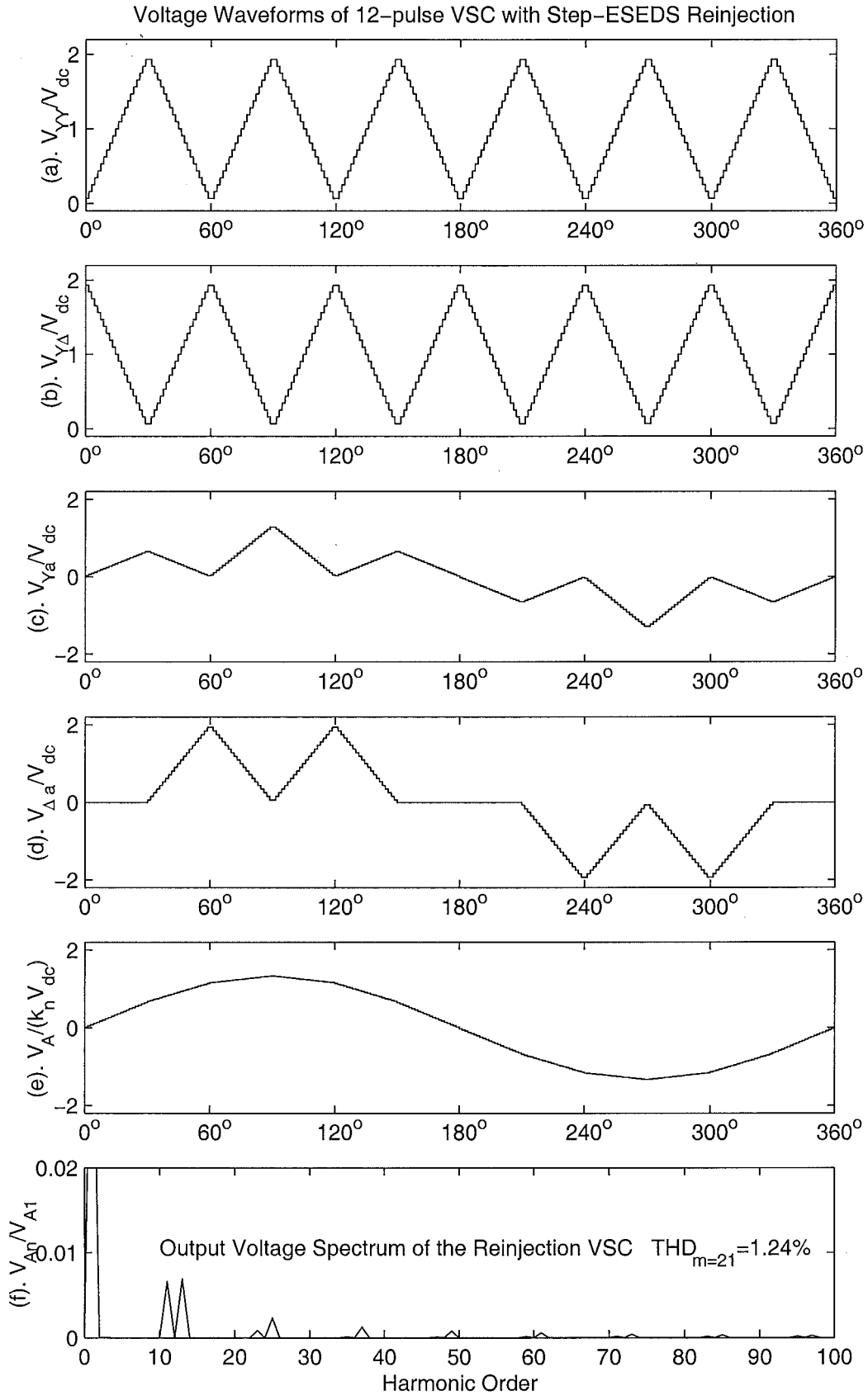


Figure 2.10 Voltage Waveforms of 12-pulse VSC with Step-ESEDS Reinjection

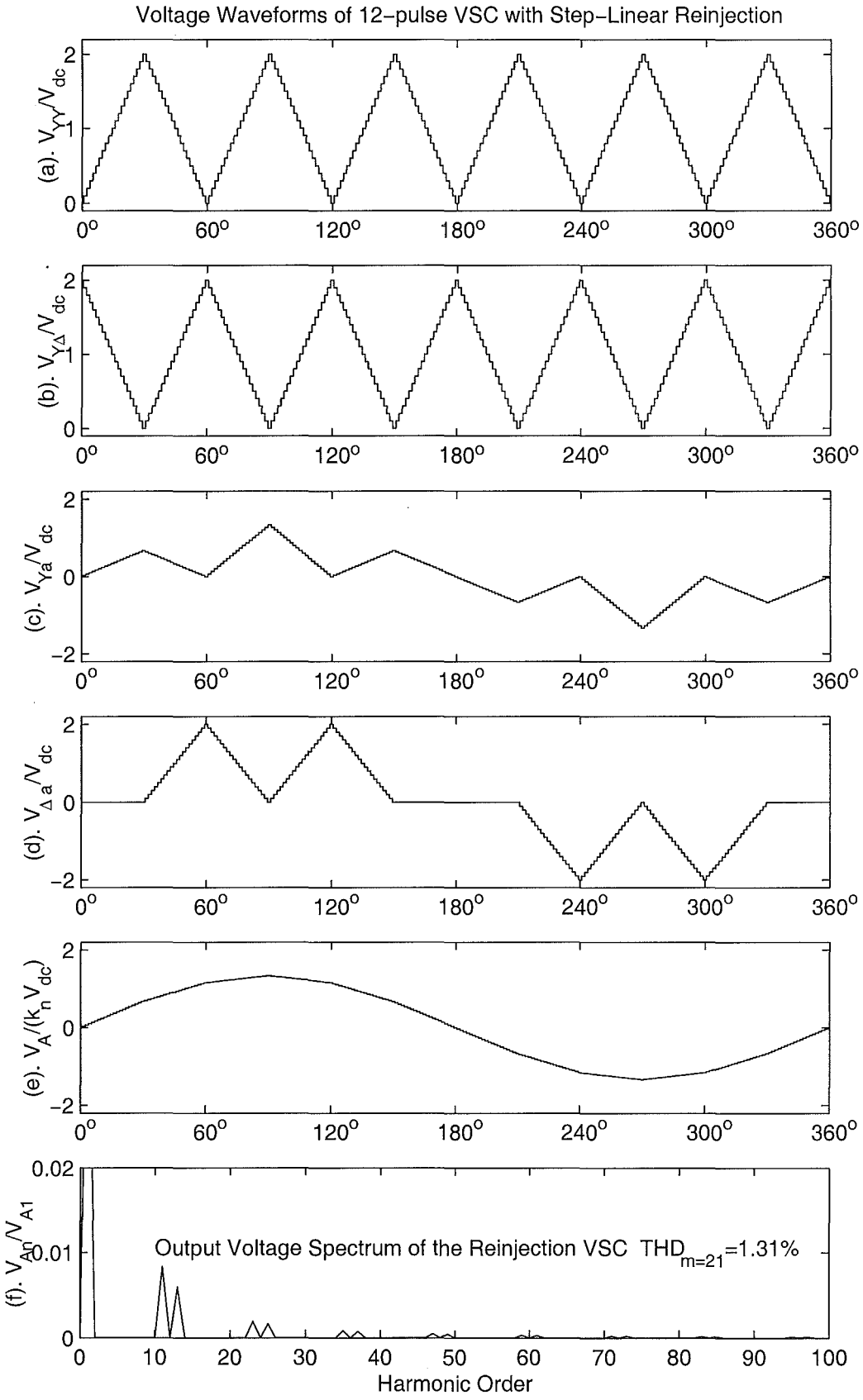


Figure 2.11 Voltage Waveforms of 12-pulse VSC with Step-Linear Reinjection

When the two bridges are supplied with the linear symmetrical step-waveforms, Figures 2.11 (c), (d) and (e) show the waveforms at their ac sides and the converter system output terminals, and Figure 2.11 (f) shows the reinjection converter system output waveform spectrum.

The voltage source converter with the two bridges supplied by the step multi-level reinjection voltage waveforms is referred here as the Multi-Level Voltage Reinjection converter (MLVR). Similarly the current source converter with the two bridges supplied by the step multi-level reinjection current waveforms is referred here as the Multi-Level Current Reinjection converter (MLCR).

It is obvious that an increase in the level number m results in a decrease in harmonic distortion of the multi-level reinjection converter system.

Under ESEDS symmetrical multi-level reinjection, the fundamental peak voltage, RMS voltage and total harmonic distortion of the MLVR converter output voltage are

Output Voltage Fundamental Peak Magnitude (ESEDS Symmetrical m-level)

$$V_{A1} = \frac{4}{\pi}\left[1 + 2(2+\sqrt{3})m^2 \sin^2(\frac{\pi}{12m}) - \frac{2+\sqrt{3}}{2} m \tan(\frac{\pi}{12m})\right] k_n V_{dc} \tag{2.57}$$

Output Voltage RMS Value (ESEDS Symmetrical m-level)

$$V_{ARMS} = \frac{\sqrt{3}+1}{3} k_n V_{dc} \sqrt{1 + 2(2+\sqrt{3})m^2 \sin^2(\frac{\pi}{12m}) - \frac{2+\sqrt{3}}{2} m \tan(\frac{\pi}{12m})} \tag{2.58}$$

Output Voltage THD (ESEDS Symmetrical m-level)

$$\begin{aligned} THD_{VA} &= \sqrt{\frac{2V_{ARMS}^2}{V_{A1}^2} - 1} \\ &= \sqrt{\frac{(2+\sqrt{3})\pi^2}{36[1 + 2(2+\sqrt{3})m^2 \sin^2(\frac{\pi}{12m}) - \frac{2+\sqrt{3}}{2} m \tan(\frac{\pi}{12m})]} - 1} \end{aligned} \tag{2.59}$$

Under linear symmetrical multi-level reinjection, the fundamental peak voltage, RMS voltage and total harmonic distortion of the MLVR converter output voltage are

Output Voltage Fundamental Peak Magnitude (Linear Symmetrical m-level)

$$V_{A1} = \frac{32}{\pi(m-1)} \sin\left(\frac{\pi}{12(m-1)}\right)\left[\frac{m-1}{2} + \sum_{j=1}^{m-2} j \cos(\frac{\pi}{6} - \frac{j\pi}{6(m-1)})\right] k_n V_{dc} \tag{2.60}$$

Output Voltage RMS Value (Linear Symmetrical m-level)

$$V_{ARMS} = \frac{2k_n V_{dc}}{3}\sqrt{\frac{(4+\sqrt{3})}{3} + \frac{(2-\sqrt{3})}{3(m-1)^2}} \tag{2.61}$$

Output Voltage THD (Linear Symmetrical m-level)

$$THD_{VA} = \sqrt{\frac{2V_{ARMS}^2}{V_{A1}^2} - 1}$$

$$= \sqrt{\frac{\pi^2[(4+\sqrt{3})(m-1)^2 + (2-\sqrt{3})]}{27 \times 128 \sin^2(\frac{\pi}{12(m-1)})\left[\frac{m-1}{2} + \sum_{j=1}^{m-2} j\cos(\frac{\pi}{6} - \frac{j\pi}{6(m-1)})\right]^2} - 1} \tag{2.62}$$

Table 2.1 shows the relationship between the level number m and the total harmonic distortion under the ESEDS and linear symmetrical multi-level reinjection conditions. The harmonic content reduction slows down when the level number m is greater than 8, and therefore there is no need of very high level numbers for harmonic suppression. Taking into account the duality between the VSC and CSC the total harmonic distortion for MLCR under the ESEDS and linear symmetrical multi-level reinjection can be directly obtained from the MLVR results.

Table 2.1 THD_{12} of the ESEDS and linear multi-level reinjection

Level m	3	4	5	6	7	8	9	10
THD_{sym}	5.09%	3.88%	3.16%	2.69%	2.36%	2.13%	1.95%	1.81%
THD_{lin}	7.77%	5.25%	3.99%	3.28%	2.77%	2.45%	2.20%	2.02%

2.4 REINJECTION WAVEFORMS FOR 6-PULSE SYSTEM

2.4.1 Ideal Reinjection for 6-pulse System

The harmonic cancellation conditions of the 6-pulse reinjection conversion system is in the same form for VSC and CSC, thus by using M_{dc} as the dc source level instead of V_{dc} and I_{dc} it can be expressed in the form:

$$\sum_{k=1}^{\infty} \frac{(-1)^k A_{PYk}/M_{dc}}{(6l \pm 1)^2 - 9k^2} = \frac{1}{(6l \pm 1)^2} \qquad (l = 1,\ 2,\ \cdots) \tag{2.63}$$

which constitute a set of linear algebraical equations [i.e. an infinite number of equations $(l = 1,\ 2,\ \cdots)$] for determining the infinite variables [$B_k = A_{PYk}/M_{dc}$ (dc

component of the two half bridges) $k = 1,\ 2,\ \cdots\ ]$.

Similarly to the 12-pulse system, the conditions described by Equation 2.63 are solved and given approximately by the explicit formula

$$B_k = \frac{A_{PYk}}{M_{dc}} = \frac{-2[2-(-1)^k]}{(9k^2-1)} = \frac{2(-1)^k - 4}{9k^2-1} \qquad k = 1, 2, \cdots \tag{2.64}$$

Thus the reinjection waveforms for the two half bridges are given by

$$\begin{aligned} A_{BPY}(x) &= M_{dc} + \sum_{k=1}^{\infty} B_k M_{dc} \cos(3kx) \\ &= M_{dc} - \sum_{k=1}^{\infty} \frac{2[2-(-1)^k]}{(9k^2-1)} M_{dc} \cos(3kx) \qquad k = 1, 2, \cdots \end{aligned} \tag{2.65}$$

$$\begin{aligned} A_{BNY}(x) &= M_{dc} + \sum_{k=1}^{\infty} (-1)^k B_k M_{dc} \cos(3kx) \\ &= M_{dc} - \sum_{k=1}^{\infty} \frac{2[2(-1)^k - 1]}{(9k^2-1)} M_{dc} \cos(3kx) \qquad k = 1, 2, \cdots \end{aligned} \tag{2.66}$$

Based on the results of B_k, the normalized voltage or current waveform:

$$\mathbf{X}_P(x) = 1 + \sum_{k=1}^{\infty} B_k \cos(3kx)$$

$$\mathbf{X}_N(x) = 1 + \sum_{k=1}^{\infty} (-1)^k B_k \cos(3kx)$$

are applied or supplied to the two half bridges as shown in Figures 2.12 (a) and (b) respectively.

The two waveforms are like those of the 12-pulse conversion system except for the frequency of the reinjection waveform which for the 6-pulse system is three times the fundamental. The same important characteristics apply, i.e.

1. Zero values appear at the points where the switches in the two half bridges are turned on and off;

2. The derivative of the waveforms are limited, particularly around the zero values where the power switches change their states;

3. The two waveforms add to a dc level with low amplitude ripple, as shown in Figure 2.12 (c).

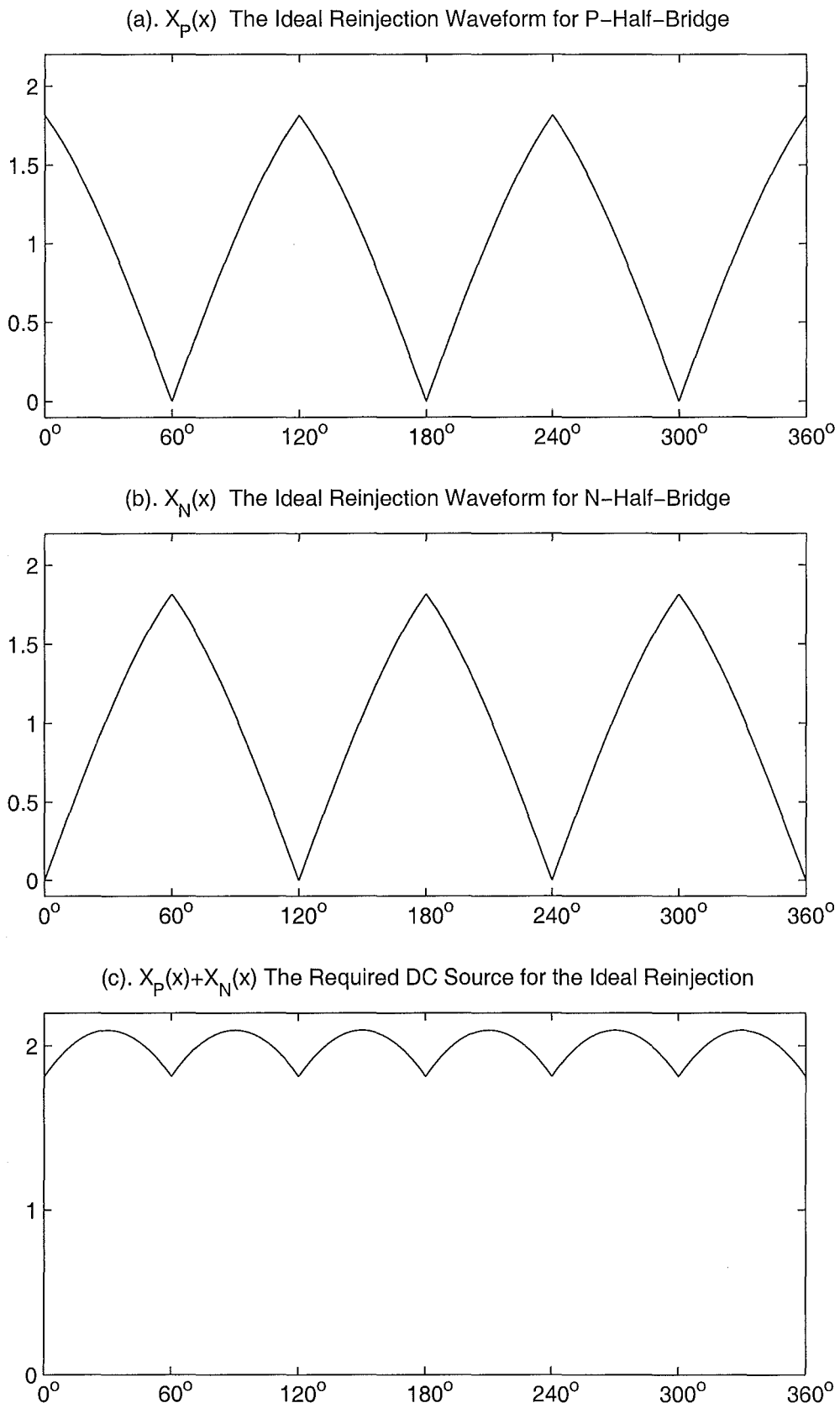


Figure 2.12 The Ideal Reinjection Waveforms for 6-Pulse System

These important characteristics can be employed to build up converters for high performance. Although these waveforms (the ideal reinjection waveforms) can produce a harmonic distortion free ac output waveform, the third characteristic restricts its practical application.

Under the operating condition that the ideal reinjection waveforms are supplied to the two half bridges, the 6-pulse MLCR converter system (refer to Figure 2.3) current waveforms are as shown in Figure 2.13, where

- (a) X_P, the normalized current of the reinjection current I_{BPY}, the base is its dc component;
- (b) X_N, the normalized current of the reinjection current I_{BNY}, the base is its dc component;
- (c) $I_{\Delta A}$, the normalized current of the interface primary phase 'A' winding current, the base is the dc component of the reinjection current I_{BPY};
- (d) $I_{\Delta B}$, the normalized current of the interface primary phase 'B' winding current, the base is the dc component of the reinjection current I_{BPY};
- (e) I_A, the normalized current of the interface primary line current, the base is the dc component of the reinjection current I_{BPY};
- (f) The spectrum of the output current I_A.

2.4.2 Symmetrical Reinjection for 6-pulse System

As explained in section 2.3.2 the reinjection waveforms supplied to the two half bridges in the 6-pulse conversion system ought to be fully symmetrical waveforms to overcome the difficulty of providing a ripple controllable dc power source.

To minimize the harmonic distortion caused by the symmetrical approximation of the ideal reinjection waveforms and to simplify the reinjection conversion configuration, the following two types of waveform are chosen.

- A waveform which minimizes the integration of the error square and the error derivative square (ESEDS), this provides the closest waveform to the ideal reinjection waveform under the symmetrical restriction.
- A linearly raising and linearly falling waveform, which provides constant derivative and linear voltage or current increment and decrement; this method greatly simplifies the practical implementation.

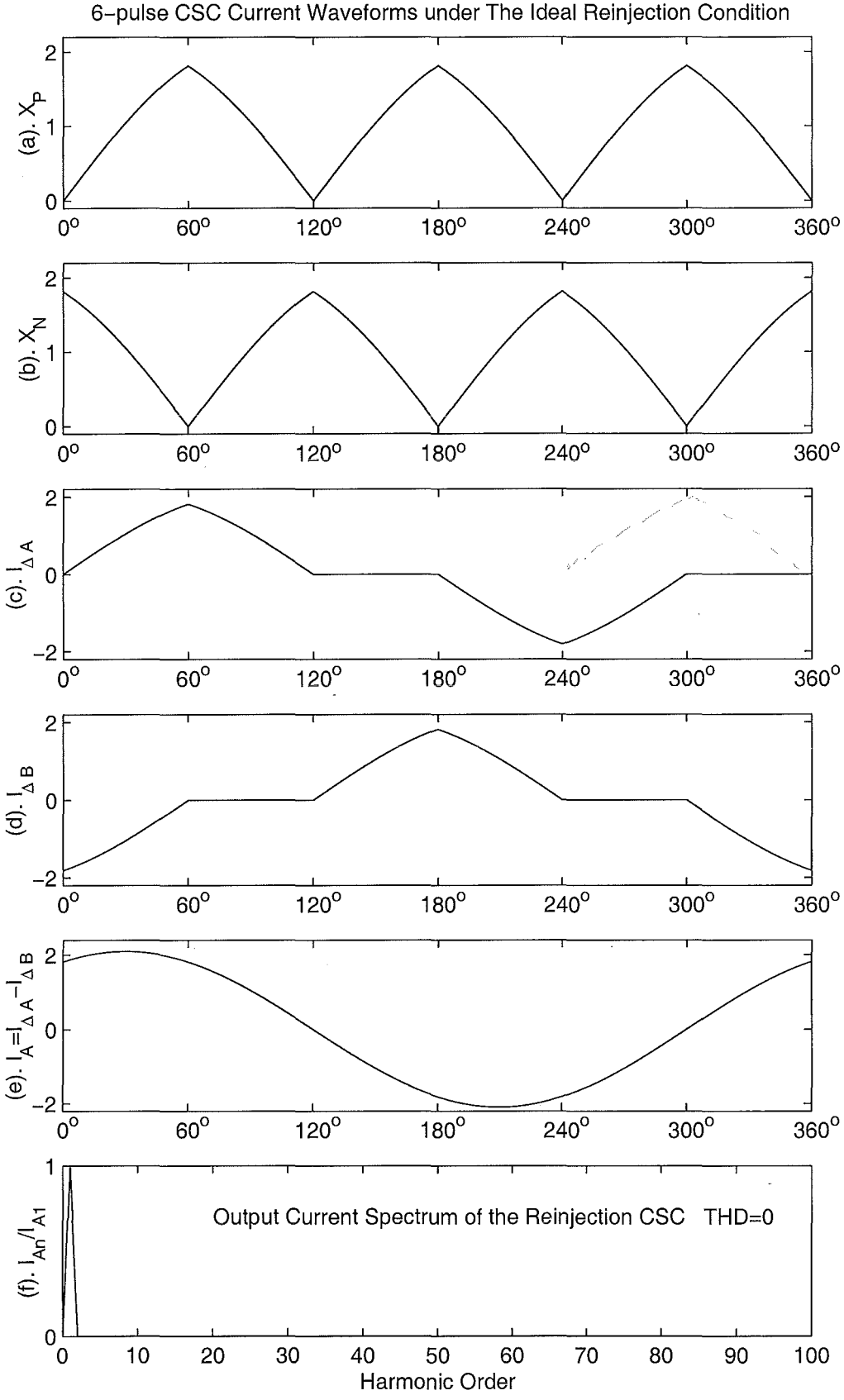


Figure 2.13 Current Waveforms of 6-pulse CSC with Ideal Reinjection

The ESEDS symmetrical waveform is obtained by solving the minimization:

$$min\left\{\int_0^{\pi/3}\left[[\mathbf{X}_P(x)-\mathbf{X}_{Ps}(x)]^2+\left(\frac{d[\mathbf{X}_P(x)-\mathbf{X}_{Ps}(x)]}{dx}\right)^2\right]dx + \int_0^{\pi/3}\left[(\mathbf{X}_N(x)-\mathbf{X}_{Ns}(x))^2+\left(\frac{d(\mathbf{X}_N(x)-\mathbf{X}_{Ns}(x))}{dx}\right)^2\right]dx\right\}$$

under the conditions of symmetrical restriction and area equality conditions between the two groups of curves, i.e.

$$\mathbf{X}_{Ps}(x)+\mathbf{X}_{Ns}(x)=2 \qquad for \quad 0<x<\pi/3\ ;$$

$$and \quad \int_0^{\pi/6}\mathbf{X}_{Ps}(x)dx=\int_0^{\pi/6}\mathbf{X}_P(x)dx, \qquad \int_{\pi/6}^{\pi/3}\mathbf{X}_{Ps}(x)dx=\int_{\pi/6}^{\pi/3}\mathbf{X}_P(x)dx,$$

$$\int_0^{\pi/6}\mathbf{X}_{Ns}(x)dx=\int_0^{\pi/6}\mathbf{X}_N(x)dx, \qquad \int_{\pi/6}^{\pi/3}\mathbf{X}_{Ns}(x)dx=\int_{\pi/6}^{\pi/3}\mathbf{X}_N(x)dx$$

Based on the numerical results of the symmetrical waveforms, $\mathbf{X}_{PS}$ and $\mathbf{X}_{NS}$, the Fourier components of the ESEDS symmetrical waveform $\mathbf{X}_{PS}(x)$ are approximately given by the explicit formula

$$B_{Sk}=\frac{-3[1-(-1)^k]}{(9k^2-1)} \qquad k=1,2,\cdots \tag{2.67}$$

Waveform $\mathbf{X}_{PS}(x)$ is shown in Figure 2.14(a) and waveform $\mathbf{X}_{NS}$ can be obtained by the application of the 60^o phase displacement between them.

The linear symmetrical waveform is shown in 2.14(b), its spectrum given by

$$B_{Lk}=\frac{4[1-(-1)^k]}{\pi^2k^2}\approx\frac{0.4053[1-(-1)^k]}{k^2} \qquad k=1,2,\cdots \tag{2.68}$$

It is clear that the ESEDS symmetrical waveform $\mathbf{X}_{PS}(x)$ is very close to the linearly rising and linearly falling waveform. Figure 2.14(c) shows that the difference between the ESEDS symmetrical and the linear symmetrical waveforms is within a narrow band, the maximum absolute value being below 0.1. Therefore the linear symmetrical waveform, which is simpler and easier to implement, is an appropriate approximation for the ideal reinjection.

The ESEDS and Linear Symmetrical Reinjection waveforms shown in Figure 2.14 (a) and (b) not only possess the advanced characteristics of the ideal reinjection waveforms (limited rising and falling derivative and starting from and stopping at zero values) but also can be supplied by a constant dc power source. The cost of the approximation is that some harmonic distortion appears at the converter ac output terminals

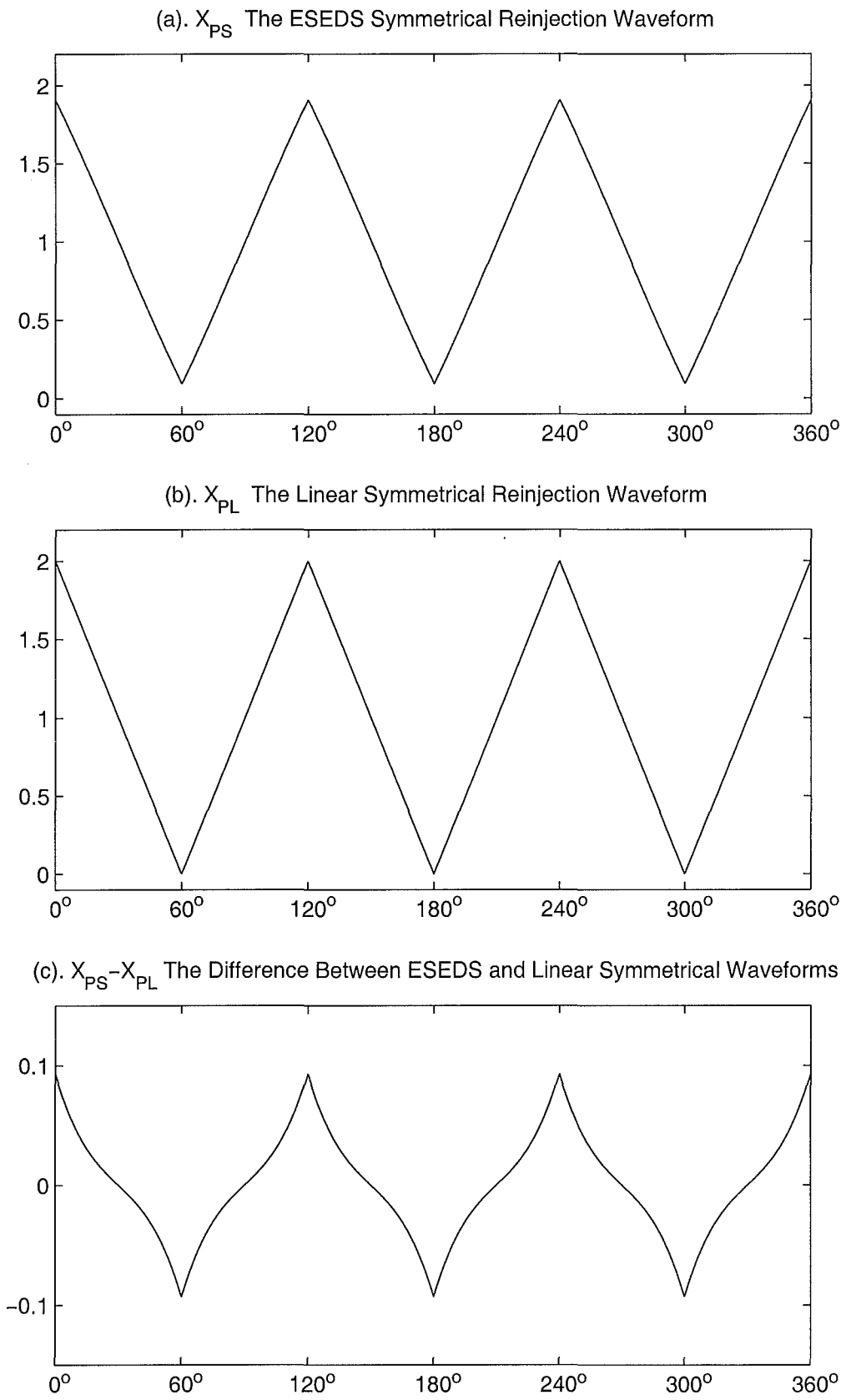


Figure 2.14 The ESEDS and Linear Reinjection Waveforms for 6-Pulse System

(THD=4.01% for the ESEDS Symmetrical Reinjection and THD=4.638% for the linear Symmetrical Reinjection). The harmonic spectrum and the THD (total harmonic distortion) for the ESEDS symmetrical reinjection waveforms are given by the following expressions.

$$\frac{B_{outS-n}}{B_{outS-1}} = \frac{n(1-\frac{\pi\sqrt{3}}{6})-\frac{1}{n}\pm\frac{\pi\sqrt{3}}{6}}{(n^2-1)(1+\frac{\pi^2}{18}-\frac{\pi\sqrt{3}}{12})} \qquad n=6k\pm1, \qquad k=1,2,\cdots \tag{2.69}$$

$$THD_{outS} = \sqrt{\frac{\pi^2}{9(1+\frac{\pi^2}{18}-\frac{\pi\sqrt{3}}{12})}-1} \approx 4.0107\% \tag{2.70}$$

When the ESEDS symmetrical reinjection waveforms are supplied to the two half bridges, the 6-pulse MLCR converter (refer to Figure 2.3) current waveforms are shown in Figure 2.15, where

- (a) X_P, the normalized current of the reinjection current I_{BPY}, the base is its dc component;
- (b) X_N, the normalized current of the reinjection current I_{BNY}, the base is its dc component;
- (c) $I_{\Delta A}$, the normalized current of the interface primary phase 'A' winding current, the base is the dc component of the reinjection current I_{BPY};
- (d) $I_{\Delta B}$, the normalized current of the interface primary phase 'B' winding current, the base is the dc component of the reinjection current I_{BPY};
- (e) I_A, the normalized current of the interface primary line current, the base is the dc component of the reinjection current I_{BPY};
- (f) The spectrum of the output current I_A.

The harmonic spectrum and the THD for the linear symmetrical reinjection waveforms are given by the following expressions.

$$\frac{B_{outL-n}}{V_{outL-1}} = \frac{\pm1}{n^2} \qquad n=6k\pm1, \qquad k=1,2,\cdots \tag{2.71}$$

$$THD_{outL} = \sqrt{\frac{5\pi^4}{18\times27}-1} \approx 4.6380\% \tag{2.72}$$

When the linear symmetrical reinjection waveforms are supplied to the two half bridges, the 6-pulse MLCR converter (refer to Figure 2.3) current waveforms are shown in Figure 2.16, where

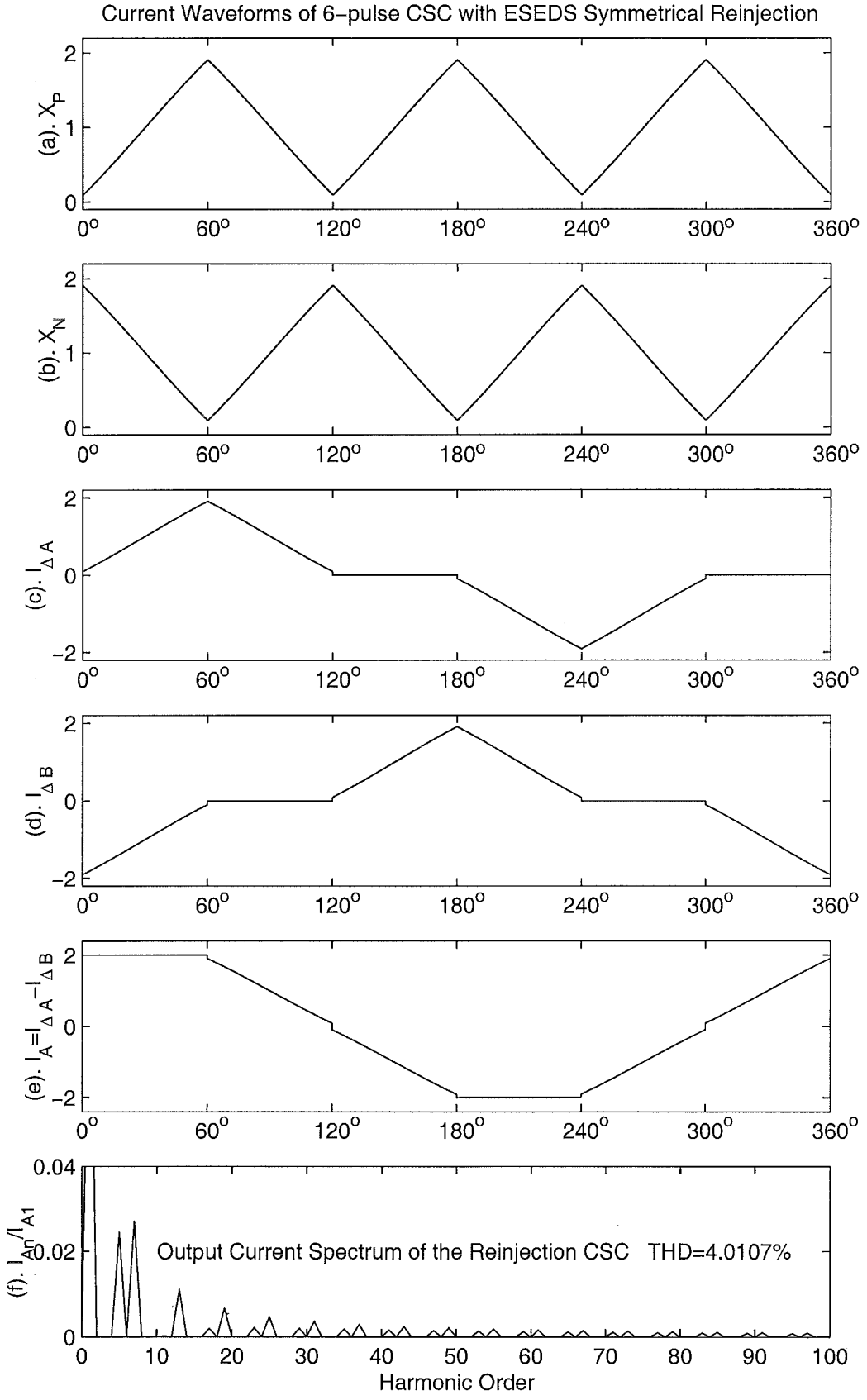


Figure 2.15 Current Waveforms of 6-pulse CSC with ESEDS Reinjection

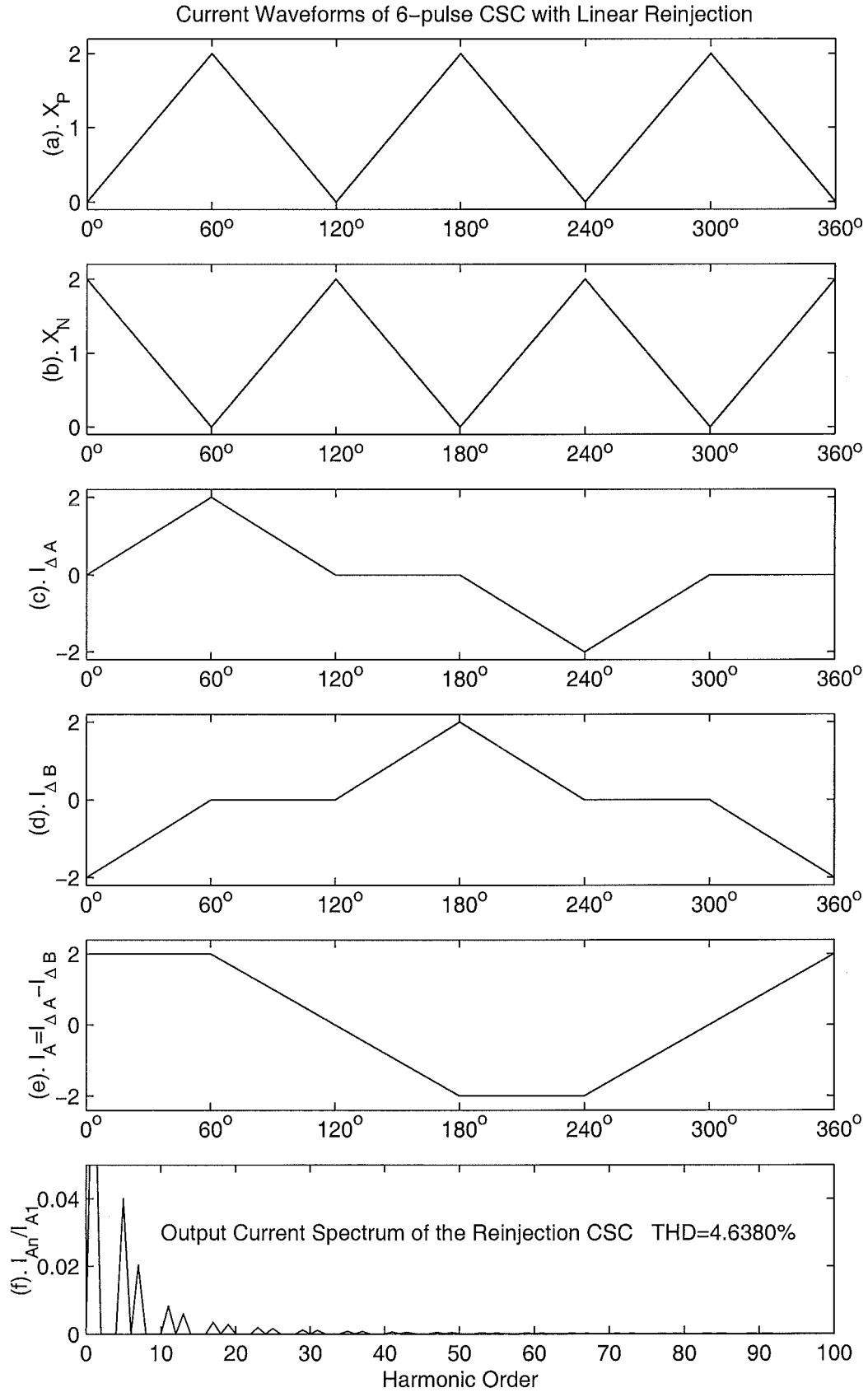


Figure 2.16 Current Waveforms of 6-pulse CSC with Linear Reinjection

- (a) X_P, the normalized current of the reinjection current I_{BPY}, the base is its dc component;
- (b) X_N, the normalized current of the reinjection current I_{BNY}, the base is its dc component;
- (c) $I_{\Delta A}$, the normalized current of the interface primary phase 'A' winding current, the base is the dc component of the reinjection current I_{BPY};
- (d) $I_{\Delta B}$, the normalized current of the interface primary phase 'B' winding current, the base is the dc component of the reinjection current I_{BPY};
- (e) I_A, the normalized current of the interface primary line current, the base is the dc component of the reinjection current I_{BPY};
- (f) The spectrum of the output current I_A.

It can be seen that the 6-pulse reinjection converter system ac output waveform is a trapezoidal waveform for the linear symmetrical reinjection, or very close to trapezoidal waveform for ESEDS symmetrical reinjection. Obviously the 6-pulse reinjection converter system ac output has more harmonic content than that of the 12-pulse reinjection converter.

2.4.3 Multi-Level Reinjection for 6-Pulse System

As for the 12-pulse reinjection conversion system, the multi-level conversion concept is adopted to generate the required reinjection waveforms for the 6-pulse conversion system.

The multi-level symmetrical reinjection waveforms generated by ideal switches and an ideal dc power source are step waveforms. The width and height of every step in the multi-level symmetrical step reinjection waveforms are decided based on the following considerations:

a. simplicity of implementation, i.e. equal level width and equal increment;
b. minimum harmonic distortion caused by the multi-level approximation;
c. sufficient zero width for valves to switch under zero voltage or current.

The ESDES symmetrical waveforms shown in Figures 2.17 (a), (b) are divided into m equal length portions from 0^o to 60^o, the height of the corresponding step waveform being determined by the area equivalent principle, i.e. for any interval the corresponding area is the same for the step symmetrical waveform and the ESDES symmetrical waveform. These step waveforms are supplied to the bridges to obtain the ac output waveform with minimum THD under the symmetrical restriction. Although the exact zero level for soft switching is not provided, as the level number m increases, the level

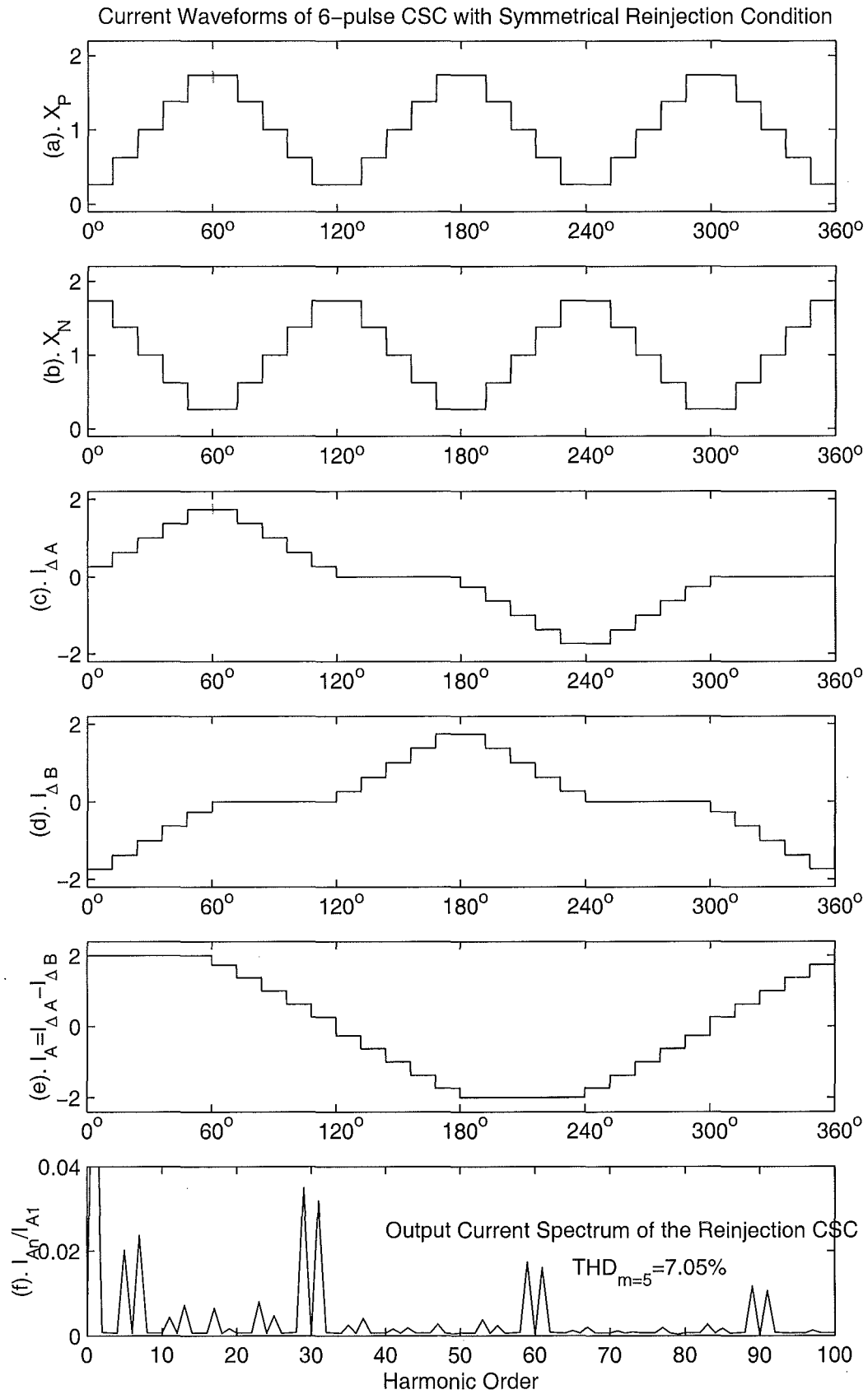


Figure 2.17 Current Waveforms of 6-pulse CSC with Step-ESEDS Reinjection

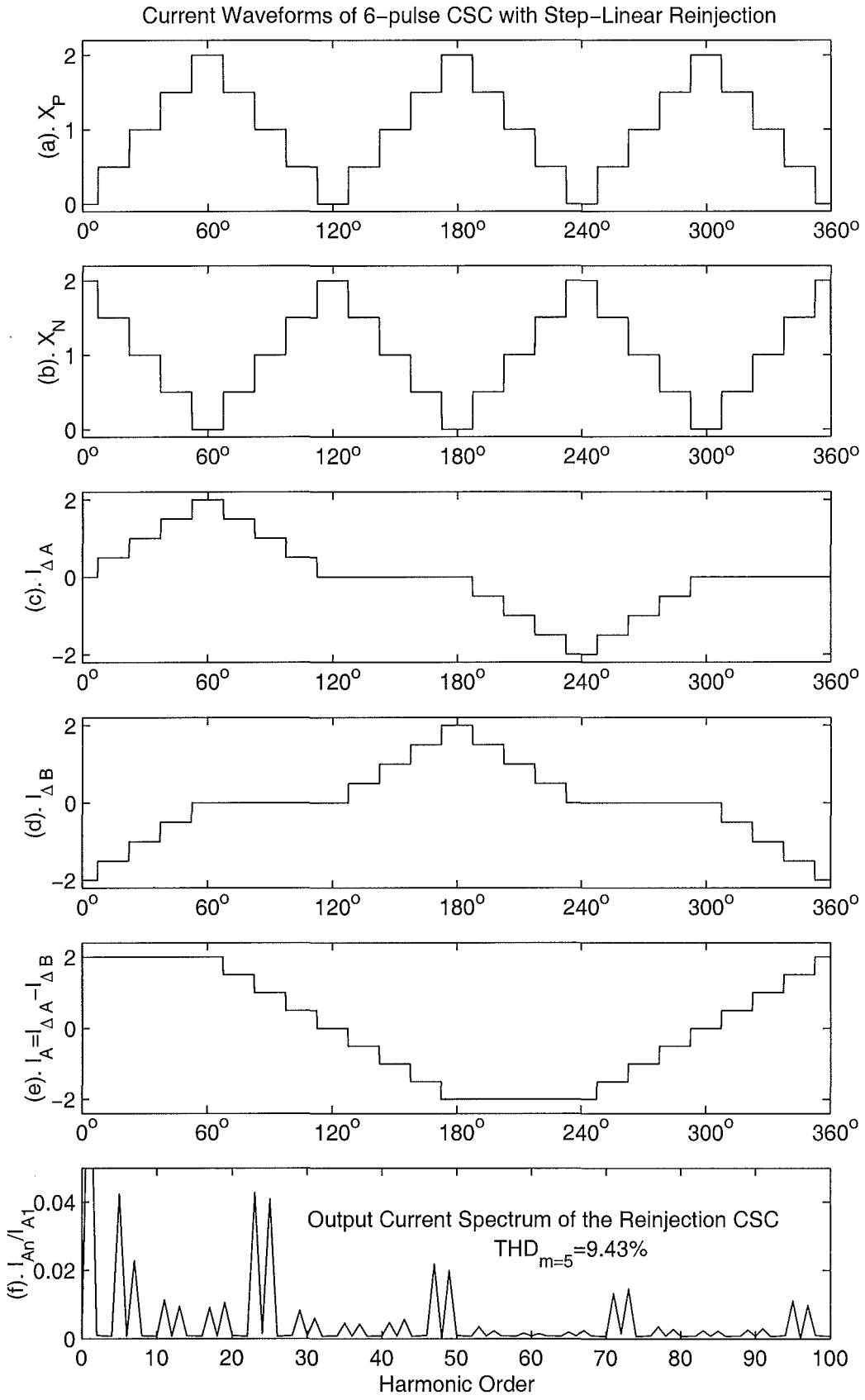


Figure 2.18 Current Waveforms of 6-pulse CSC with Step-Linear Reinjection

height decreases and the power valves switch under very low voltage or current stress. If the m heights are denoted by H_{6Si} $i = 1, 2, \cdots, m$, from 0 to $\pi/6$, they are given by

$$H_{6Si} = 1 + 3.4641m \sin\left(\frac{\pi}{6m}\right) \sin\left[\frac{(2i-1)\pi}{6m} - \frac{\pi}{6}\right] \qquad i = 1, 2, \cdots, m \tag{2.73}$$

The linear symmetrical waveforms are converted to the symmetrical step waveform with m levels in the interval from $-\frac{\pi}{6(m-1)}$ to $\frac{\pi}{3} - \frac{\pi}{6(m-1)}$, almost in the same way. The only difference results from the starting and stopping points of the zero level soft switching region, the $\pi/6$ radians interval being divided into $(m-1)$ sections of equal width. The first interval starts at $-\frac{\pi}{6(m-1)}$ and stops at $\frac{\pi}{6(m-1)}$, with zero level height; the second interval starts at $\frac{\pi}{6(m-1)}$ and stops at $\frac{3\pi}{6(m-1)}$, with level height $\frac{2}{m-1}$; $\cdots$; the i^{th} interval starts at $\frac{(2i-3)\pi}{6(m-1)}$ and stops at $\frac{(2i-1)\pi}{6(m-1)}$, with level height $\frac{2(i-1)}{m-1}$; $\cdots$; the m^{th} interval starts at $\frac{(2m-3)\pi}{12(m-1)}$ and stops at $\frac{(2m-1)\pi}{12(m-1)}$, with level height $\frac{2(m-1)}{m-1}$. The heights of the m levels are given by

$$H_{6Li} = \frac{2(i-1)}{m-1} \qquad i = 1, 2, \cdots, m \tag{2.74}$$

The linearly increasing and decreasing waveforms with zero levels simplify the practical implementation, using the same type of components.

When the two half bridges are supplied with the ESEDS symmetrical step-waveforms (for m=5) the waveforms at their power system side and the converter output terminals are shown in Figure 2.17 (c), (d) and (e), and the reinjection converter system (refer to Figure 2.3) output waveform spectrum is shown in Figure 2.17 (f).

When the two bridges are supplied with the linear symmetrical step-waveforms (for m=5) the waveforms at their power system side and the converter system output terminals are shown in Figure 2.18 (c), (d) and (e), and the reinjection converter system output waveform spectrum is shown in Figure 2.18 (f).

The voltage source converter with the two half bridges supplied by the step multi-level reinjection voltage waveforms, is referred here as the Multi-Level Voltage Reinjection converter (MLVR). Similarly the current source converter with their two half bridges supplied by the multi-level step reinjection current waveforms, is referred here as the Multi-Level Current Reinjection converter (MLCR).

It is obvious that an increase in the level number m results in a decrease in harmonic distortion of the reinjection converter system.

Under ESEDS symmetrical multi-level reinjection, the fundamental peak current, RMS current and total harmonic distortion of the MLCR converter output current are:

Output Current Fundamental Peak Magnitude (ESEDS Symmetrical m-level)

$$I_{A1Sm} = \frac{6}{\pi}\left[1 + 2m^2 \sin^2(\frac{\pi}{6m}) - \frac{\sqrt{3}}{2} m \tan(\frac{\pi}{6m})\right]\frac{I_{dc}}{k_n} \tag{2.75}$$

Output Current RMS Value (ESEDS Symmetrical m-level)

$$I_{ASmRMS} = \frac{\sqrt{2}\, I_{dc}}{k_n}\sqrt{1 + 2m^2 \sin^2(\frac{\pi}{6m}) - \frac{\sqrt{3}}{2} m \tan(\frac{\pi}{6m})} \tag{2.76}$$

Output Current THD (ESEDS Symmetrical m-level)

$$\begin{aligned} THD_{IASm} &= \sqrt{\frac{2I^2_{ASmRMS}}{I^2_{A1Sm}} - 1} \\ &= \sqrt{\frac{\pi^2}{9\left[1 + 2m^2 \sin^2(\frac{\pi}{6m}) - \frac{\sqrt{3}}{2} m \tan(\frac{\pi}{6m})\right]} - 1} \end{aligned} \tag{2.77}$$

Under linear symmetrical multi-level reinjection waveforms, the fundamental peak current, RMS current and total harmonic distortion of the MLCR converter output current are:

Output Current Fundamental Peak Magnitude(Linear Symmetrical m-level)

$$I_{A1Lm} = \frac{8I_{dc}}{\pi k_n}\left[\cos\left(\frac{(2m-3)\pi}{6(m-1)}\right) + \frac{2}{m-1}\sin\left(\frac{\pi}{6(m-1)}\right)\sum_{j=1}^{m-2} j \sin\left(\frac{j\pi}{3(m-1)}\right)\right] \tag{2.78}$$

Output Current RMS Value (Linear Symmetrical m-level)

$$I_{ALmRMS} = \frac{2I_{dc}}{3k_n}\sqrt{5 + \frac{1}{(m-1)^2}} \tag{2.79}$$

Output Current THD (Linear Symmetrical m-level)

$$\begin{aligned} THD_{IALm} &= \sqrt{\frac{2I^2_{ALmRMS}}{I^2_{A1Lm}} - 1} \\ &= \sqrt{\frac{\pi^2[1 + 5(m-1)^2]}{72(m-1)^2\left[\cos(\frac{(2m-3)\pi}{6(m-1)}) + \frac{2}{m-1}\sum_{j=1}^{m-2} j \sin(\frac{j\pi}{6(m-1)})\right]^2} - 1} \end{aligned} \tag{2.80}$$

Table 2.2 shows the relation between the level number m and the total harmonic distortion THD under the ESEDS and linear symmetrical multi-level reinjection conditions.

Table 2.2 THD_6 of the ESEDS and linear multi-level reinjection

Level m	3	4	5	6	7	8	9	10
THD_{sym}	10.05%	8.29%	7.05%	6.28%	5.76%	5.40%	5.14%	4.95%
THD_{lin}	16.86%	11.86%	9.43%	8.05%	7.19%	6.61%	6.20%	5.91%

The harmonic content reduction slows down when the level number m is greater than 8, and therefore there is no need for very high level numbers; for $m > 10$, the output waveform THD is close to its minimum value, i.e. $\lim_{m\to\infty}[THD_{sym}] = 4.01\%$ and $\lim_{m\to\infty}[THD_{lin}] = 4.64\%$ for the ESEDS and linear symmetrical multi-level reinjection respectively.

Taking into account the duality between the CSC and VSC the total harmonic distortion for MLVR under the ESEDS and linear symmetrical multi-level reinjection can be directly obtained from the MLCR results.

2.5 CONCLUSION

2.5.1 Reinjection Characteristics for 12-Pulse System

The reinjection waveforms for the 12-pulse reinjection converter system are summarized as follows:

1. The ideal reinjection waveform can produce an ac output waveform without harmonic distortion; but the dc power source is required to supply an amplitude and frequency controllable ripple.

2. The ESEDS and linear symmetrical reinjection waveforms can produce ac output waveforms with about 1% total harmonic distortion and without any specific requirements regarding the dc power supply.

3. The multi-level symmetrical reinjection waveforms are the best suited for practical implementation. An m-level ESEDS symmetrical reinjection converter is almost equivalent to a $12m$-pulse (or $6m$-level) conversion system, and an m-level linear symmetrical reinjection converter is equivalent to a $12(m-1)$-pulse (or $(6m-5)$-level) conversion system.

4. For a reinjection waveform level number $m < 6$, ESEDS symmetrical reinjection can produce a better ac output waveform than linear symmetrical reinjection;

however for level numbers $m \geq 8$, there is no significant difference between the ESEDS symmetrical and the linear symmetrical reinjection waveforms.

5. Multi-level linear symmetrical reinjection combines the benefits of harmonic reinjection, multi-level conversion and soft switching together to form the MLVR and MLCR converters. Based on linearity and equal increments, the multi-level linear symmetrical reinjection circuitry can be built up by the same type of components, which is a significant advantage for practical high voltage and high power applications.

2.5.2 Reinjection Characteristics for 6-Pulse System

The reinjection waveforms for the 6-pulse reinjection converter system are summarized as follows:

1. The ideal reinjection waveform can produce an ac output waveform without harmonic distortion; but the dc power source is required to supply an amplitude and frequency controllable ripple.

2. The ESEDS and linear symmetrical reinjection waveforms can produce trapezoidal ac output waveforms with about 4.0% to 4.6% THD (total harmonic distortion) and without any specific requirements regarding the dc power supply.

3. The multi-level symmetrical reinjection waveforms are the best suited for practical implementation. An m-level ESEDS symmetrical reinjection converter is almost equivalent to $6m$-pulse or $2(m+1)$-level conversion system, and the linear symmetrical reinjection converter is equivalent to a $6(m-1)$-pulse or $(2m-1)$-level conversion system.

4. For a reinjection waveform level number $m < 6$, ESEDS symmetrical reinjection can produce a better ac output waveform than linear symmetrical reinjection; however for $m \geq 8$, there is no significant difference between the ESEDS symmetrical and the linear symmetrical reinjection waveforms. For the 6-pulse system under the multi-level symmetrical reinjection, the output waveform minimum THD is about 4.01% or 4.64% for the ESEDS and linear symmetrical multi-level reinjection respectively; reinjection level numbers m greater than 10 would not reduce the THD significantly.

5. Multi-level linear symmetrical reinjection combines the benefits of harmonic reinjection, multi-level conversion and soft switching together to form the MLCR and MLVR converters. Based on linearity and equal increments, the multi-level linear symmetrical reinjection circuitry can be built up by the same type of components, which is a significant advantage for practical high voltage and high power applications.

Chapter 3

MULTI-LEVEL ESEDS-REINJECTION VSC

3.1 INTRODUCTION

The self-commutated Voltage Source Converter (VSC) is favoured by industry over the self-commutated current source converter (CSC), because the latter requires the expensive high voltage ac capacitors to interface with the power system. For high power applications the voltage reinjection configuration based on the conventional 12-pulse converter scheme is more attractive than the configuration based on the 6-pulse converter, not only because it can handle higher power ratings, but also because the 6-pulse converter scheme needs some extra switches to remove the uncertainty of the output voltage, and the triple harmonic voltages require an extra path in the interface transformer for the triple harmonic fluxes. Thus the Multi-Level Reinjection VSC will be described only with reference to the 12-pulse configuration.

The practical implementation of the Multi-Level Reinjection VSC is based on the principle that the voltages across the two main bridges can be decomposed into their dc and ac components; the dc components of the two main bridge voltages are always the same, while the ac voltage components are the same in amplitude but in opposite direction at any instant. This means that the main bridge voltages can be formed by an isolated ac voltage component added to the same dc component either forwardly or in reverse respectively. This ac component is referred to as the fully symmetrical reinjection voltage.

The amplitude of the fully symmetrical reinjection voltage must be related to the dc voltage, and its frequency and phase must be synchronized with those of the ac output voltage of the main bridges; thus a self-commutated H-bridge powered by the dc source is a suitable choice to generate the fully symmetrical reinjection voltage. Because this generated ac voltage must be isolated from the dc source in order to be added to the dc source voltage, an isolation transformer is needed to form the reinjection circuit.

Depending on the location of the reinjection components with respect to the main power flow path, two possible configurations are described in this chapter. In the first configuration the dc outputs of the two main bridges are connected in parallel;

this results in a reduction of the dc side capacitance requirement but the reinjection transformer secondary windings are connected in the main power flow path. In the alternative configuration the two main bridges are in cascaded connection, the reinjection components are not involved in the dc current path but there is no reduction in the dc capacitance requirement.

3.2 THE PARALLEL CONNECTED BRIDGE SCHEME

3.2.1 Operating Principle

Figure 3.1 shows a double bridge self-commutated voltage source converter modified with extra circuitry to produce a 36-pulse equivalent multi-level waveform. The extra circuit consists of a reinjection transformer and a GTO-Diode single phase bridge.

The reinjection transformer two windings with turns N_{s1} and N_{s2} are connected to obtain the following voltages: $u_{j1} = -u_{j2} = u_j$

The voltages across the main Y and Δ connected bridges, are respectively:

$$V_{YY} = U_{dc} + u_{j1} = U_{dc} + u_j \qquad V_{Y\Delta} = U_{dc} + u_{j2} = U_{dc} - u_j$$

If the voltage drops of the converter valves are ignored, the ac voltage outputs of the Y connected and Δ connected bridges are also V_{YY} and $V_{Y\Delta}$, thus, adjustments of u_j can shape the ac output voltage waveforms of both bridges simultaneously.

Again neglecting the voltage drops of the reinjection switches, the reinjection voltage u_j can be regulated by the on-off pattern of the switching devices and the turns ratio of the reinjection transformer. Under balanced conditions the harmonics of orders $6k(2k-1) \pm 1$ $(k = 1, 2, \cdots)$ in the star and delta connected secondary windings will cancel on the primary side. Then the selection of the switching pattern and the transformer turns ratio are made to minimise the remaining harmonics.

Another important consideration is the reduction of switching losses, which can be achieved by using the fundamental modulation firing for the main bridge switches and keeping the switching frequency of the reinjection bridges as low as possible.

The proposed switching pattern is shown in Figure 3.2, the main bridge switches ($S_{Y1} - S_{Y6}$ and $S_{\Delta 1} - S_{\Delta 6}$) are under the firing control of the conventional 12-pulse converter; the reinjection switches ($S_{j1} - S_{j4}$) are synchronously switched every 60^o (i.e. the switching frequency is 6 times the fundamental frequency), 30^o in on-state and 30^o in off-state.

For the provision of the possible three levels the firing sequence of the reinjection switches is as follows:

- S_{j4}'s firing signal leads S_{j1}'s by 10^o, and their common on-state overlap provides a positive level for 20^o;

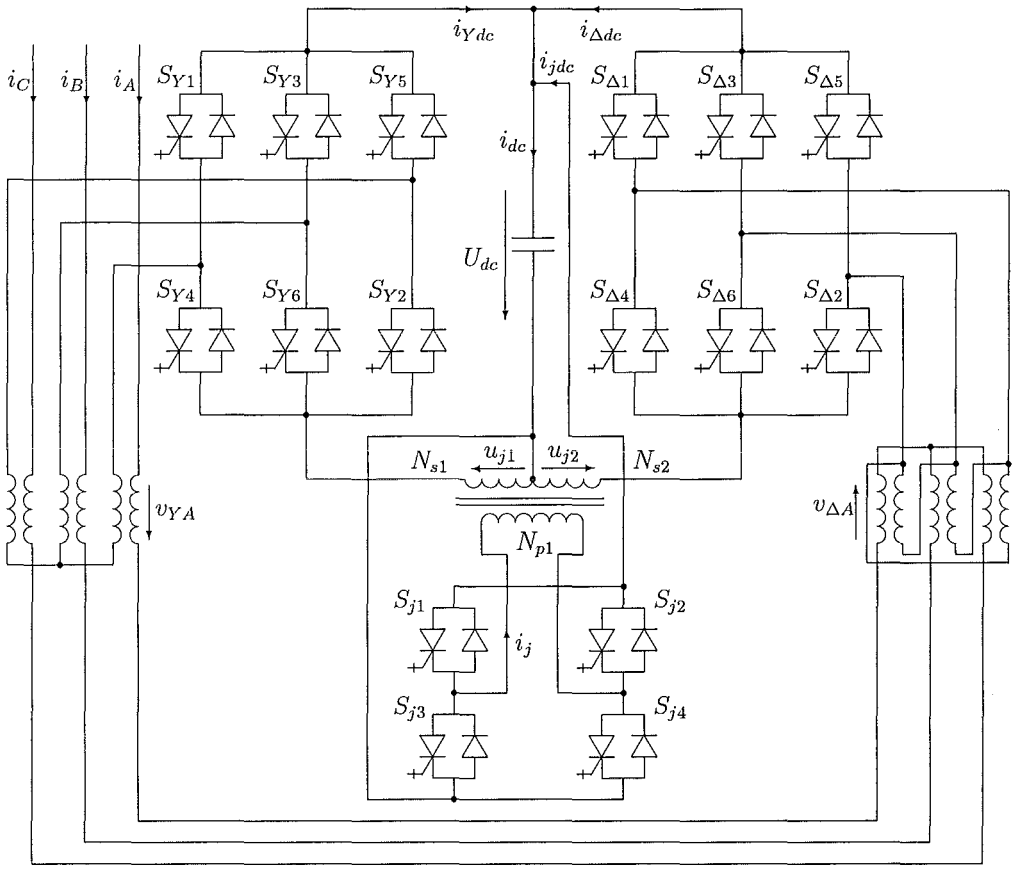


Figure 3.1 The parallel 3-Level ESEDS-VSC

- S_{j1}'s firing signal leads S_{j2}'s by 20^o, and their common on-state overlap provides a zero level for 10^o;
- S_{j2}'s firing signal leads S_{j3}'s by 10^o, and their common on-state overlap provides a negative level for 20^o;
- S_{j3}'s firing signal leads S_{j4}'s by 20^o, and their common on-state overlap provides a zero level for 10^o.

The reinjection transformer turns ratios can be decided based on the ESEDS-reinjection waveform. From Equation 2.55, which describes the individual level height related to the dc component of the voltage across the bridges, the normalized m level heights ($H_{jSi} = u_{ji}/U_{dc}$ $i = 1, 2, \cdots, m$) of the reinjection voltage u_j are given by

$$H_{jSi} = 14.4195m \sin\left(\frac{\pi}{12m}\right) \sin\left[\frac{(2i-1)\pi}{12m} - \frac{\pi}{12}\right] \qquad i = 1, 2, \cdots, m \tag{3.1}$$

For the 3-level u_j, they are:

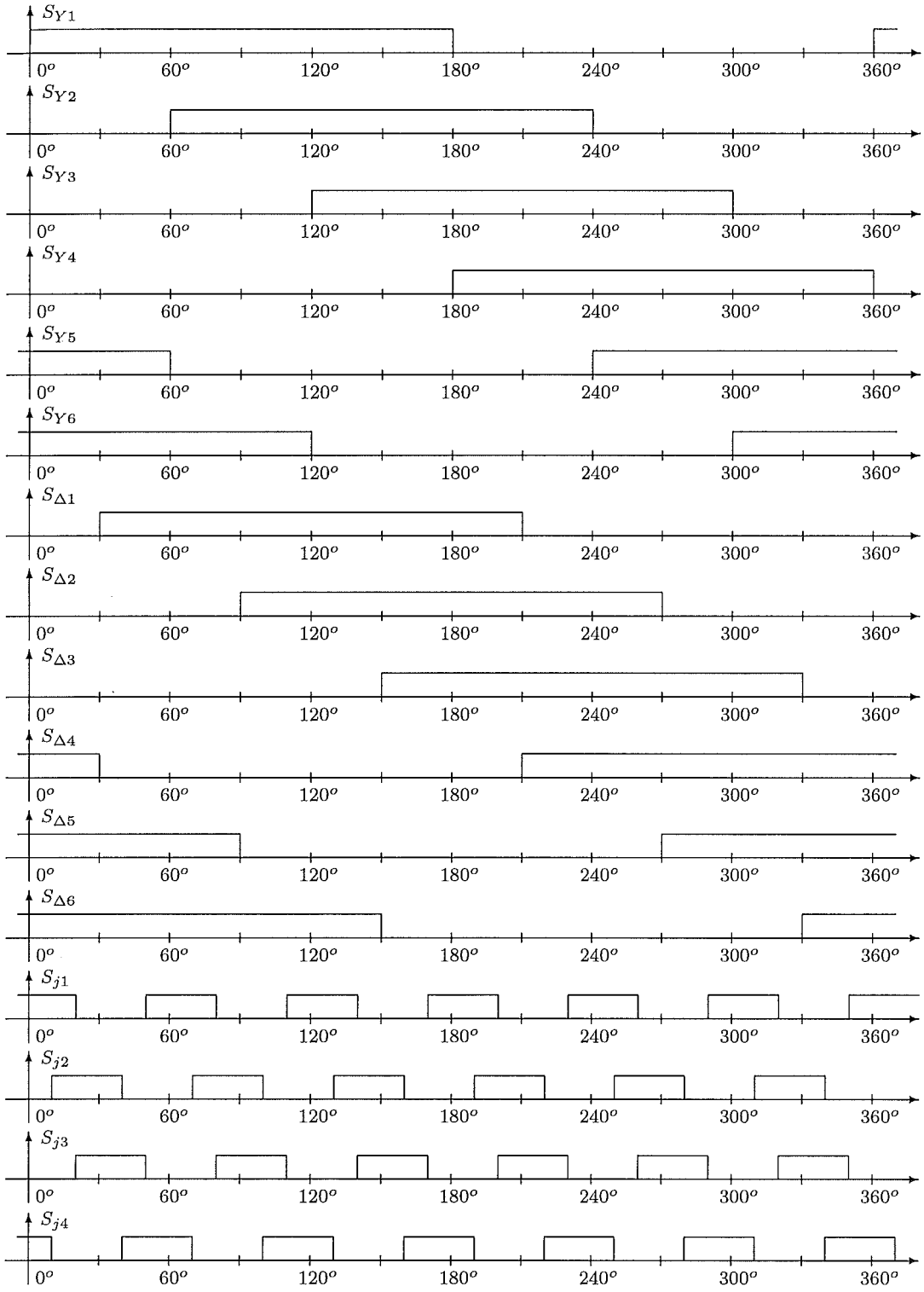


Figure 3.2 The Switching Pattern of the 3-level ESEDS-VSC

$H_{jS1} = -0.6547 \qquad H_{jS2} = 0 \qquad H_{jS3} = 0.6547$

therefore the reinjection transformer turns ratio is:

$k_j = N_{p1}/N_{s1} = N_{p2}/N_{s1} = 0.6547.$

That value will be shown in the next section to be the optimal ratio to minimize the output voltage total harmonic distortion ($THD_{Vmin} = 5.09\%$).

For some applications the harmonic distortion level of the 36-pulse configuration may not be low enough, and a higher level number is required.

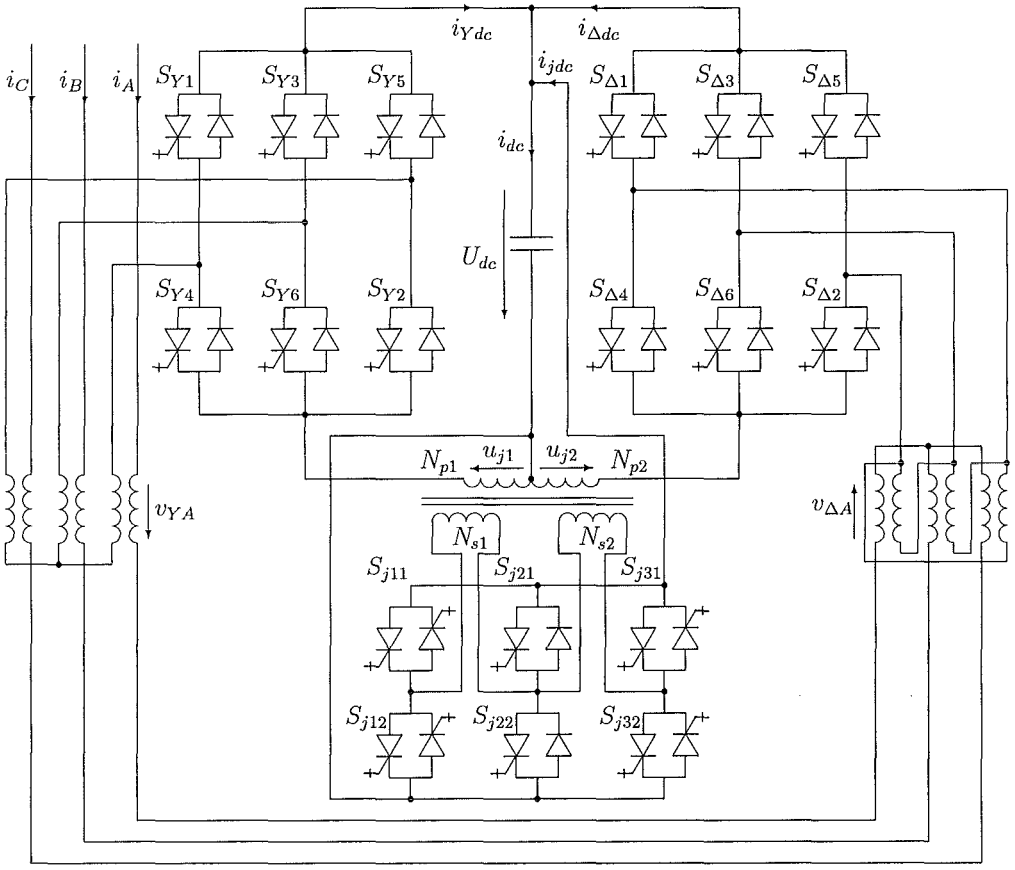


Figure 3.3 The parallel 5-Level ESEDS reinjection VSC

Figure 3.3 shows a 60-pulse equivalent MLVR VSC configuration with a 5-level reinjection voltage, which produces a very low output voltage harmonic distortion level ($THD_V = 3.16\%$) and should meet the strictest standards.

From Equation 3.1 the 5 normalized level heights of the reinjection voltage are:

$H_{jS1} = -0.7845 \qquad H_{jS2} = -0.3944$

$H_{jS3} = 0 \qquad H_{jS4} = 0.3944 \qquad H_{jS5} = 0.7845$

thus the required turns ratios are arranged as:

$$k_{j1} = N_{p1}/(N_{s1} + N_{s2})$$
$$= N_{p2}/(N_{s1} + N_{s2}) = 0.3922$$

$$k_{j2} = N_{p1}/N_{s1}$$
$$= N_{p2}/N_{s1} = 0.7844$$

The modification from 0.7845 and 0.3944 to 0.7844 and 0.3922 provides a simple reinjection bridge structure and forces the reinjection transformer windings N_{s1} and N_{s2} to be used equally. As the windings with turns N_{s1} and N_{s2} are identical, they can be individually connected across the dc capacitor or in series to generate the required reinjection voltage levels by appropriate switching actions of the reinjection switches. Thus the N_{s1} winding is connected to the dc capacitor to generate the high amplitude negative level; the N_{s2} winding is connected to the dc capacitor to generate the high amplitude positive level; the N_{s1} and N_{s2} windings in series generate the low amplitude positive and negative levels. The N_{s1} and N_{s2} windings are controlled to operate with the same rating.

Configurations of level numbers beyond 5 will become complicated and their harmonic content would not be reduced significantly. The following waveform analysis is made only for the configuration shown in Figure 3.1.

3.2.2 Analysis of the Voltage Waveforms

In Figure 3.4(e), the ac output phase voltage of the Δ connected converter has the following levels:

$$v_{\Delta a}(\omega t)/U_{dc} = \begin{cases} 0 & 0^o < \omega t < 30^o \\ (1-k_j) & 30^o < \omega t < 40^o \\ 1 & 40^o < \omega t < 50^o \\ (1+k_j) & 50^o < \omega t < 70^o \\ 1 & 70^o < \omega t < 80^o \\ (1-k_j) & 80^o < \omega t < 100^o \\ 1 & 100^o < \omega t < 110^o \\ (1+k_j) & 110^o < \omega t < 130^o \\ 1 & 130^o < \omega t < 140^o \\ (1-k_j) & 140^o < \omega t < 150^o \\ 0 & 150^o < \omega t < 180^o \end{cases} \tag{3.2}$$

The corresponding harmonic content is expressed by the Fourier series

$$v_{\Delta a}(\omega t) = \sum_{n=1}^{\infty} V_{\Delta an} U_{dc} \sin(n\omega t) \tag{3.3}$$

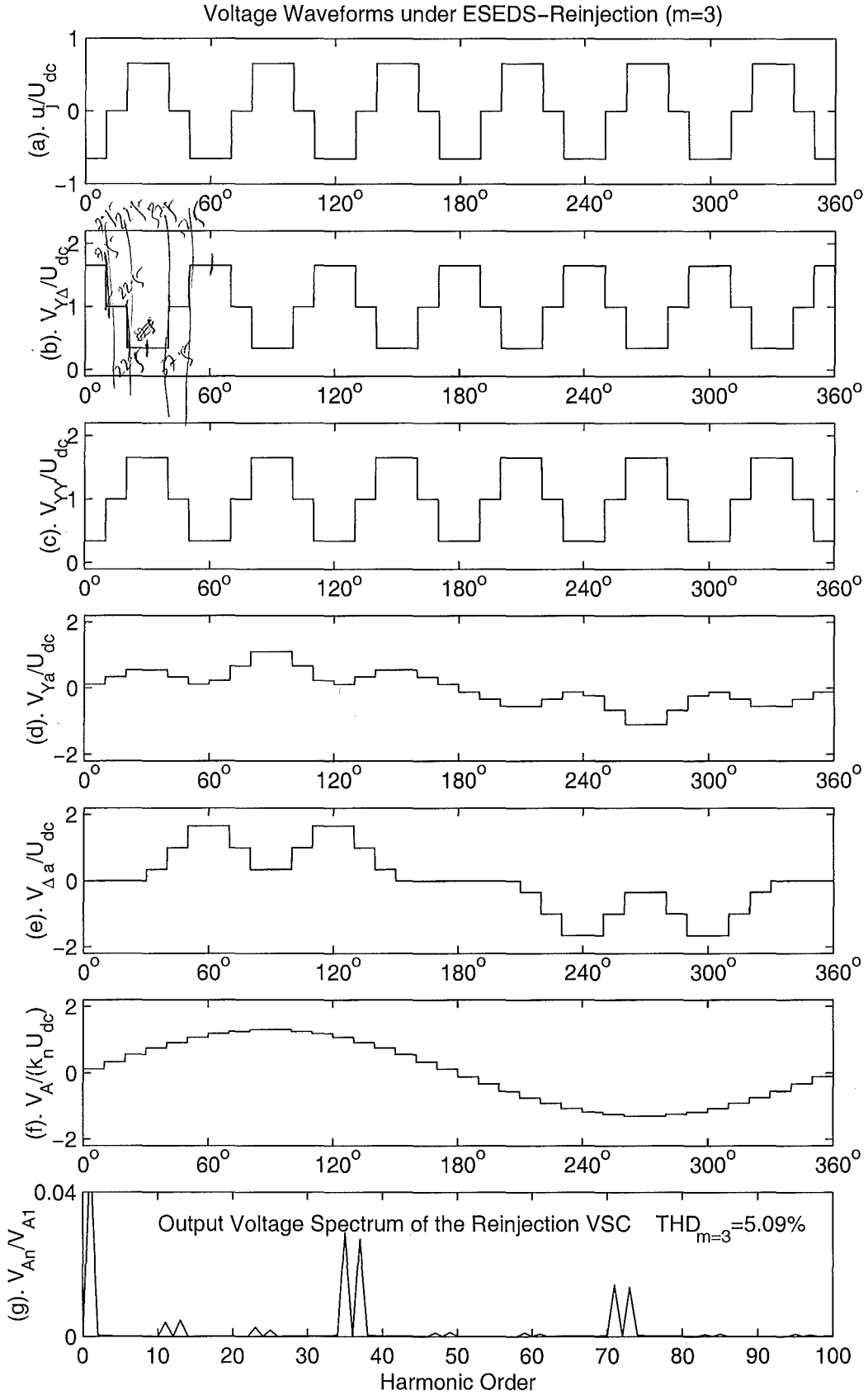


Figure 3.4 The Voltage Waveforms of the 3-Level ESEDS-VSC

where

$$V_{\Delta an} = \frac{2[1-(-1)^n]}{n\pi}\left\{1+k_j\left[8\sin(\frac{n\pi}{6})\sin(\frac{n\pi}{12})\cos(\frac{n\pi}{36})-1\right]\right\}\cos(\frac{n\pi}{6}) \quad for \quad n=1,2,3,\cdots \tag{3.4}$$

Similarly, the ac output phase voltage components of the Y connection converter (the same as the waveform of $v_{\Delta a}$ shown in Figure 3.4(e), except for the 30^o phase displacement) are as follows:

$$v_{Ya}(\omega t)/U_{dc} = \begin{cases} (1-k_j)/3 & 0^o < \omega t < 10^o \\ 1/3 & 10^o < \omega t < 20^o \\ (1+k_j)/3 & 20^o < \omega t < 40^o \\ 1/3 & 50^o < \omega t < 60^o \\ 2(1-k_j)/3 & 60^o < \omega t < 70^o \\ 2/3 & 70^o < \omega t < 80^o \\ 2(1+k_j)/3 & 80^o < \omega t < 100^o \\ 2/3 & 100^o < \omega t < 110^o \\ 2(1-k_j)/3 & 110^o < \omega t < 120^o \\ (1-k_j)/3 & 120^o < \omega t < 130^o \\ 1/3 & 130^o < \omega t < 140^o \\ (1+k_j)/3 & 140^o < \omega t < 160^o \\ 1/3 & 160^o < \omega t < 170^o \\ (1-k_j)/3 & 170^o < \omega t < 180^o \end{cases} \tag{3.5}$$

and the corresponding harmonic content

$$v_{Ya}(\omega t) = \sum_{n=1}^{\infty} V_{Yan} U_{dc} \sin(n\omega t) \qquad for \qquad n=1,2,3,\cdots \tag{3.6}$$

where

$$V_{Yan} = \frac{4[1-(-1)^n]}{3n\pi}\{1+k_j[\frac{2\cos(\frac{n\pi}{36})\left(2\cos(\frac{n\pi}{4})-\cos(\frac{n\pi}{12})\right)}{\cos\frac{n\pi}{6}}-1]\}\cos^2(\frac{n\pi}{6}) \quad for \quad n=1,2,3,\cdots \tag{3.7}$$

The output (or primary side) ac voltage, V_A, is the sum of $v_{Ya}(\omega t)$ and $v_{\Delta a}(\omega t)$, namely

$$V_A = k_n[v_{Ya}(\omega t) + \frac{v_{\Delta a}(\omega t)}{\sqrt{3}}] \tag{3.8}$$

where k_n is the turns ratio of the Y/Y interface transformer.

Thus the output voltage components of the half cycle waveform are:

$$\frac{V_A}{k_n U_{dc}} = \begin{cases} (1-k_j)/3 & 0^o < \omega t < 10^o \\ 1/3 & 10^o < \omega t < 20^o \\ (1+k_j)/3 & 20^o < \omega t < 30^o \\ (1+k_j)/3 + (1-k_j)/\sqrt{3} & 30^o < \omega t < 40^o \\ 1/3 + 1/\sqrt{3} & 40^o < \omega t < 50^o \\ (1-k_j)/3 + (1+k_j)/\sqrt{3} & 50^o < \omega t < 60^o \\ 2(1-k_j)/3 + (1+k_j)/\sqrt{3} & 60^o < \omega t < 70^o \\ 2/3 + 1/\sqrt{3} & 70^o < \omega t < 80^o \\ 2(1+k_j)/3 + (1-k_j)/\sqrt{3} & 80^o < \omega t < 100^o \\ 2/3 + 1/\sqrt{3} & 100^o < \omega t < 110^o \\ 2(1-k_j)/3 + (1+k_j)/\sqrt{3} & 110^o < \omega t < 120^o \\ (1-k_j)/3 + (1+k_j)/\sqrt{3} & 120^o < \omega t < 130^o \\ 1/3 + 1/\sqrt{3} & 130^o < \omega t < 140^o \\ (1+k_j)/3 + (1-k_j)/\sqrt{3} & 140^o < \omega t < 150^o \\ (1+k_j)/3 & 150^o < \omega t < 160^o \\ 1/3 & 160^o < \omega t < 170^o \\ (1-k_j)/3 & 170^o < \omega t < 180^o \end{cases} \tag{3.9}$$

The total RMS value, is given by the expression

$$V_{ARMS} = \frac{k_n U_{dc}}{9} \sqrt{36 + 18\sqrt{3} + (24 - 12\sqrt{3}) k_j^2}. \tag{3.10}$$

and the peak amplitude of its fundamental component:

$$V_{A1} = \frac{4 k_n U_{dc}}{\pi} \left[1 + \left(4 \cos(\frac{\pi}{36}) \sin(\frac{\pi}{12}) - 1 \right) k_j \right] \tag{3.11}$$

The total harmonic distortion of the phase output voltage, THD_V, is given by

$$THD_V = \sqrt{\frac{2V_{ARMS}^2}{V_{A1}^2} - 1} \tag{3.12}$$

and the reinjection transformer turns ratio required to minimize the total harmonic distortion is

$$k_j = 1.5(7 + 4\sqrt{3}) \left[4 \cos(\frac{\pi}{36}) \sin(\frac{\pi}{12}) - 1 \right] \approx 0.6547 \tag{3.13}$$

which is the same as the value from Equation 3.1, and produces the following minimum

$$THD_{Vmin} = 5.09\%. \tag{3.14}$$

Alternatively to cancel completely the lowest harmonic order of the basic 12-pulse

conversion (i.e. the 11^{th}) the required value of k_j is 0.6274. However, in this case the THD (5.13%) is slightly increased.

3.2.3 Analysis of Current Waveforms

I. Analysis of the output current waveform

The self-commutated converters used in high power and high voltage applications are normally connected to a strong power system. In such cases the source impedance is not significant and the power system seen from the interface transformer primary terminals can be modelled as an ideal three phase voltage source V_s, i.e.

$$\mathbf{V_s}(\omega t) = \begin{bmatrix} v_{sA}(\omega t) \\ v_{sB}(\omega t) \\ v_{sC}(\omega t) \end{bmatrix} = \begin{bmatrix} V_{sm}\sin(\omega t + \phi) \\ V_{sm}\sin(\omega t - 120^o + \phi) \\ V_{sm}\sin(\omega t + 120^o + \phi) \end{bmatrix} \tag{3.15}$$

Under the assumptions that the capacitance of the converter dc side is infinite, and the on state voltage drop of all switches in the converter system is ignored, the converter seen from the interface transformer secondary terminals can be modelled as a voltage source V_o, without internal impedance but with harmonics, i.e.

$$\mathbf{V_o}(\omega t) = \begin{bmatrix} v_A(\omega t) \\ v_B(\omega t) \\ v_C(\omega t) \end{bmatrix} = \begin{bmatrix} \sum_{n=1}^{\infty} V_{An}\sin(n\omega t) \\ \sum_{n=1}^{\infty} V_{An}\sin(n\omega t - 120^o) \\ \sum_{n=1}^{\infty} V_{An}\sin(n\omega t + 120^o) \end{bmatrix}. \tag{3.16}$$

These two voltage sources are inter connected via the interface transformer. If the interface transformer is perfectly balanced and the winding resistance and core loses are ignored, the two voltage sources are connected by L_s, the leakage inductance of the interface transformer. The output current waveforms of the converter system can then be obtained by analysis of the simple model in Figure 3.5. The output current vector

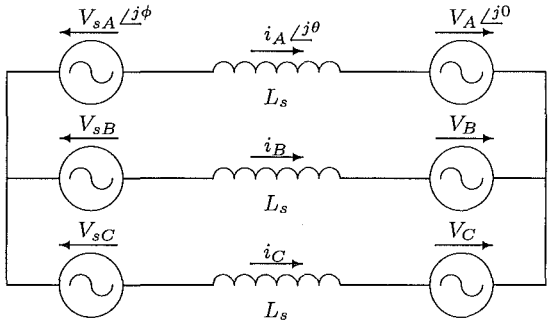


Figure 3.5 The ESEDS reinjection VSC system model

$$\mathbf{I_o}(\omega t) = [i_A(\omega t) \;\; i_B(\omega t) \;\; i_C(\omega t)]^T \tag{3.17}$$

is governed by the equation below

$$L_s \frac{dI_o(\omega t)}{dt} = V_s(\omega t) - V_o(\omega t) \tag{3.18}$$

Thus the output current vector can be expressed as

$$\mathbf{I_o}(\omega t) = \frac{1}{X_s} \int_0^{\omega t} [V_s(\omega t) - V_o(\omega t)] d(\omega t) + I_o(0) \tag{3.19}$$

where $X_s = \omega L_s$ is the leakage reactance of the interface transformer. In the steady state $I_o(\omega t)|_{\omega t=0} = -I_o(\omega t)|_{\omega t=\pi}$, and therefore $I_o(0)$ can be determined from

$$\mathbf{I_o}(0) = -\frac{V_{sm}}{X_s} \begin{bmatrix} \cos(\phi) \\ \cos(\phi - 120^o) \\ \cos(\phi + 120^o) \end{bmatrix} + \frac{1}{2X_s} \int_0^{\pi} V_o(\omega t) d(\omega t) \tag{3.20}$$

Thus the output current vector can be expressed as

$$\mathbf{I_o}(\omega t) = \mathbf{F_o}(\omega t) - \mathbf{F_s}(\omega t) \tag{3.21}$$

where,

$$F_o(\omega t) = \begin{bmatrix} f_a(\omega t) \\ f_b(\omega t) \\ f_c(\omega t) \end{bmatrix} \quad \text{and} \quad F_s(\omega t) = \frac{V_{sm}}{X_s} \begin{bmatrix} \cos(\omega t + \phi) \\ \cos(\omega t + \phi - 120^o) \\ \cos(\omega t + \phi + 120^o) \end{bmatrix}$$

The right side of Equation 3.21 consists of two parts determined by the converter output voltage and the source voltage. The former part, $F_o(\omega t)$ can be expressed in terms of harmonic components and the time functions for different time intervals. The harmonic component expression can be obtained by substituting expression 3.16 into equation 3.21, i.e.

$$\begin{aligned} \mathbf{I_o}(\omega t) = \begin{bmatrix} i_a(\omega t) \\ i_b(\omega t) \\ i_c(\omega t) \end{bmatrix} &= \begin{bmatrix} \sum_{m=2}^{\infty} \frac{1}{mX_S} V_{Am} \cos(m\omega t) \\ \sum_{m=2}^{\infty} \frac{1}{mX_S} V_{Am} \cos(m\omega t - 120^o) \\ \sum_{m=2}^{\infty} \frac{1}{mX_S} V_{Am} \cos(m\omega t + 120^o) \end{bmatrix} \\ &+ \begin{bmatrix} \frac{1}{\omega L_s}[V_{A1} \cos(\omega t) - V_{sm} \cos(\omega t + \phi)] \\ \frac{1}{\omega L_s}[V_{A1} \cos(\omega t - 120^o) - V_{sm} \cos(\omega t - 120^o + \phi)] \\ \frac{1}{\omega L_s}[V_{A1} \cos(\omega t + 120^o) - V_{sm} \cos(\omega t + 120^o + \phi)] \end{bmatrix} \end{aligned} \tag{3.22}$$

Equation 3.22 shows that the harmonic content of the output currents is caused solely by the harmonic components of the converter output voltages, and for a specified voltage waveform the harmonic current injections can be reduced only by increasing

the leakage reactance of the interface transformer.

For simplicity, under balanced operating conditions, the current waveform can be analyzed using the amplitude and phase angle of the individual frequency component of a single phase (phase 'a' for example). The fundamental component amplitude of the phase output current, I_{A1} is given by

$$I_{A1} = \frac{1}{\omega L_s}\sqrt{V_{sm}^2 + V_{A1}^2 - 2V_{sm}V_{A1}\cos(\phi)} = \frac{V_{A1}}{\omega L_s}k \tag{3.23}$$

The m^{th} order harmonic amplitude of the output current is

$$I_{Am} = \frac{V_{Am}}{m\omega L_s} \tag{3.24}$$

Once the converter system output voltage waveform is fixed, i. e. V_{A1}, V_{Am} *and* ϕ have been determined, the output current spectrum becomes

$$I_{Am}/I_{A1} = \frac{1}{m\sqrt{1 + \frac{V_{sm}^2}{V_{A1}^2} - 2\frac{V_{sm}}{V_{A1}}\cos(\phi)}}\frac{V_{Am}}{V_{A1}} = \frac{1}{mk}\frac{V_{Am}}{V_{A1}}, \tag{3.25}$$

which shows that the current spectrum can be simply obtained by dividing the output voltage spectrum by mk (where m is harmonic order, and k is given by

$$k = \sqrt{1 + \frac{V_{sm}^2}{V_{A1}^2} - 2\frac{V_{sm}}{V_{A1}}\cos(\phi)} \tag{3.26}$$

the index of the specified operating condition of the output voltage). Figure 3.7 shows the output current spectra corresponding to the waveforms in Figure 3.6 for the conditions:

$$\begin{aligned}
&(V_{sm} = 0.90V_{A1},\ \phi = 0,\ i.\ e.\ k = 0.1)\\
&(V_{sm} = 1.10V_{A1},\ \phi = 0,\ i.\ e.\ k = 0.1)\\
&(V_{sm} = 0.99V_{A1},\ \phi = 0,\ i.\ e.\ k = 0.01)\\
&(V_{sm} = 1.01V_{A1},\ \phi = 0,\ i.\ e.\ k = 0.01)\\
&(V_{sm} = V_{A1},\quad \phi = 0,\ i.\ e.\ k = 0)
\end{aligned}$$

From Equations 3.23 and 3.25 it is clear that the percentage harmonic content will increase when the fundamental component of the output current is decreased.

Equation 3.22 is not in a suitable form to obtain the output current waveform and the output current RMS value. Instead, the output current waveform described by Equation 3.21 can be obtained by the direct integration of the output voltage in the stair case shaped waveforms. The direct integration of the phase 'a' output voltage provides the multi-slope time domain function $f_a(\omega t)$, the first element of $F_o(\omega t)$, is as

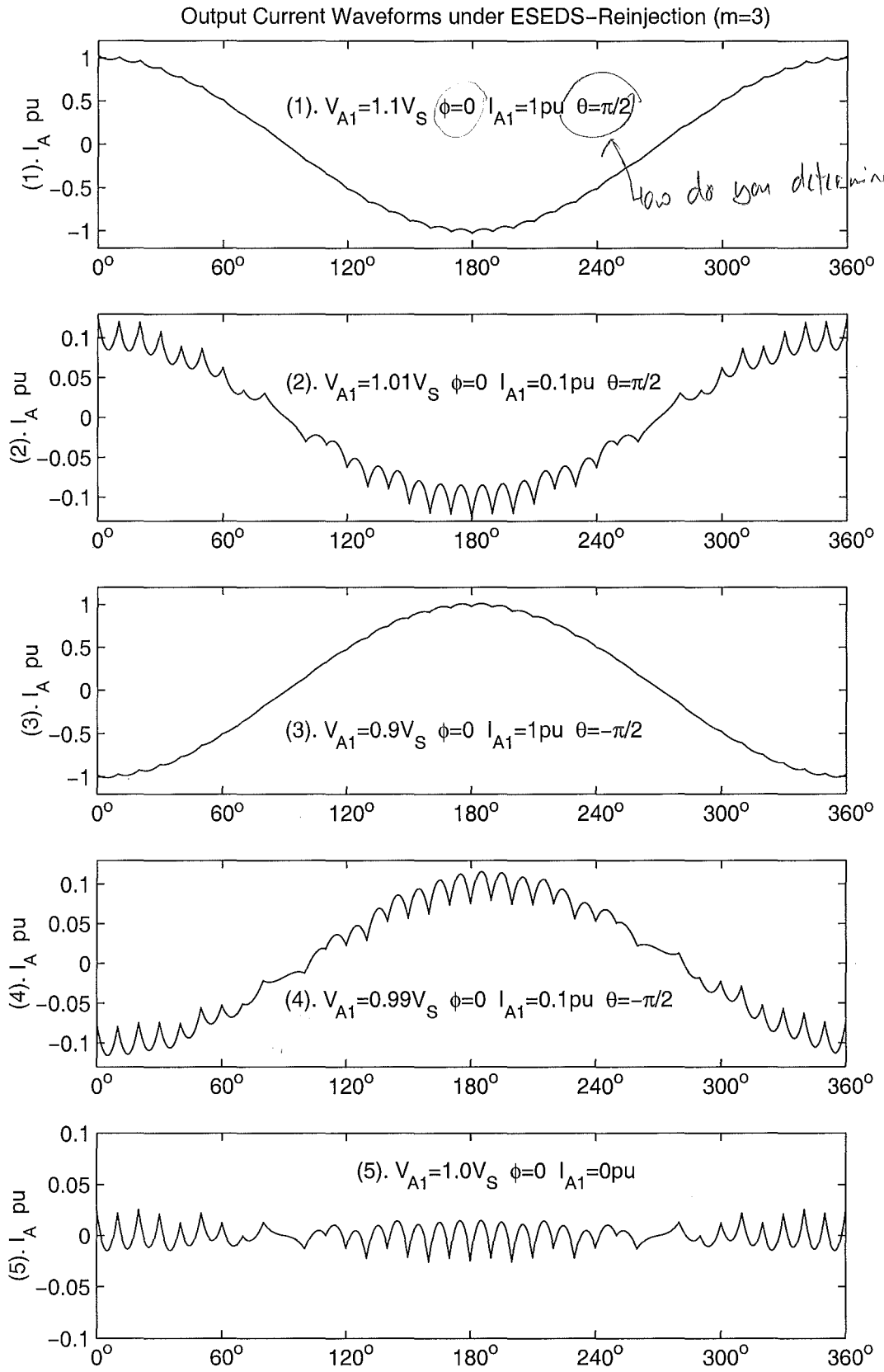


Figure 3.6 The Output Current Waveforms of the 3-Level ESEDS-VSC

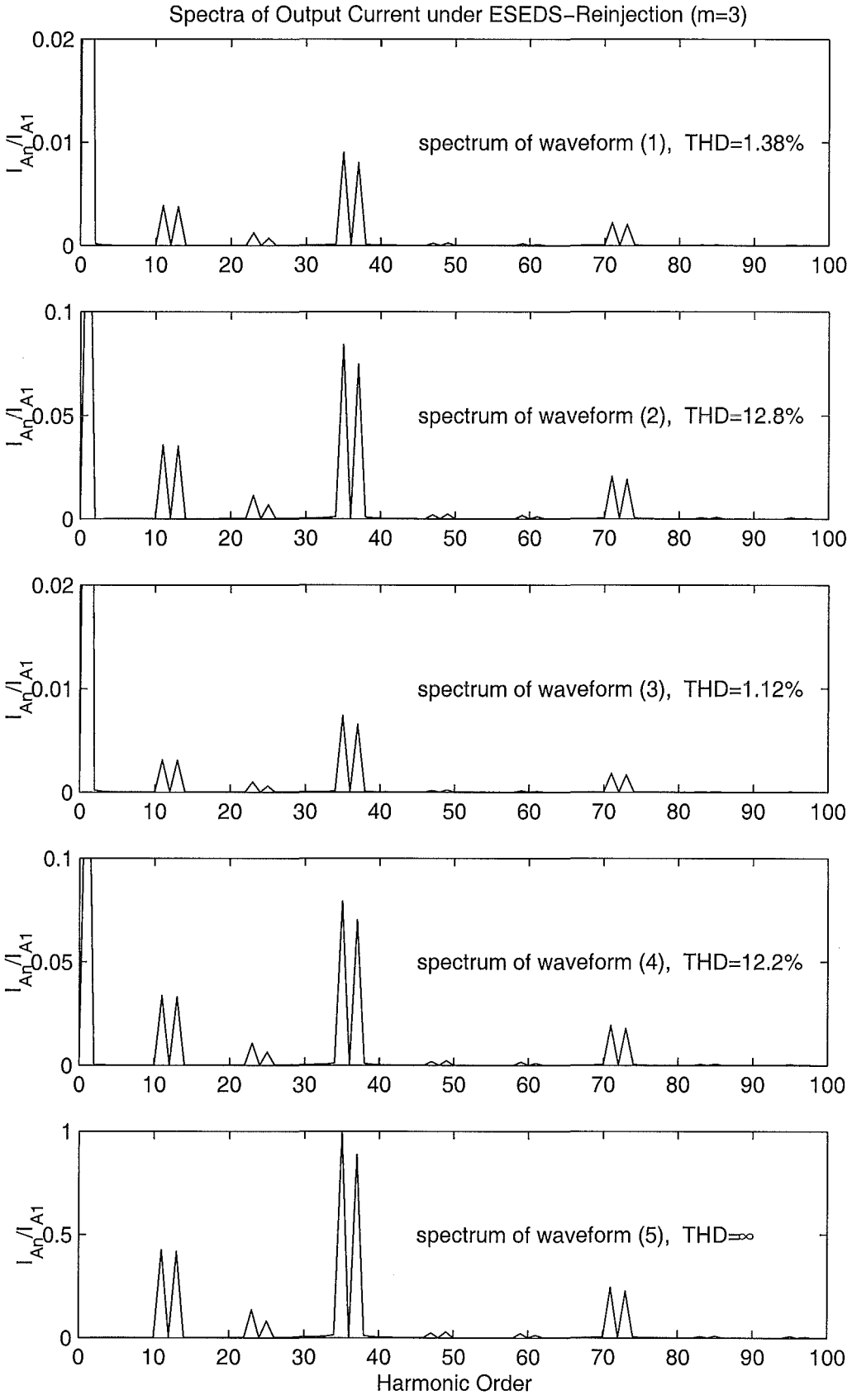


Figure 3.7 The Output Current Spectra of the 3-Level ESEDS-VSC

follows

$$\frac{f_a(\omega t)}{U_C} = \begin{cases} -\frac{\pi}{54}(12+6\sqrt{3}) + \frac{1}{3}(1-k_j)\omega t & 0 < \omega t < \frac{\pi}{18} \\ -\frac{\pi}{54}(11+6\sqrt{3}+k_j) + \frac{1}{3}(\omega t - \frac{\pi}{18}) & \frac{\pi}{18} < \omega t < \frac{2\pi}{18} \\ -\frac{\pi}{54}(10+6\sqrt{3}+k_j) & \\ \quad +\frac{1}{3}(1+k_j)(\omega t - \frac{2\pi}{18}) & \frac{2\pi}{18} < \omega t < 3\frac{\pi}{18} \\ -\frac{\pi}{54}(9+6\sqrt{3}) & \\ \quad +\frac{1}{3}[1+\sqrt{3}+(1-\sqrt{3})k_j](\omega t - \frac{3\pi}{18}) & \frac{3\pi}{18} < \omega t < \frac{4\pi}{18} \\ -\frac{\pi}{54}[8+5\sqrt{3}+(\sqrt{3}-1)k_j] & \\ \quad +\frac{1}{3}(1+\sqrt{3})(\omega t - \frac{4\pi}{18}) & \frac{4\pi}{18} < \omega t < \frac{5\pi}{18} \\ -\frac{\pi}{54}[7+4\sqrt{3}+(\sqrt{3}-1)k_j] & \\ \quad +\frac{1}{3}[1+\sqrt{3}+(\sqrt{3}-1)k_j](\omega t - \frac{5\pi}{18}) & \frac{5\pi}{18} < \omega t < \frac{6\pi}{18} \\ -\frac{\pi}{54}(6+3\sqrt{3}) & \\ \quad +\frac{1}{3}[2+\sqrt{3}+(\sqrt{3}-2)k_j](\omega t - \frac{6\pi}{18}) & \frac{6\pi}{18} < \omega t < \frac{7\pi}{18} \\ -\frac{\pi}{54}[4+2\sqrt{3}+(2-\sqrt{3})k_j] & \\ \quad +\frac{1}{3}(2+\sqrt{3})(\omega t - \frac{7\pi}{18}) & \frac{7\pi}{18} < \omega t < \frac{8\pi}{18} \\ -\frac{\pi}{54}[2+\sqrt{3}+(2-\sqrt{3})k_j] & \\ \quad +\frac{1}{3}[2+\sqrt{3}+(2-\sqrt{3})k_j](\omega t - \frac{8\pi}{18}) & \frac{8\pi}{18} < \omega t < \frac{\pi}{2} \\ \frac{1}{3}[2+\sqrt{3}+(2-\sqrt{3})k_j](\omega t - \frac{\pi}{2}) & \frac{\pi}{2} < \omega t < \frac{10\pi}{18} \\ \frac{\pi}{54}[2+\sqrt{3}+(2-\sqrt{3})k_j] & \\ \quad +\frac{1}{3}(2+\sqrt{3})(\omega t - \frac{10\pi}{18}) & \frac{10\pi}{18} < \omega t < \frac{11\pi}{18} \\ \frac{\pi}{54}[4+2\sqrt{3}+(2-\sqrt{3})k_j] & \\ \quad +\frac{1}{3}[2+\sqrt{3}+(\sqrt{3}-2)k_j](\omega t - \frac{11\pi}{18}) & \frac{11\pi}{18} < \omega t < \frac{12\pi}{18} \\ \frac{\pi}{54}(6+3\sqrt{3}) & \\ \quad +\frac{1}{3}[1+\sqrt{3}+(\sqrt{3}-1)k_j](\omega t - \frac{12\pi}{18}) & \frac{12\pi}{18} < \omega t < \frac{13\pi}{18} \\ \frac{\pi}{54}[7+4\sqrt{3}+(\sqrt{3}-1)k_j] & \\ \quad +\frac{1}{3}(1+\sqrt{3})(\omega t - \frac{13\pi}{18}) & \frac{13\pi}{18} < \omega t < \frac{14\pi}{18} \\ \frac{\pi}{54}[8+5\sqrt{3}+(\sqrt{3}-1)k_j] & \\ \quad +\frac{1}{3}[1+\sqrt{3}+(1-\sqrt{3})k_j](\omega t - \frac{14\pi}{18}) & \frac{14\pi}{18} < \omega t < \frac{15\pi}{18} \\ \frac{\pi}{54}(9+6\sqrt{3}) & \\ \quad +\frac{1}{3}(1+k_j)(\omega t - \frac{15\pi}{18}) & \frac{15\pi}{18} < \omega t < \frac{16\pi}{18} \\ \frac{\pi}{54}(10+6\sqrt{3}+k_j) & \\ \quad +\frac{1}{3}(\omega t - \frac{16\pi}{18}) & \frac{16\pi}{18} < \omega t < \frac{17\pi}{18} \\ \frac{\pi}{54}(11+6\sqrt{3}+k_j) & \\ \quad +\frac{1}{3}(1-k_j)(\omega t - \frac{17\pi}{18}) & \frac{17\pi}{18} < \omega t < \pi \end{cases} \tag{3.27}$$

Based on this time domain multi-slope function $f_a(\omega t)$, the output current RMS value, I_{ARMS} can be calculated,

$$I_{ARMS} = \sqrt{I_{A1RMS}^2 + \frac{1}{2\pi X_s^2}\int_0^{2\pi} f_a^2(\omega t)d\omega t - \frac{V_{A1}^2}{2X_s^2}} \tag{3.28}$$

where

$$I_{A1RMS} = \frac{V_{A1}}{\sqrt{2}X_s}\sqrt{1 + \frac{V_{sm}^2}{V_{A1}^2} - 2\frac{V_{sm}}{V_{A1}}\cos(\phi)} = \frac{V_{A1}}{\sqrt{2}X_s}k \tag{3.29}$$

and

$$\frac{1}{2\pi X_s^2}\int_0^{2\pi} f_a^2(\omega t)d\omega t = P\frac{V_{A1}^2}{2X_s^2} \tag{3.30}$$

$$P = (\frac{\pi}{18})^4 \frac{10(2-\sqrt{3})k_j^2 + 36(2+\sqrt{3})k_j + 1080 + 621\sqrt{3}}{2[1 + k_j(4\sin(\frac{\pi}{12})\cos(\frac{\pi}{36}) - 1)]^2}$$

Thus the output current RMS value, I_{ARMS} can be simplified as

$$I_{ARMS} = \frac{V_{A1}}{\sqrt{2}X_s}\sqrt{k^2 + P - 1} \tag{3.31}$$

When the reinjection transformer turns ratio is fixed at $k_j = 0.6547$ for minimum THD_V, $P-1$ is constant and equal to 1.5556×10^{-6}. The Total Harmonic Distortion of the output current (THD_I) is then:

$$THD_I = \sqrt{\frac{I_{ARMS}^2}{I_{A1RMS}^2} - 1} = \sqrt{\frac{k^2 + P - 1}{k^2} - 1} \approx 1.247 \times 10^{-3}/k \tag{3.32}$$

It is clear that the Total Harmonic Distortion of the output current is dependent on the operating conditions, i.e. the relative amplitude percentage V_{sm}/V_{A1} and phase angle difference ϕ between the output voltage fundamental and the source voltage. It is also dependent on k, which from Equation 3.29, is

$$k = I_{A1RMS} \cdot \frac{\sqrt{2}X_s}{V_{A1}} = \frac{1}{V_{A1}/V_{sm}} \cdot \frac{I_{A1RMS}}{I_{Arated}} \cdot \frac{X_s}{(V_{sm}/\sqrt{2})/I_{Arated}} \tag{3.33}$$

In equation 3.33 the rated output current I_{Arated} and the source voltage V_{sm} are set as the current and voltage base, thus the output current total harmonic distortion THD_I is related to the nominal voltage V_{A1}/V_{sm}, the nominal current I_{A1RMS}/I_{Arated} and the nominal reactance $\frac{X_s}{(V_{sm}/\sqrt{2})/I_{Arated}}$.
Based on Equation 3.21 and Equation 3.27, the output current waveforms at some specific operation conditions are plotted in Figure 3.6.

II. Analysis of the system current waveforms

Because the primary (power system side) windings of the interface transformers are connected in series, the primary winding currents are the same as the output current. Under the assumption of unit mutual coupling, the secondary (i. e. the converter side) winding currents are related to the primary side currents by the turns ratios of

the main interface transformers, i. e. $k_n : 1$ (for Y/Y) and $k_n : \sqrt{3}$ (for Y/Δ). The following expressions can be written for the converter side phase currents of the Y/Y and Y/Δ connection interface transformers:

$$\begin{aligned} I_{YY}(\omega t) &= [i_{Ya}(\omega t) \quad i_{Yb}(\omega t) \quad i_{Yc}(\omega t)]^T \\ = k_n I_o(\omega t) &= k_n[i_A(\omega t) \quad i_B(\omega t) \quad i_C(\omega t)]^T \end{aligned} \tag{3.34}$$

$$\begin{aligned} I_{Y\Delta p}(\omega t) &= [i_{\Delta ap}(\omega t) \quad i_{\Delta bp}(\omega t) \quad i_{\Delta cp}(\omega t)]^T \\ = \frac{k_n}{\sqrt{3}} I_o(\omega t) &= \frac{k_n}{\sqrt{3}}[i_A(\omega t) \quad i_B(\omega t) \quad i_C(\omega t)]^T \end{aligned} \tag{3.35}$$

and the line current vector becomes

$$\begin{aligned} I_{Y\Delta}(\omega t) &= [i_{\Delta a}(\omega t) \quad i_{\Delta b}(\omega t) \quad i_{\Delta c}(\omega t)]^T = k_n I_o(\omega t + 30^o) \\ &= k_n[i_A(\omega t + 30^o) \quad i_B(\omega t + 30^o) \quad i_C(\omega t + 30^o)]^T \end{aligned} \tag{3.36}$$

The dc side currents of these two six-pulse converters are determined by the interface transformer secondary line currents and the switching state combinations of the valves in the two main bridges. For steady operation with the time reference specified by Equation 3.16, the dc side currents can be described by the interface transformer currents and the switching functions, $f_{s\Delta}$ and f_{sY} for the Y/Y and Y/Δ connection converters respectively.

$$\mathbf{f_{sY}}(\omega t) = \begin{cases} [\ 0 & -1 & 0\ ] & 0 < \omega t < \pi/3 \\ [\ 1 & 0 & 0\ ] & \pi/3 < \omega t < 2\pi/3 \\ [\ 0 & 0 & -1\ ] & 2\pi/3 < \omega t < \pi \\ [\ 0 & 1 & 0\ ] & \pi < \omega t < 4\pi/3 \\ [-1 & 0 & 0\ ] & 4\pi/3 < \omega t < 5\pi/3 \\ [\ 0 & 0 & 1\ ] & 5\pi/3 < \omega t < 2\pi \end{cases} \tag{3.37}$$

$$\mathbf{f_{s\Delta}}(\omega t) = \begin{cases} [\ 0 & -1 & 0\ ] & 0 < \omega t < \pi/6 \\ [\ 1 & 0 & 0\ ] & \pi/6 < \omega t < 3\pi/6 \\ [\ 0 & 0 & -1\ ] & 3\pi/6 < \omega t < 5\pi/6 \\ [\ 0 & 1 & 0\ ] & 5\pi/6 < \omega t < 7\pi/6 \\ [-1 & 0 & 0\ ] & 7\pi/6 < \omega t < 9\pi/6 \\ [\ 0 & 0 & 1\ ] & 9\pi/6 < \omega t < 11\pi/6 \\ [\ 0 & -1 & 0\ ] & 11\pi/6 < \omega t < 2\pi \end{cases} \tag{3.38}$$

The dc side currents, i_{Ydc} and $i_{\Delta dc}$ are given by the expressions below.

$$i_{Ydc}(\omega t) = f_{sY}(\omega t) \cdot I_{YY}(\omega t) \tag{3.39}$$

$$i_{\Delta dc}(\omega t) = f_{s\Delta}(\omega t) \cdot I_{Y\Delta}(\omega t) \tag{3.40}$$

Under the assumption of unity mutual coupling and ignoring the small exciting component, the reinjection transformer primary current, i_j is the addition of currents, i_{Ydc} and $i_{\Delta dc}$, i.e.

$$i_j(\omega t) = k_j[i_{\Delta dc}(\omega t) - i_{Ydc}(\omega t)] \tag{3.41}$$

where k_j is the turns ratio of the reinjection transformer.

The reinjection bridge dc side current i_{jdc} is given by

$$i_{jdc}(\omega t) = f_{sj}(\omega t) \cdot i_j(\omega t) \tag{3.42}$$

where $f_{sj}(\omega t)$ is the switching state function of the reinjection bridge which operates at six times the fundamental frequency of the power system, and it is given by

$$f_{sj}(\omega t) = \begin{cases} -1 & 0 < \omega t < \pi/18 \\ 0 & \pi/18 < \omega t < 2\pi/18 \\ 1 & 2\pi/18 < \omega t < 4\pi/18 \\ 0 & 4\pi/18 < \omega t < 5\pi/18 \\ -1 & 5\pi/18 < \omega t < \pi/3 \end{cases} \tag{3.43}$$

If the converter system operates with no dc power output or absorbtion, the current through the dc capacitor i_{dc} is given by

$$i_{dc}(\omega t) = i_{Ydc}(\omega t) + i_{\Delta dc}(\omega t) + i_{jdc}(\omega t) \tag{3.44}$$

Based on the analysis discussed above the resulting reinjection system current waveforms are plotted in Figure 3.8.

3.2.4 Component Ratings

The converter system nominal apparent power rating, on the power system side of the interfacing transformer, is defined by

$$S_s = 3S = 3V_{SR}I_{SR} \tag{3.45}$$

where V_{SR} is the fundamental phase RMS voltage, and I_{SR} the fundamental phase RMS current of the converter system. The ratings of all the components in the system are derived based on the conditions that the converter is directly connected to an ideal three phase sine waveform voltage source, which RMS voltage is V_{SR}, operates under perfectly balanced conditions, and its phase current I_A has a fundamental RMS value I_{SR} (being the same as the converter system rated RMS current).

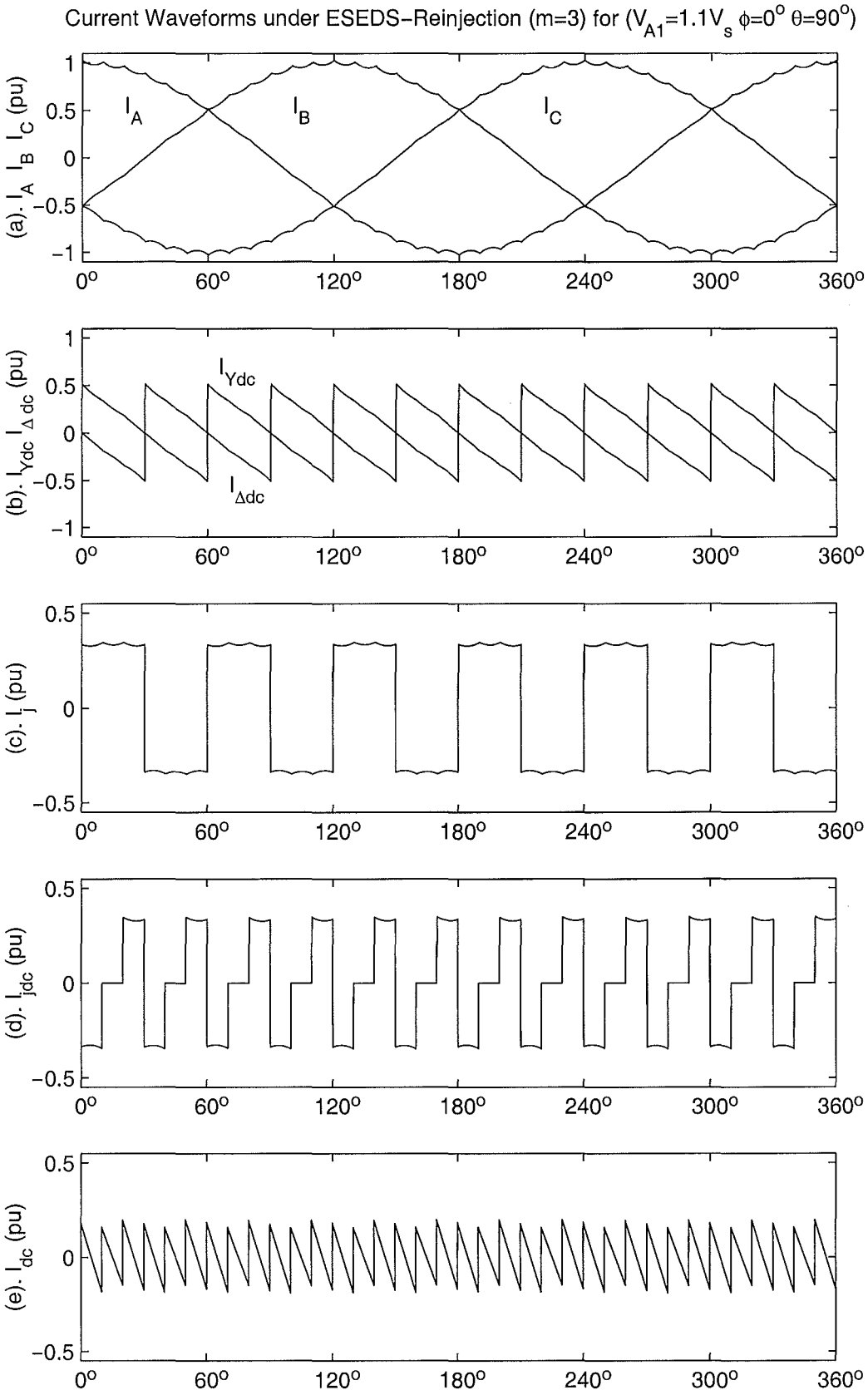


Figure 3.8 The Current Waveforms of the Parallel 3-Level ESEDS-VSC

Interface transformer

On the assumption that the interface transformer primary windings are directly connected to an ideal power system, and since the secondary windings are directly connected to the converter bridges, with the reference of the model in Figure 3.5, the converter output fundamental RMS voltage is

$$V_{Ar} = \sqrt{V_{SR}^2 + (X_s I_{SR})^2 + 2V_{SR}X_s I_{SR}\sin(\psi)} \tag{3.46}$$

where ψ is the displacement angle between the source voltage V_{SR} and current I_{SR}, and X_s is the fundamental frequency leakage reactance of the interfacing transformers. It is obvious that when $\psi = 90^o$ (namely pure capacitive operation), the converter system output voltage reaches its maximum, i. e.

$$V_{AR} = V_{SR} + X_s I_{SR} = V_{SR}(1 + \frac{X_s}{V_{SR}/I_{SR}}) = V_{SR}(1 + k_s) \tag{3.47}$$

where V_{AR} is defined as the rated phase fundamental output voltage of the converter system and k_s $(=\frac{X_s}{V_{SR}/I_{SR}})$ is the normalized fundamental reactance of the converter system seen from the terminals of the interface transformer.

The rating of the voltages across the interfacing transformer windings should include the harmonic content. Under the nominal operating conditions, the fundamental RMS voltage of each of the converter transformer is

$$U_{pfR} = 0.5V_{AR} = 0.5(1 + k_s)V_{SR} \tag{3.48}$$

the peak value of the Y/Y connection transformer

$$U_{peakY} = \frac{(1 + k_j)\pi\sqrt{2}}{6[1 + (4\sin(\frac{\pi}{12})\cos(\frac{\pi}{36}) - 1)k_j]}V_{AR} \approx 1.2006(1 + k_s)V_{SR}, \tag{3.49}$$

and the peak value of the Y/Δ connection transformer

$$U_{peak\Delta} = \frac{(1 + k_j)\pi\sqrt{2}}{4\sqrt{3}[1 + (4\sin(\frac{\pi}{12})\cos(\frac{\pi}{36}) - 1)k_j]}V_{AR} \approx 1.0398(1 + k_s)V_{SR}, \tag{3.50}$$

Both transformers have a phase voltage RMS value of

$$U_{pRMS} = \frac{\pi\sqrt{1 + 2k_j^2/3}}{6[1 + (4\sin(\frac{\pi}{12})\cos(\frac{\pi}{36}) - 1)k_j]}V_{AR} \approx 0.5818(1 + k_s)V_{SR}, \tag{3.51}$$

Although most of the harmonics are cancelled on the power system side, the converter transformers have to cope with their presence. The Total Harmonic Distortion of the

voltage across the interface transformer windings is

$$THD_U = \sqrt{\frac{\pi^2(1+2k_j^2/3)}{9[1+(4\sin(\frac{\pi}{12})\cos(\frac{\pi}{36})-1)k_j]^2} - 1} \approx 59.49\% \tag{3.52}$$

Under the nominal operating condition, the voltages of the interfacing transformer windings on the converter side can be obtained directly by multiplication by k_n^{-1} for the Y/Y transformer and $\sqrt{3}k_n^{-1}$ for the Y/Δ transformer (k_n being the turn ratio of the Y/Y transformer, and $k_n = n_p/n_c$, where n_p and n_c are the number of turns of the windings on the system and converter sides respectively).

From Equations 3.31 and 3.33, the RMS current of the primary winding under the rated operation condition is

$$I_{ARMS} = I_{SR}\sqrt{1 + 1.5556 \times 10^{-6}(1+k_s^{-1})^2} \tag{3.53}$$

The corresponding voltage and current ratings on the power system side windings are summarized in Table 3.1. All these expressions are based on the rated system voltage V_{SR} and current I_{SR}. Since each of the two interface transformer nominal VA ratings is different from $0.5V_{SR}I_{SR}$, a normalized leakage reactance k_s is defined, i.e. $k_s = X_s/(V_{SR}/I_{SR})$. Finally the symbol B in Table 3.1 is equal to $1.5556 \times 10^{-6}(1+1/k_s)^2$.

Table 3.1 Interface transformer ratings

		Y/Y connection transformer	Y/Δ connection transformer
phase voltage	peak voltage	$U_{peakY} = 1.2006(1+k_s)V_{SR}$	$U_{peak\Delta} = 1.0398(1+k_s)V_{SR}$
	RMS value	$U_{RMS} = 0.5818(1+k_s)V_{SR}$	$U_{RMS} = 0.5818(1+k_s)V_{SR}$
	funda-mental	$U_{fRMS} = 0.5(1+k_s)V_{SR}$	$U_{fRMS} = 0.5(1+k_s)V_{SR}$
phase current	RMS value	$I_{ARMS} = I_{SR}\sqrt{1+B}$	$I_{ARMS} = I_{SR}\sqrt{1+B}$
	funda-mental	$I_{AfRMS} = I_{SR}$	$I_{AfRMS} = I_{SR}$

Main switches

The GTO and Diode arm pairs in the main bridges have the same voltage ratings, the maximum voltage across each arm being

$$U_{GDm} = \frac{\pi k_n^{-1}\sqrt{2}(1+k_j)(1+k_s)}{4[1+(4\sin(\frac{\pi}{12})\cos(\frac{\pi}{36})-1)k_j]}V_{SR} \approx 1.801k_n^{-1}(1+k_s)V_{SR} \tag{3.54}$$

The current waveforms of the GTO and Diode depend on the converter system output current waveform and the firing pattern. From Equations 3.31 to 3.33, the total harmonic distortion of the converter system output current at the rated condition is:

$$THD_{IR} = \frac{\sqrt{P-1}}{k} = 1.247 \times 10^{-3} \cdot \frac{V_{A1rms}}{V_{SR}} \cdot \frac{1}{k_s} \tag{3.55}$$

and the possible maximum value of the voltage, V_{A1rms} is $(1 + k_s)V_{SR}$. Thus the maximum value of the total harmonic distortion of the converter system output current at the rated condition is:

$$THD_{IRmax} = 1.247 \times 10^{-3} \cdot \frac{1 + k_s}{k_s} \tag{3.56}$$

By choosing a sufficiently large leakage reactance, the harmonic components of the converter system output current can be kept to a very low level, e.g. $k_s \geq 0.1$, $THD_{IRmax} \leq 1.37\%$, and $I_{ARMS} \leq 1.0001 I_{SR}$. This means that the switch current rating can be derived using only the fundamental component, without introducing significant error.

Under nominal rated current operation, the GTO's and Diode's current RMS value is only dependent on the power angle θ. To derive the current ratings of the switching devices in the main bridges, it can be divided into two possible operating states, i.e. current leading the voltage and current lagging the voltage.

For the first operating state, if the converter system output current of phase A is expressed as $I_A(\omega t) = \sqrt{2} I_{SR} \sin(\omega t)$, and GTO G_{SY1} is fired in the period between $\omega t = \theta$ and $\omega t = \theta + \pi$ $(0 < \theta < \pi)$ (while GTO G_{SY4} is off during this period), the current of G_{SY1} can be expressed as

$$I_{GSY}(\omega t) = \begin{cases} 0 & 0 < \omega t < \pi \\ \sqrt{2} k_n I_{SR} \sin(\omega t - \pi) & \pi < \omega t < \pi + \theta \\ 0 & \pi + \theta < \omega t < 2\pi \end{cases} \tag{3.57}$$

and the current of Diode D_{SY1}

$$I_{DSY}(\omega t) = \begin{cases} 0 & 0 < \omega t < \theta \\ \sqrt{2} k_n I_{SR} \sin(\omega t) & \theta < \omega t < \pi \\ 0 & \pi < \omega t < 2\pi \end{cases} \tag{3.58}$$

The RMS values of $I_{GSY}(\omega t)$ and $I_{DSY}(\omega t)$ are respectively

$$I_{GSYRMS} = I_{SR} k_n \sqrt{\frac{1}{\pi} \int_{\pi}^{\pi+\theta} \sin^2(\omega t - \pi) d\omega t} = I_{SR} k_n \sqrt{\frac{1}{2\pi} [\theta - 0.5 \sin(2\theta)]} \tag{3.59}$$

and

$$I_{DSYRMS} = I_{SR}k_n\sqrt{\frac{1}{\pi}\int_{\theta}^{\pi}\sin^2(\omega t)d\omega t} = I_{SR}k_n\sqrt{\frac{1}{2}-\frac{1}{2\pi}[\theta - 0.5\sin(2\theta)]} \tag{3.60}$$

For the second operating state (i.e. the current lagging the voltage), if the converter system output current of phase A is expressed as $I_A(\omega t) = \sqrt{2}I_{SR}\sin(\omega t)$, and GTO G_{y1} is fired in the period between $\omega t = \theta$ and $\omega t = \theta + \pi$ $(-\pi < \theta < 0)$ (while GTO G_{SY4} is off during this period), the current of G_{SY1} can be expressed as

$$I_{GSY}(\omega t) = \begin{cases} -\sqrt{2}k_n I_{SR}\sin(\omega t) & \theta < \omega t < 0 \\ 0 & 0 < \omega t < 2\pi + \theta \end{cases} \tag{3.61}$$

and the current of Diode D_{SY1}

$$I_{DSY}(\omega t) = \begin{cases} 0 & \theta < \omega t < 0 \\ \sqrt{2}k_n I_{SR}\sin(\omega t) & 0 < \omega t < \pi + \theta \\ 0 & \theta + \pi < \omega t < \theta + 2\pi \end{cases} \tag{3.62}$$

The RMS values of $I_{GSY1}(\omega t)$ and $I_{DSY1}(\omega t)$ are respectively

$$I_{GSYRMS} = I_{SR}k_n\sqrt{\frac{1}{\pi}\int_{\theta}^{0}\sin^2(\omega t)d\omega t} = I_{SR}k_n\sqrt{\frac{1}{2\pi}[-\theta + 0.5\sin(2\theta)]} \tag{3.63}$$

and

$$I_{DSYRMS} = I_{SR}k_n\sqrt{\frac{1}{\pi}\int_{0}^{\theta+\pi}\sin^2(\omega t)d\omega t} = I_{SR}k_n\sqrt{\frac{1}{2}+\frac{1}{2\pi}[\theta - 0.5\sin(2\theta)]} \tag{3.64}$$

By the combination of the expressions of the two states, the GTO's and Diode's RMS currents for the full range operation $(-\pi < \theta < \pi)$ are given by:

$$I_{GSYRMS} = I_{SR}k_n\sqrt{\frac{1}{2\pi}|\theta - 0.5\sin(2\theta)|} \tag{3.65}$$

$$I_{DSYRMS} = I_{SR}k_n\sqrt{\frac{1}{2}-\frac{1}{2\pi}|\theta - 0.5\sin(2\theta)|} \tag{3.66}$$

The maximum values of the GTO's and Diode's RMS current ratings (derived from Equations 3.65 and 3.66) are

$$I_{GSYRMSmax} = I_{SR}k_n\sqrt{\tfrac{1}{2}} \quad for \quad \theta \to \pm\pi \tag{3.67}$$

$$I_{DSYRMSmax} = I_{SR}k_n\sqrt{\tfrac{1}{2}} \quad for \quad \theta \to 0 \tag{3.68}$$

Reinjection transformer

The reinjection circuitry component ratings can be derived with reference to Figures 3.4 and 3.8. Because the reinjection transformer primary winding is connected through the reinjection GTO-Diode bridge to the dc capacitor, the maximum voltage across the reinjection transformer primary winding is the maximum voltage of the dc capacitor. If the capacitance of the capacitor is large enough and the current through the capacitor is of high frequency and low amplitude, the dc capacitor voltage will have very low ripple. Then the voltage amplitude across the reinjection transformer primary winding is the rated dc capacitor voltage. The primary winding rated RMS voltage can be derived directly from the waveform of the reinjection voltage in Figure 3.4, i.e.

$$U_{jpRMS} = \frac{\pi k_n^{-1}\sqrt{3}(1+k_s)}{6[1+(4\cos(\frac{\pi}{36})\sin(\frac{\pi}{12})-1)k_j]}V_{SR} = 0.8887k_n^{-1}(1+k_s)V_{SR} \tag{3.69}$$

The maximum and rated RMS voltage of the reinjection transformer secondary windings can be obtained by multiplying those of the primary by the turns ratio $k_j(=0.6547)$.

The frequency of the reinjection current is 6 times the power source frequency. In the rated operation region a complete cycle of the current in the two secondary windings can be expressed as

$$i_{Ydc}(\omega t) = \sqrt{2}k_n I_{sR}\cos(\omega t - \pi/6 + \theta) \qquad 0 < \omega t < \pi/3 \tag{3.70}$$

and

$$i_{\Delta dc}(\omega t) = \begin{cases} \sqrt{2}k_n I_{sR}\cos(\omega t + \theta) & 0 < \omega t < \pi/6 \\ \sqrt{2}k_n I_{sR}\cos(\omega t + \theta - \pi/3) & \pi/6 < \omega t < \pi/3 \end{cases} \tag{3.71}$$

where $-\pi < \theta < \pi$ is the phase difference between the reinjection system output current and voltage fundamentals. The RMS value of these two currents is

$$I_{jsRMS} = k_n I_{sR}\sqrt{1+\frac{3\sqrt{3}}{2\pi}\cos(2\theta)} \tag{3.72}$$

It is clear that the RMS current is greatly influenced by the phase difference between the converter output phase current and voltage. The minimum value of the RMS current is $0.4159k_nI_{SR}$, while the maximum RMS value is $1.3517k_nI_{SR}$ (3.25 times higher). If the phase difference between the converter output current and voltage, θ is limited to a narrow margin, the reinjection transformer rating can be greatly reduced but the response speed of the converter system will be decreased. For instance if $|\theta \pm \pi/2| < 10^o$, the maximum RMS value of the current will be $0.4721k_nI_{SR}$, which is only 1.14 times the minimum value.

The primary winding current of the reinjection transformer

$$i_j(\omega t) = k_j[i_{Ydc}(\omega t) - i_{\Delta dc}(\omega t)] \tag{3.73}$$

can be expressed as

$$i_j(\omega t) = \begin{cases} -2\sqrt{2}k_j k_n I_{sR} \sin\frac{\pi}{12} \sin(\omega t + \theta - \pi/12) & 0 < \omega t < \pi/6 \\ 2\sqrt{2}k_j k_n I_{sR} \sin\frac{\pi}{12} \sin(\omega t + \theta - \pi/4) & \pi/6 < \omega t < \pi/3 \end{cases} \tag{3.74}$$

The RMS value of the primary winding current is

$$I_{jpRMS} = 2k_j k_n \sin\frac{\pi}{12} I_{SR}\sqrt{1 - \frac{3}{\pi}\cos(2\theta)} = 0.3389 k_n I_{SR}\sqrt{1 - 0.955\cos(2\theta)} \tag{3.75}$$

According to the expression above the primary winding current of the reinjection transformer reaches its maximum RMS value ($0.4738 k_n I_{SR}$) at the operation state ($\theta = \pm\pi/2$). The rated values of the reinjection transformer are summarized in Table 3.2.

Table 3.2 Reinjection Transformer Ratings

	Primary Winding	Secondary Windings
fundamental frequency	$F_{Reinj} = 6F_{Source}$	$F_{Reinj} = 6F_{Source}$
phase voltage peak value	$U_{jpeakP} = 1.0884 k_n^{-1}(1 + k_s)V_{SR}$	$U_{jpeakS} = 0.7126 k_n^{-1}(1 + k_s)V_{SR}$
phase voltage RMS value	$U_{jRMSp} = 0.8887 k_n^{-1}(1 + k_s)V_{SR}$	$U_{jRMSs} = 0.5818 k_n^{-1}(1 + k_s)V_{SR}$
phase current RMS value	$I_{jRMSp} = 0.3389 k_n I_{SR}\sqrt{1 - 0.955\cos 2\theta}$	$I_{jsRMS} = k_n I_{SR}\sqrt{1 + 0.827\cos 2\theta}$

Reinjection switches

As the reinjection bridge is connected directly across the dc capacitor the maximum voltage of the GTO-Diode pairs in the reinjection bridge is the same as the capacitor voltages.

$$U_{jGDm} = \frac{\sqrt{2}\pi k_n^{-1}(1 + k_s)V_{SR}}{2[1 + 2(4\sin(\frac{\pi}{12})\cos(\frac{\pi}{36}) - 1)k_j]} = 1.0884 k_n^{-1}(1 + k_s)V_{SR} \tag{3.76}$$

The currents of the GTOs and Diodes in the reinjection bridge are related to the reinjection transformer primary winding current i_j which is shown in Figure 3.8 (c). The current i_j depends on the system operating state, i.e. the amplitude of the system current and the phase angle displacement between the converter system current and voltage. Each GTO-Diode arm in the reinjection bridge conducts for 30^o every 60^o.

But the reinjection transformer primary winding current passes through the GTO or the diode depending on the actual flowing direction of the current. If the output current of the converter system leads the corresponding output voltage by an angle θ ($-\pi < \theta < \pi$), the primary winding current of the reinjection transformer can be expressed as

$$i_j(\omega t)=\begin{cases}(\sqrt{3}-1)k_j k_n I_{SR}\sin(\omega t-\pi/12) & \theta<\omega t<\theta+\pi/6\\ -(\sqrt{3}-1)k_j k_n I_{SR}\sin(\omega t-\pi/4) & \theta+\pi/6<\omega t<\theta+\pi/3\end{cases} \tag{3.77}$$

In order to obtain a 3-level voltage across the reinjection transformer primary winding, the two GTOs on the diagonal of the reinjection bridge are not fired to on-state in the same interval of 30°, but with a 20° overlap. This firing control strategy causes the currents in the GTO and Diode of the two diagonal pairs to be different according to the specific operating condition.

Because the current waveforms of the four reinjection switch pairs are the same in steady state, the GTO and diode in S_{j1} are chosen as the example for the derivation of current rating, and the GTO in S_{j1} is fired to on state in the interval $\theta+\pi/18 \le \omega t \le \theta+4\pi/18$. It is difficult to give an expression for the derivation of the current ratings of the GTO and Diode for all operation conditions. The derivation has to be performed in several different states based on the phase angle displacement between the converter output current and voltage.

(1). $-\pi < \theta < -35\pi/36$

For this case the currents through the GTO and the Diode are

$$i_{jG}(\omega t)=\begin{cases}(\sqrt{3}-1)k_j k_n I_{SR}\sin(\omega t-\pi/12) & \theta+\pi/18<\omega t<-11\pi/12\\ 0 & -11\pi/12<\omega t<\theta+\pi/3\end{cases} \tag{3.78}$$

$$i_{jD}(\omega t)=\begin{cases}0 & \theta+\pi/18<\omega t<-11\pi/12\\ (\sqrt{3}-1)k_j k_n I_{SR}\sin(\omega t-\pi/12) & -11\pi/12<\omega t<\theta+\pi/6\\ (\sqrt{3}-1)k_j k_n I_{SR}\sin(\omega t-\pi/4) & \theta+\pi/6<\omega t<\theta+2\pi/9\\ 0 & \theta+2\pi/9<\omega t<\theta+\pi/3\end{cases} \tag{3.79}$$

and the corresponding RMS currents of the GTO and the Diode are

$$I_{jGRMS}=(\sqrt{3}-1)k_j k_n I_{SR}\sqrt{\frac{3}{2\pi}[-\frac{35\pi}{36}-\theta+0.5\sin(2\theta-\frac{\pi}{18})]} \tag{3.80}$$

$$I_{jDRMS}=(\sqrt{3}-1)k_j k_n I_{SR}\sqrt{\frac{3}{2\pi}[\frac{41\pi}{36}+\theta-\sin(\frac{2\pi}{9})\sin(2\theta+\frac{2\pi}{9})]} \tag{3.81}$$

(2). $-35\pi/36 < \theta < -11\pi/12$

For this case the currents through the GTO and the Diode are

$$i_{jG}(\omega t)=\begin{cases}0 & \theta+\pi/18<\omega t<-3\pi/4\\ -(\sqrt{3}-1)k_jk_nI_{SR}\sin(\omega t-\pi/4) & -3\pi/4<\omega t<\theta+2\pi/9\\ 0 & \theta+2\pi/9<\omega t<\theta+\pi/3\end{cases} \tag{3.82}$$

$$i_{jD}(\omega t)=\begin{cases}(\sqrt{3}-1)k_jk_nI_{SR}\sin(\omega t-\pi/12) & \theta+\pi/18<\omega t<\theta+\pi/6\\ (\sqrt{3}-1)k_jk_nI_{SR}\sin(\omega t-\pi/4) & \theta+\pi/6<\omega t<-3\pi/4\\ 0 & -3\pi/4<\omega t<\theta+\pi/3\end{cases} \tag{3.83}$$

and the corresponding RMS currents of the GTO and the Diode are

$$I_{jGRMS}=(\sqrt{3}-1)k_jk_nI_{SR}\sqrt{\frac{3}{2\pi}[\frac{35\pi}{36}+\theta-0.5\sin(2\theta-\frac{\pi}{18})]} \tag{3.84}$$

$$I_{jDRMS}=(\sqrt{3}-1)k_jk_nI_{SR}\sqrt{\frac{3}{2\pi}[-\frac{29\pi}{36}-\theta-\cos(\frac{2\pi}{9})\cos(2\theta+\frac{2\pi}{9})]} \tag{3.85}$$

(3). $-11\pi/12<\theta<-\pi/12$

For this case the currents through the GTO and the Diode are

$$i_{jG}(\omega t)=\begin{cases}0 & \theta+\pi/18<\omega t<\theta+\pi/6\\ -(\sqrt{3}-1)k_jk_nI_{SR}\sin(\omega t-\pi/4) & \theta+\pi/6<\omega t<\theta+2\pi/9\\ 0 & \theta+2\pi/9<\omega t<\theta+\pi/3\end{cases} \tag{3.86}$$

$$i_{jD}(\omega t)=\begin{cases}(\sqrt{3}-1)k_jk_nI_{SR}\sin(\omega t-\pi/12) & \theta+\pi/18<\omega t<\theta+\pi/6\\ 0 & \theta+\pi/6<\omega t<\theta+\pi/3\end{cases} \tag{3.87}$$

and the corresponding RMS currents of the GTO and the Diode are

$$I_{jGRMS}=(\sqrt{3}-1)k_jk_nI_{SR}\sqrt{\frac{3}{2\pi}[\frac{\pi}{18}-\sin(\frac{\pi}{18})\cos(2\theta-\frac{\pi}{9})]} \tag{3.88}$$

$$I_{jDRMS}=(\sqrt{3}-1)k_jk_nI_{SR}\sqrt{\frac{3}{2\pi}[\frac{\pi}{9}-\sin(\frac{\pi}{9})\cos(2\theta+\frac{\pi}{18})]} \tag{3.89}$$

(4). $-\pi/12<\theta<\pi/36$

For this case the currents through the GTO and the Diode are

$$i_{jG}(\omega t)=\begin{cases}0 & \theta+\pi/18<\omega t<\pi/12\\ (\sqrt{3}-1)k_jk_nI_{SR}\sin(\omega t-\pi/12) & \pi/12<\omega t<\theta+\pi/6\\ -(\sqrt{3}-1)k_jk_nI_{SR}\sin(\omega t-\pi/4) & \theta+\pi/6<\omega t<\theta+2\pi/9\end{cases} \tag{3.90}$$

$$i_{jD}(\omega t)=\begin{cases}(\sqrt{3}-1)k_jk_nI_{SR}\sin(\omega t-\pi/12) & \theta+\pi/18<\omega t<\pi/12\\ 0 & \pi/12<\omega t<\theta+\pi/3\end{cases} \tag{3.91}$$

$$I_{jGRMS} = (\sqrt{3}-1)k_j k_n I_{SR}\sqrt{\frac{3}{2\pi}[\frac{5\pi}{36} + \theta - \sin(\frac{2\pi}{9})\sin(2\theta + \frac{2\pi}{9})]} \tag{3.92}$$

$$I_{jDRMS} = (\sqrt{3}-1)k_j k_n I_{SR}\sqrt{\frac{3}{2\pi}[\frac{\pi}{36} - \theta + 0.5\sin(2\theta - \frac{\pi}{18})]} \tag{3.93}$$

(5). $\pi/36 < \theta < \pi/12$

For this case the currents through the GTO and the Diode are

$$i_{jG}(\omega t) = \begin{cases} (\sqrt{3}-1)k_j k_n I_{SR}\sin(\omega t - \pi/12) & \theta + \pi/18 < \omega t < \theta + \pi/6 \\ -(\sqrt{3}-1)k_j k_n I_{SR}\sin(\omega t - \pi/4) & \theta + \pi/6 < \omega t < \pi/4 \\ 0 & \pi/4 < \omega t < \theta + \pi/3 \end{cases} \tag{3.94}$$

$$i_{jD}(\omega t) = \begin{cases} 0 & \theta + \pi/18 < \omega t < \pi/4 \\ -(\sqrt{3}-1)k_j k_n I_{SR}\sin(\omega t - \pi/4) & \pi/4 < \omega t < \theta + 2\pi/9 \end{cases} \tag{3.95}$$

$$I_{jGRMS} = (\sqrt{3}-1)k_j k_n I_{SR}\sqrt{\frac{3}{2\pi}[\frac{7\pi}{36} - \theta - \cos(\frac{2\pi}{9})\cos(2\theta + \frac{2\pi}{9})]} \tag{3.96}$$

$$I_{jDRMS} = (\sqrt{3}-1)k_j k_n I_{SR}\sqrt{\frac{3}{2\pi}[\theta - \frac{\pi}{36} - 0.5\sin(2\theta - \frac{\pi}{18})]} \tag{3.97}$$

(6). $\pi/12 < \theta < 11\pi/12$

For this case the currents through the GTO and the Diode are

$$i_{jG}(\omega t) = \begin{cases} (\sqrt{3}-1)k_j k_n I_{SR}\sin(\omega t - \pi/12) & \theta + \pi/18 < \omega t < \theta + \pi/6 \\ 0 & \theta + \pi/6 < \omega t < \theta + \pi/3 \end{cases} \tag{3.98}$$

$$i_{jD}(\omega t) = \begin{cases} 0 & \theta + \pi/18 < \omega t < \theta + \pi/6 \\ -(\sqrt{3}-1)k_j k_n I_{SR}\sin(\omega t - \pi/4) & \theta + \pi/6 < \omega t < \theta + 2\pi/9 \end{cases} \tag{3.99}$$

$$I_{jGRMS} = (\sqrt{3}-1)k_j k_n I_{SR}\sqrt{\frac{3}{2\pi}[\frac{\pi}{9} - \sin(\frac{\pi}{9})\cos(2\theta + \frac{\pi}{18})]} \tag{3.100}$$

$$I_{jDRMS} = (\sqrt{3}-1)k_j k_n I_{SR}\sqrt{\frac{3}{2\pi}[\frac{\pi}{18} - \sin(\frac{\pi}{18})\cos(2\theta - \frac{\pi}{9})]} \tag{3.101}$$

(7). $11\pi/12 < \theta < \pi$

For this case the currents through the GTO and the Diode are

$$i_{jG}(\omega t) = \begin{cases} (\sqrt{3}-1)k_j k_n I_{SR}\sin(\omega t - \pi/12) & \theta + \pi/18 < \omega t < 13\pi/12 \\ 0 & 13\pi/12 < \omega t < \theta + \pi/3 \end{cases} \tag{3.102}$$

$$i_{jD}(\omega t) = \begin{cases} (\sqrt{3}-1)k_j k_n I_{SR}\sin(\omega t - \pi/12) & 13\pi/12 < \omega t < \theta + \pi/6 \\ -(\sqrt{3}-1)k_j k_n I_{SR}\sin(\omega t - \pi/4) & \theta + \pi/6 < \omega t < \theta + 2\pi/9 \end{cases} \tag{3.103}$$

$$I_{jGRMS} = (\sqrt{3}-1)k_j k_n I_{SR}\sqrt{\frac{3}{2\pi}[\frac{37\pi}{36} - \theta + 0.5\sin(2\theta - \frac{\pi}{18})]} \tag{3.104}$$

$$I_{jDRMS} = (\sqrt{3}-1)k_j k_n I_{SR}\sqrt{\frac{3}{2\pi}[\theta - \frac{31\pi}{36} - \sin(\frac{2\pi}{9})\sin(2\theta + \frac{2\pi}{9})]} \tag{3.105}$$

Based on the RMS current expressions described above, it is clear that the RMS current ratings of the GTOs and Diodes in the reinjection bridge are related to the operatng condition of the output current amplitude and the phase angle displacement between the output current and voltage.

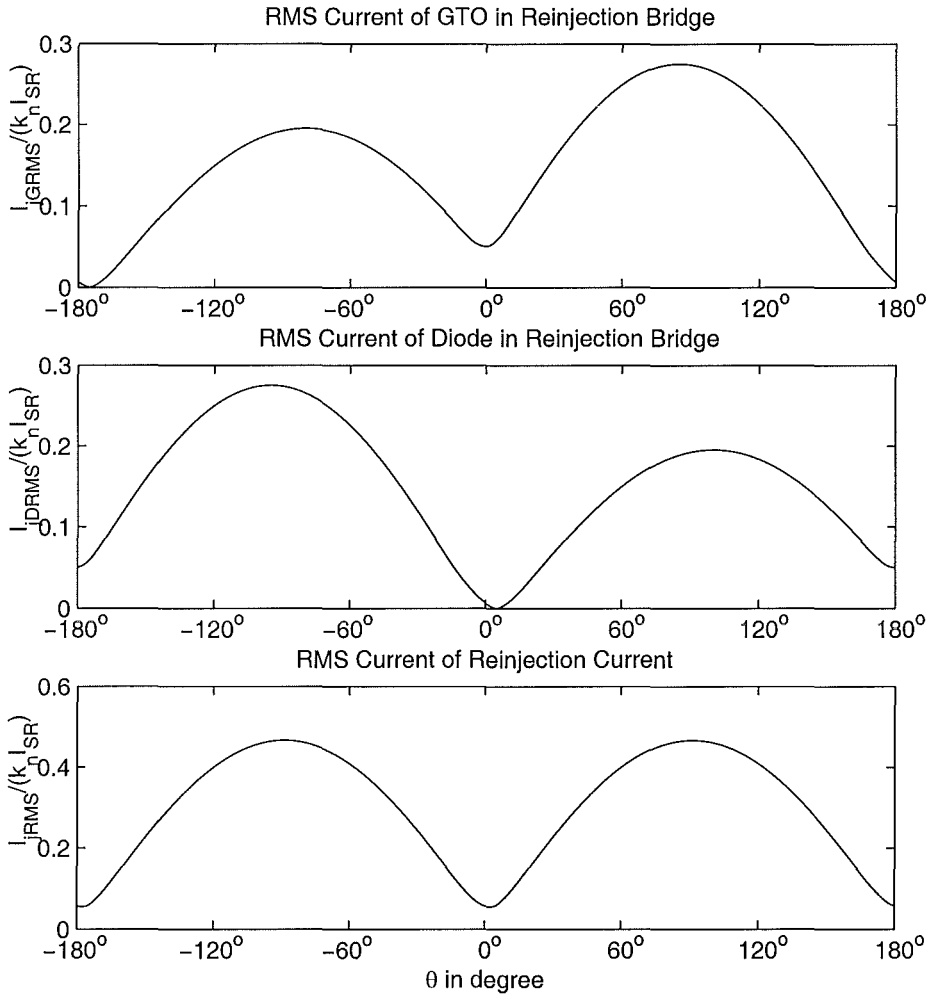


Figure 3.9 The Reinjection Switch RMS Current Versus Power Angle

Figure 3.9 shows the variation of $I_{jGRMS}/(k_n I_{SR})$, $I_{jDRMS}/(k_n I_{SR})$ and the reinjection RMS current with θ. The curves show that the RMS currents of the GTO and Diode in the reinjection bridge under the nominal operating condition vary with the converter power factor. A higher power factor results in lower RMS current in the reinjection bridge. The maximum RMS current for the reinjection GTO and Diode is

$$I_{jGDRMSmax} = (\sqrt{3}-1)k_j k_n I_{SR}\sqrt{\frac{3}{2\pi}\left[\frac{\pi}{9} + \sin(\frac{\pi}{9})\right]} = 0.275 k_n I_{SR} \tag{3.106}$$

These maximums take place at the operating conditions: $\theta = \frac{17\pi}{36}$ and $\theta = -\frac{19\pi}{36}$ for

the GTO and Diode respectively, while the minimum RMS current for the reinjection GTO and Diode is zero at the operation conditions: $\theta = -\frac{35\pi}{36}$ and $\theta = \frac{\pi}{36}$ respectively.

D.C. side capacitance

Referring to equations 3.2 to 3.4, equations 3.5 to 3.7 and equations 3.9 to 3.121, the rated dc average voltage of the dc capacitor is

$$U_{dcR} = \frac{\sqrt{2}\pi k_n^{-1}}{4[1 + (4\sin(\frac{\pi}{12})\cos(\frac{\pi}{36}) - 1)k_j]} V_{AR} = 1.0884 k_n^{-1}(1 + k_s)V_{SR} \tag{3.107}$$

where k_n is the turns ratio of the interfacing transformers ($k_n : 1$ for Y/Y transformer and $k_n : \sqrt{3}$ for Y/Δ transformer).

As the analysis is based on a constant capacitor voltage, the dc capacitor must be sufficiently large to ensure that the capacitor voltage ripple is within acceptable limits to suppress harmonics caused by the capacitor voltage fluctuation. The dc capacitor voltage ripple is determined by the capacitor current of the stable operating state (i.e. without dc component current). For a 12-pulse convertor, if the output current of the converter system is an ideal sine wave, ($\sqrt{2}I_{sR}\sin\omega t$), the full cycle stable state current of the dc capacitor is

$$i_{c12}(\omega t) = 2\sqrt{2}k_n I_{SR}\cos(\frac{\pi}{12})\sin(\omega t - \frac{\pi}{12}) \qquad 0 < \omega t < \pi/6 \tag{3.108}$$

Then the capacitor ripple voltage can be expressed as

$$\begin{aligned} v_{c12rp}(\omega t) &= \frac{1}{\omega C_{12}}\int_0^{\omega t} i_{c12}(\omega t)d\omega t \\ &= \frac{2\sqrt{2}k_n I_{SR}}{\omega C_{12}}\cos(\frac{\pi}{12})\Big[\cos(\frac{\pi}{12}) - \cos(\omega t - \frac{\pi}{12})\Big] \qquad 0 < \omega t < \pi/6 \end{aligned} \tag{3.109}$$

and the peak to peak value of the ripple voltage is

$$\begin{aligned} V_{ppr12} &= \frac{2\sqrt{2}k_n I_{SR}}{\omega C_{12}}\cos(\frac{\pi}{12})\Big[1 - \cos(\frac{\pi}{12})\Big] \\ &\approx \frac{9.31 \times 10^{-2} k_n I_{SR}}{\omega C_{12}} \end{aligned} \tag{3.110}$$

For the reinjection system the full cycle stable current of the dc capacitor is given by

$$i_{dc}(\omega t) = \begin{cases} \sqrt{2}k_n I_{SR}[(1 - k_j)\sin(\omega t - \frac{\pi}{6}) & \\ \quad +(1 + k_j)\sin(\omega t)] & 0 < \omega t < \frac{\pi}{18} \\ 2\sqrt{2}k_n I_{SR}\cos\frac{\pi}{12}\sin(\omega t - \frac{\pi}{12}) & \frac{\pi}{18} < \omega t < \frac{\pi}{9} \\ \sqrt{2}k_n I_{SR}[(1 + k_j)\sin(\omega t - \frac{\pi}{12}) & \\ \quad +(1 - k_j)\sin(\omega t)] & \frac{\pi}{9} < \omega t < \frac{\pi}{6} \end{cases} \tag{3.111}$$

The dc capacitor ripple voltage of the reinjection system can be obtained by integration of the current, i.e.

$$v_{dc}(\omega t) = \begin{cases} \frac{\sqrt{2}k_n I_{SR}}{\omega C}[(1-k_j)(\cos\frac{\pi}{6} - \cos(\omega t - \frac{\pi}{6})) \\ \quad +(1+k_j)(1-\cos\omega t)] + v_{dc}(0) & 0 < \omega t < \frac{\pi}{18} \\ \frac{2\sqrt{2}k_n I_{SR}}{\omega C}\cos\frac{\pi}{12}[\cos\frac{\pi}{36} \\ \quad -\cos(\omega t - \frac{\pi}{12})] + v_{dc}(\frac{\pi}{18}) & \frac{\pi}{18} < \omega t < \frac{\pi}{9} \\ \frac{\sqrt{2}k_n I_{SR}}{\omega C}[(1+k_j)(\cos\frac{\pi}{18} - \cos(\omega t - \frac{\pi}{6})) \\ \quad +(1-k_j)(\cos(\pi/9) - \cos\omega t)] + v_{dc}(\frac{\pi}{9}) & \frac{\pi}{9} < \omega t < \frac{\pi}{6} \end{cases} \tag{3.112}$$

The peak to peak ripple voltage of the reinjection system, V_{ppR}, can be derived from the equation above, and is given by

$$V_{ppR} = \frac{2\sqrt{2}k_n I_{SR}}{\omega C}\cos(\frac{\pi}{12})\left[1-\cos(\frac{\pi}{36})\right] \approx \frac{1.04\times 10^{-2}k_n I_{SR}}{\omega C} \tag{3.113}$$

And thus $V_{ppr12}/V_{ppR} \approx 8.95$, which means that the reinjection system can use a greatly reduced size capacitor for the same ripple amplitude.

3.3 THE SERIES CONNECTED BRIDGE SCHEME

3.3.1 Operating Principle

Figure 3.10 shows the reinjection voltage source converter system, in which the two main bridges are connected in series to obtain higher dc output. The series connected bridge scheme possesses the advantage that the output dc current does not pass through the reinjection components. This is achieved by connecting the reinjection transformer secondary winding between the bridge neutral and the common node of the two dc capacitors in series.

With reference to Figure 3.10 the voltages across the two main YY and $Y\Delta$ connected bridges, are respectively:

$$V_{YY} = U_{CY} + u_j$$

$$V_{Y\Delta} = U_{C\Delta} - u_j$$

If the dc capacitor voltages are the same ($U_{CY} = U_{C\Delta} = U_C$) and equal to the dc capacitor voltage U_{dc} in Figure 3.1, the output voltage waveforms of the two main bridges are the same as those of the waveforms of the configuration in Figure 3.1. The operating principle of the series connected bridge scheme is the same as the parallel connected bridge scheme, except that the reinjection components do not carry the dc current component of the main bridges, and that the reinjection bridge has to withstand twice the voltage $2U_C$. Therefore the analysis of the series connected bridge scheme can be simplified.

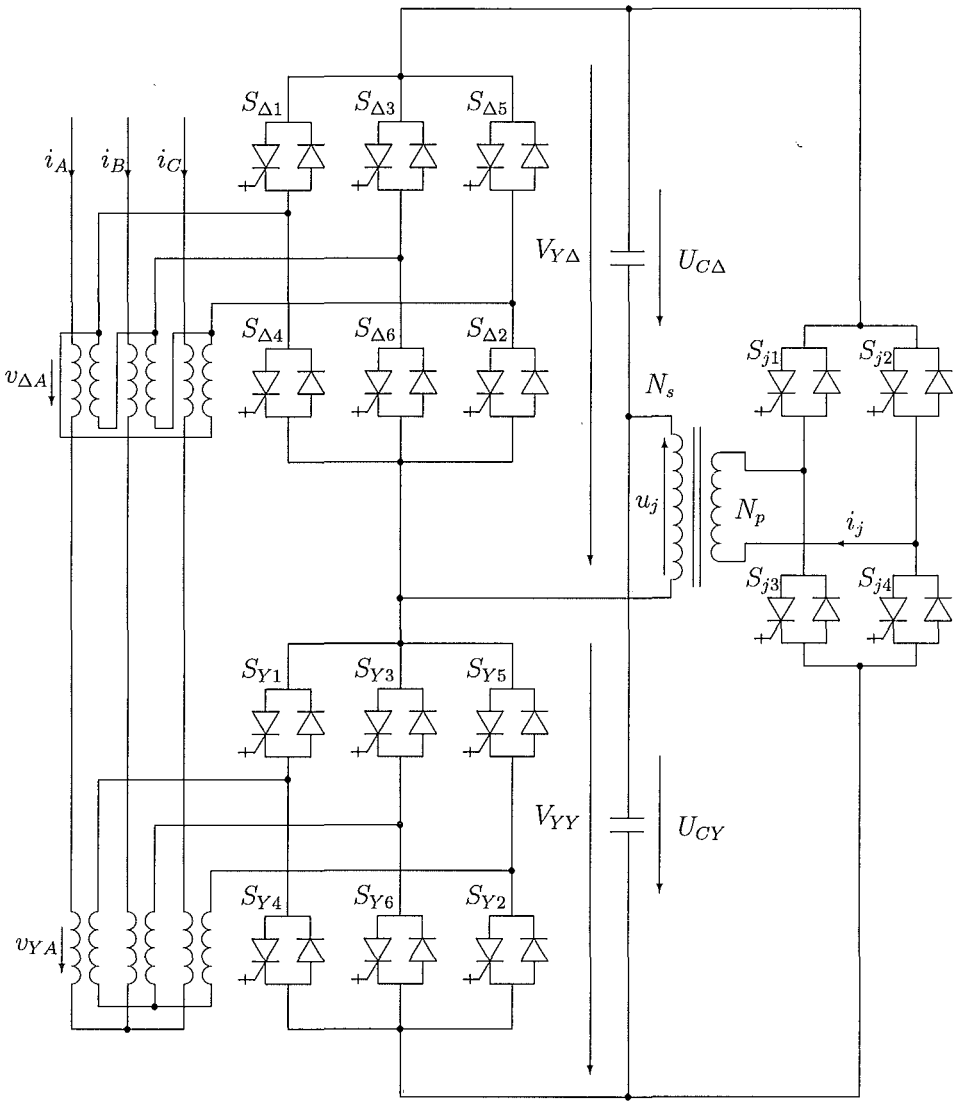


Figure 3.10 The Series 3-Level ESEDS reinjection VSC

3.3.2 Analysis of the Voltage Waveforms

By using the same trigger pattern shown in Figure 3.2 the $Y\Delta$ connected bridge produce the phase output voltage

$$V_{\Delta a}(\omega t) = \sum_{n=1}^{\infty} V_{\Delta an} U_{C\Delta} \sin(n\omega t) \tag{3.114}$$

where

$$V_{\Delta an} = \frac{2[1-(-1)^n]}{n\pi}\left\{1 + 2k_j\left[8\sin(\frac{n\pi}{6})\sin(\frac{n\pi}{12})\cos(\frac{n\pi}{36}) - 1\right]\right\}\cos(\frac{n\pi}{6}) \quad for \quad n = 1, 2, 3, \cdots \tag{3.115}$$

The YY connected bridge produce the phase output voltage

$$V_{Ya}(\omega t) = \sum_{n=1}^{\infty} V_{Yan} U_{CY} \sin(n\omega t) \qquad for \quad n = 1, 2, 3, \cdots \tag{3.116}$$

where

$$V_{Yan} = \frac{4[1-(-1)^n]}{3n\pi}\Big\{1 + 2k_j\Big[8\sin(\frac{n\pi}{6})\sin(\frac{n\pi}{12})\cos(\frac{n\pi}{36}) - 1\Big]\Big\}\cos^2(\frac{n\pi}{6}) \qquad for \quad n = 1, 2, 3, \cdots \tag{3.117}$$

The output (or primary side) ac voltage, V_A, is the sum of $v_{Ya}(\omega t)$ and $v_{\Delta a}(\omega t)$, namely

$$V_A = k_n[V_{Ya}(\omega t) + \frac{1}{\sqrt{3}} V_{\Delta a}(\omega t)] \tag{3.118}$$

where k_n is the Y/Y interface transformer turns ratio, and the half cycle levels of the output phase voltage are:

$$\frac{V_A}{k_n U_C} = \begin{cases} (1-2k_j)/3 & 0^o < \omega t < 10^o \\ 1/3 & 10^o < \omega t < 20^o \\ (1+2k_j)/3 & 20^o < \omega t < 30^o \\ (1+2k_j)/3 + (1-2k_j)/\sqrt{3} & 30^o < \omega t < 40^o \\ 1/3 + 1/\sqrt{3} & 40^o < \omega t < 50^o \\ (1-2k_j)/3 + (1+2k_j)/\sqrt{3} & 50^o < \omega t < 60^o \\ 2(1-2k_j)/3 + (1+2k_j)/\sqrt{3} & 60^o < \omega t < 70^o \\ 2/3 + 1/\sqrt{3} & 70^o < \omega t < 80^o \\ 2(1+2k_j)/3 + (1-2k_j)/\sqrt{3} & 80^o < \omega t < 100^o \\ 2/3 + 1/\sqrt{3} & 100^o < \omega t < 110^o \\ 2(1-2k_j)/3 + (1+2k_j)/\sqrt{3} & 110^o < \omega t < 120^o \\ (1-2k_j)/3 + (1+2k_j)/\sqrt{3} & 120^o < \omega t < 130^o \\ 1/3 + 1/\sqrt{3} & 130^o < \omega t < 140^o \\ (1+2k_j)/3 + (1-2k_j)/\sqrt{3} & 140^o < \omega t < 150^o \\ (1+2k_j)/3 & 150^o < \omega t < 160^o \\ 1/3 & 160^o < \omega t < 170^o \\ (1-2k_j)/3 & 170^o < \omega t < 180^o \end{cases} \tag{3.119}$$

The total RMS value of the output phase voltage is given by the expression

$$V_{ARMS} = \frac{k_n U_C}{9}\sqrt{36 + 18\sqrt{3} + 4(24 - 12\sqrt{3})k_j^2} \tag{3.120}$$

the peak level of its fundamental component being:

$$V_{A1} = \frac{4k_n U_C}{\pi}\Big[1 + 2\Big(4\cos(\frac{\pi}{36})\sin(\frac{\pi}{12}) - 1\Big)k_j\Big] \tag{3.121}$$

and the peak level of its n^{th} harmonic component:

$$V_{An} = k_n U_C (V_{Yan} + \frac{V_{\Delta an}}{\sqrt{3}}) = k_n U_C \Big[1 + \frac{2}{\sqrt{3}} \cos(\frac{n\pi}{6})\Big] \frac{V_{\Delta an}}{\sqrt{3}} \qquad n = 1, 2, \cdots \quad (3.122)$$

It is obvious that

$$V_{An} = \begin{cases} 0 & n \neq 12k \pm 1, k = 1, 2, \cdots \\ \frac{4k_n U_C}{n\pi}\{1 + 2k_j[\frac{4(-1)^k}{\sqrt{6}+\sqrt{2}} \cos(\frac{n\pi}{36}) - 1]\} & n = 12k \pm 1, k = 1, 2, \cdots \end{cases} \quad (3.123)$$

The total harmonic distortion of the phase output voltage, THD_V, is given by

$$THD_V = \sqrt{\frac{2V_{ARMS}^2}{V_{A1}^2} - 1} \quad (3.124)$$

and the reinjection transformer turns ratio required to minimize the total harmonic distortion is

$$k_j = (\frac{21}{4} + 3\sqrt{3})\Big(4\cos(\frac{\pi}{36})\sin(\frac{\pi}{12}) - 1\Big) \approx 0.3273 \quad (3.125)$$

which is half of that of the previous scheme, and produces the same minimum output voltage THD, i.e.

$$THD_{Vmin} = 5.09\%. \quad (3.126)$$

The reinjection voltage, the voltages across the two main bridges, the two bridge and the converter system output output voltage waveforms are shown in Figure 3.11.

3.3.3 Analysis of the Current Waveforms

The output current can be obtained directly from the results of the previous analysis, because the two converters are connected to voltage sources with the same characteristics and they produce the same voltage at the interface transformers.

As the reinjection components are connected in a different way from the previous scheme, some of the current waveforms of the converter system need to be analyzed in detail.

The ac side currents of the two main bridges are the same as in the previous scheme, and the Y/Y connected interface transformer line currents are given by

$$\begin{aligned} I_{YY}(\omega t) &= [i_{Ya}(\omega t) \quad i_{Yb}(\omega t) \quad i_{Yc}(\omega t)]^T \\ = k_n I_O(\omega t) &= k_n[i_a(\omega t) \quad i_b(\omega t) \quad i_c(\omega t)]^T \end{aligned} \quad (3.127)$$

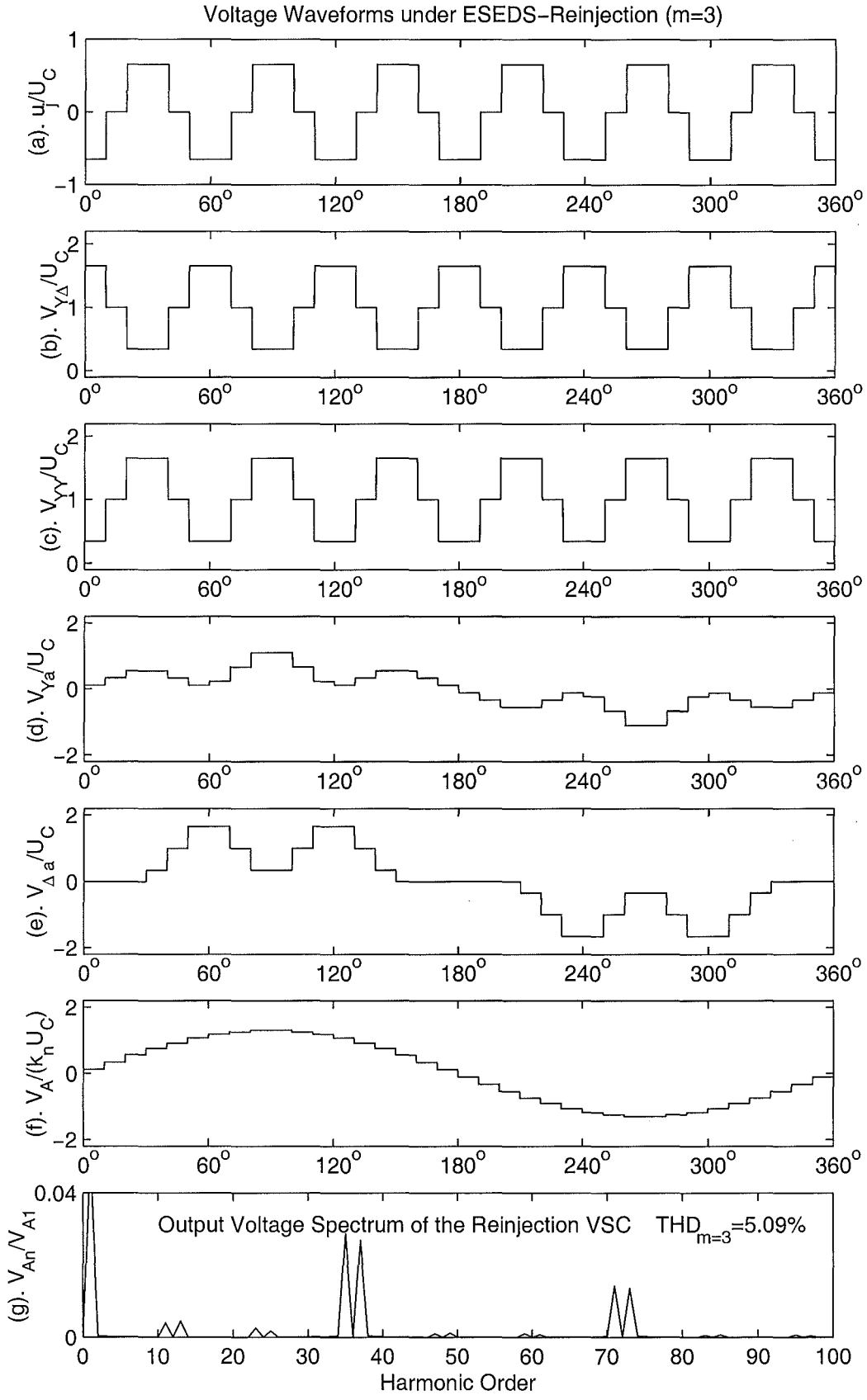


Figure 3.11 The Voltage Waveforms of the Series 3-Level ESEDS-VSC

and the Y/Δ connected interface transformer line currents are given by

$$\begin{aligned} I_{Y\Delta}(\omega t) &= [i_{\Delta a}(\omega t) \quad i_{\Delta b}(\omega t) \quad i_{\Delta c}(\omega t)]^T = k_n I_O(\omega t + 30^o) \\ &= k_n[i_A(\omega t + 30^o) \quad i_B(\omega t + 30^o) \quad i_C(\omega t + 30^o)]^T \end{aligned} \tag{3.128}$$

The dc side currents of these two six-pulse converters are determined by the interface transformer secondary currents and the switching state combinations of the converter valves. For steady operation the dc side currents can be described by the interface transformer currents and the switching functions, $f_{s\Delta}$ and f_{sY} for Y/Y and Y/Δ connection converters respectively.

$$f_{sY}(\omega t) = \begin{cases} [\ 0 \quad -1 \quad 0\ ] & 0 < \omega t < \pi/3 \\ [\ 1 \quad 0 \quad 0\ ] & \pi/3 < \omega t < 2\pi/3 \\ [\ 0 \quad 0 \quad -1\ ] & 2\pi/3 < \omega t < \pi \\ [\ 0 \quad 1 \quad 0\ ] & \pi < \omega t < 4\pi/3 \\ [-1 \quad 0 \quad 0\ ] & 4\pi/3 < \omega t < 5\pi/3 \\ [\ 0 \quad 0 \quad 1\ ] & 5\pi/3 < \omega t < 2\pi \end{cases} \tag{3.129}$$

$$f_{s\Delta}(\omega t) = \begin{cases} [\ 0 \quad -1 \quad 0\ ] & 0 < \omega t < \pi/6 \\ [\ 1 \quad 0 \quad 0\ ] & \pi/6 < \omega t < 3\pi/6 \\ [\ 0 \quad 0 \quad -1\ ] & 3\pi/6 < \omega t < 5\pi/6 \\ [\ 0 \quad 1 \quad 0\ ] & 5\pi/6 < \omega t < 7\pi/6 \\ [-1 \quad 0 \quad 0\ ] & 7\pi/6 < \omega t < 9\pi/6 \\ [\ 0 \quad 0 \quad 1\ ] & 9\pi/6 < \omega t < 11\pi/6 \\ [\ 0 \quad -1 \quad 0\ ] & 11\pi/6 < \omega t < 2\pi \end{cases} \tag{3.130}$$

The dc side currents, i_{Ydc} and $i_{\Delta dc}$ are given by

$$i_{Ydc}(\omega t) = f_{sY}(\omega t) \cdot I_{YY}(\omega t) \tag{3.131}$$

$$i_{\Delta dc}(\omega t) = f_{s\Delta}(\omega t) \cdot I_{Y\Delta}(\omega t) \tag{3.132}$$

The reinjection transformer primary current, i_j is the addition of currents i_{Ydc} and $i_{\Delta dc}$, i.e.

$$i_j(\omega t) = k_j[i_{\Delta dc}(\omega t) - i_{Ydc}(\omega t)] \tag{3.133}$$

where $k_j = 0.3273$ is the turns ratio of the reinjection transformer.

The reinjection bridge dc side current i_{jdc} is given by

$$i_{jdc}(\omega t) = f_{sj}(\omega t) \cdot i_j(\omega t) \tag{3.134}$$

where $f_{sj}(\omega t)$ is the switching state function of the reinjection bridge, which operates

at six times the fundamental frequency of the power system, and is given by

$$f_{sj}(\omega t) = \begin{cases} -1 & 0 < \omega t < \pi/18 \\ 0 & \pi/18 < \omega t < 2\pi/18 \\ 1 & 2\pi/18 < \omega t < 4\pi/18 \\ 0 & 4\pi/18 < \omega t < 5\pi/18 \\ -1 & 5\pi/18 < \omega t < \pi/3 \end{cases} \tag{3.135}$$

With reference to Figure 3.10, the current through the dc capacitor i_{cy} is given by

$$i_{cy}(\omega t) = i_{Ydc}(\omega t) + i_{jdc}(\omega t) \tag{3.136}$$

Based on the analysis discussed above the resulting reinjection system current waveforms are shown in Figure 3.12.

3.3.4 Component Ratings

Most of the components ratings can be directly obtained from the previous results, therefore, only those that are different will be discussed in detail.

The calculations are based on the same nominal fundamental apparent power rating

$$S_s = 3S = 3V_{SR}I_{SR}$$

Interface transformers

The interface transformers have the same ratings as before and, therefore, the summarizing table is repeated here.

Table 3.3 Interface transformer ratings

		Y/Y connection transformer	Y/Δ connection transformer
phase voltage	peak voltage	$U_{peakY} = 1.2006(1+k_s)V_{SR}$	$U_{peak\Delta} = 1.0398(1+k_s)V_{SR}$
	RMS value	$U_{RMS} = 0.5818(1+k_s)V_{SR}$	$U_{RMS} = 0.5818(1+k_s)V_{SR}$
	funda-mental	$U_{fRMS} = 0.5(1+k_s)V_{SR}$	$U_{fRMS} = 0.5(1+k_s)V_{SR}$
phase current	RMS value	$I_{ARMS} = I_{SR}\sqrt{1+B}$	$I_{ARMS} = I_{SR}\sqrt{1+B}$
	funda-mental	$I_{AfRMS} = I_{SR}$	$I_{AfRMS} = I_{SR}$

where in Table 3.3 $k_s = X_s/(V_{SR}/I_{SR})$ and $B = 1.5556 \times 10^{-6}(1+1/k_s)^2$.

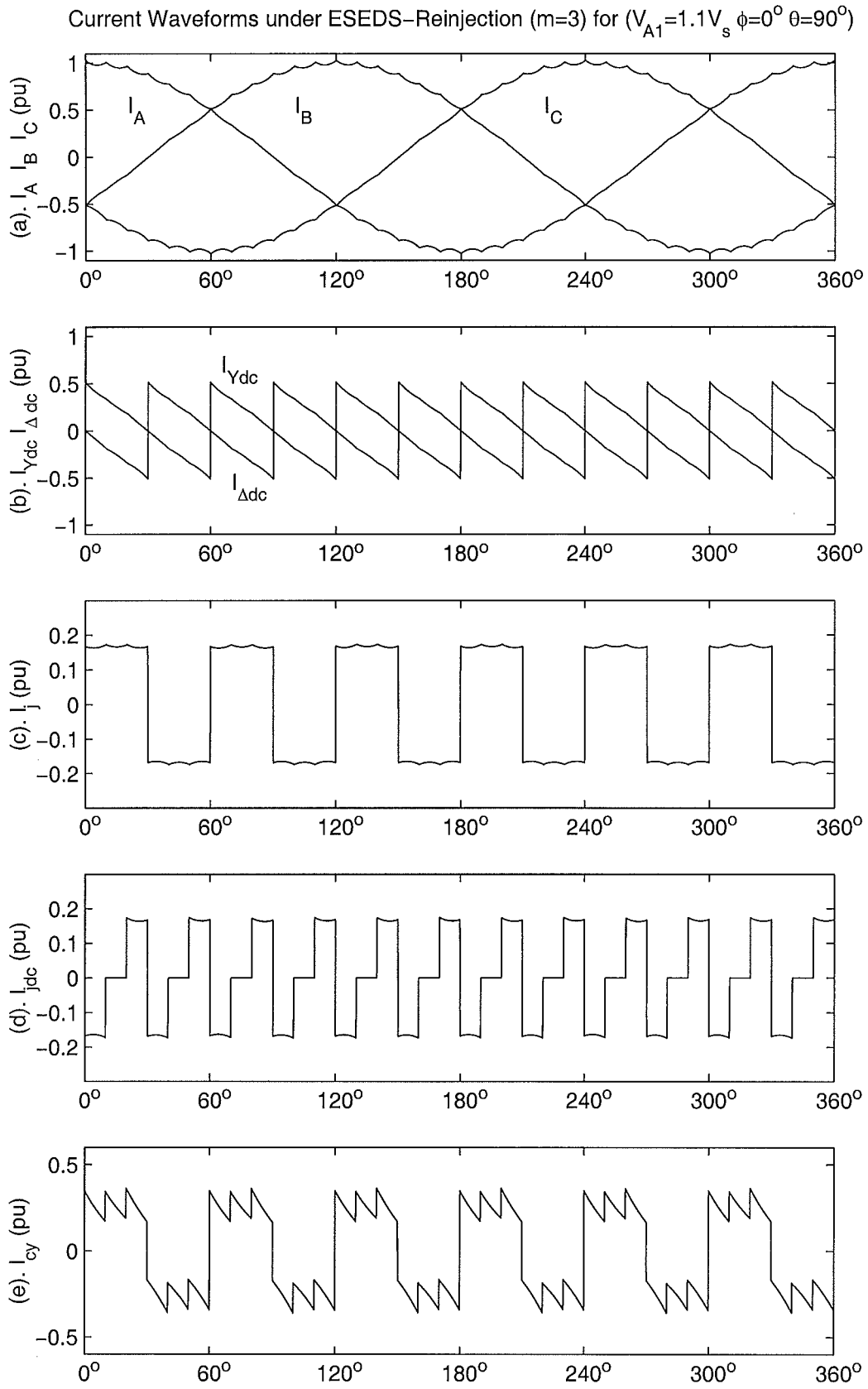


Figure 3.12 The Current Waveforms of the Series 3-Level ESEDS-VSC

Main switches

The main switches have the same voltage ratings, the maximum voltage across each arm being

$$U_{GDm} = \frac{\pi k_n^{-1}\sqrt{2}(1+k_j)(1+k_s)}{4[1+(4\sin(\frac{\pi}{12})\cos(\frac{\pi}{36})-1)k_j]}V_{SR} \approx 1.801k_n^{-1}(1+k_s)V_{SR} \tag{3.137}$$

The current ratings are related to the power angle θ. The GTO's and Diode's RMS currents for the full range of operation ($-\pi < \theta < \pi$) are given by:

$$I_{GSYRMS} = I_{SR}k_n\sqrt{\frac{1}{2\pi}|\theta - 0.5\sin(2\theta)|} \tag{3.138}$$

and

$$I_{DSYRMS} = I_{SR}k_n\sqrt{\frac{1}{2} - \frac{1}{2\pi}|\theta - 0.5\sin(2\theta)|} \tag{3.139}$$

Reinjection transformer

The reinjection transformer has lower current ratings compared with the previous scheme, because now the windings currents do not have a dc component.

Because the reinjection transformer primary winding is connected through the reinjection GTO-Diode bridge to the dc capacitors, the maximum voltage across the reinjection transformer primary winding is the sum of the voltage of the two dc capacitors. If the capacitance of the two dc capacitors is large enough the voltage amplitude across the reinjection transformer primary winding is the sum of the two capacitor dc average voltages.

$$U_{jpeakP} = 2U_C = \frac{\pi k_n^{-1}\sqrt{2}V_{AR}}{2[1+2(4\cos(\frac{\pi}{36})\sin(\frac{\pi}{12})-1)k_j]} = 2.1768k_n^{-1}(1+k_s)V_{SR} \tag{3.140}$$

The primary winding rated RMS voltage can be derived from the waveform of the reinjection voltage in Figure 3.11 (a), i.e.

$$U_{jpRMS} = \frac{\pi k_n^{-1}\sqrt{3}(1+k_s)V_{SR}}{3[1+(4\cos(\frac{\pi}{36})\sin(\frac{\pi}{12})-1)k_j]} = 1.7773k_n^{-1}(1+k_s)V_{SR} \tag{3.141}$$

The peak and rated RMS voltage of the reinjection transformer secondary windings can be obtained by multiplying those of the primary by the turns ratio $k_j(= 0.3273)$.

The frequency of the reinjection current is 6 times the power frequency. Under nominal operation conditions a complete cycle of the current in the secondary winding of the reinjection transformer can be expressed as

$$i_{js} = i_{\Delta dc}(\omega t) - i_{Ydc}(\omega t) \tag{3.142}$$

The dc output currents of the two bridges $i_{Ydc}(\omega t)$ and $i_{\Delta dc}(\omega t)$ are given by

$$i_{Ydc}(\omega t) = \sqrt{2}k_n I_{SR}\cos(\omega t - \pi/6 + \theta) \qquad 0 < \omega t < \pi/3 \tag{3.143}$$

and

$$i_{\Delta dc}(\omega t) = \begin{cases} \sqrt{2}k_n I_{SR}\cos(\omega t + \theta) & 0 < \omega t < \pi/6 \\ \sqrt{2}k_n I_{SR}\cos(\omega t + \theta - \pi/3) & \pi/6 < \omega t < \pi/3 \end{cases} \tag{3.144}$$

where $-\pi < \theta < \pi$ is the phase difference between the fundamental components of the reinjection system output current and voltage. By substituting the expressions of i_{Ydc} and $i_{\Delta dc}$ into i_{js}, the reinjection transformer secondary winding current becomes

$$i_{js}(\omega t) = \begin{cases} -2\sqrt{2}k_n I_{SR}\sin(\frac{\pi}{12})\sin(\omega t + \theta - \pi/12) & 0 < \omega t < \pi/6 \\ 2\sqrt{2}k_n I_{SR}\sin(\frac{\pi}{12})\sin(\omega t + \theta - \pi/4) & \pi/6 < \omega t < \pi/3 \end{cases} \tag{3.145}$$

The RMS value of this current is

$$I_{jsRMS} = 2k_n I_{SR}\sin\frac{\pi}{12}\sqrt{1 - \frac{3}{\pi}\cos(2\theta)} \tag{3.146}$$

The minimum value of the RMS current is $0.1099k_n I_{SR}$ and its maximum $0.7237k_n I_{sR}$ (6.5856 times higher). The minimum RMS value corresponds to the operation of unity power factor. The maximum RMS value corresponds to the operation of zero power factor, i.e. a higher power factor results in a lower reinjection current.

The primary winding current of the reinjection transformer is obtained by multiplying the secondary current by the turns ratio of the reinjection transformer k_j.

The rated values of the reinjection transformer are summarized in Table 3.4.

Table 3.4 Reinjection Transformer Ratings

	Primary Winding	Secondary Windings
fundamental frequency	$F_{Reinj} = 6F_{Source}$	$F_{Reinj} = 6F_{Source}$
phase voltage peak value	$U_{jpeakP} = 2.1768k_n^{-1}(1 + k_s)V_{sR}$	$U_{jpeakS} = 0.7126k_n^{-1}(1 + k_s)V_{sR}$
phase voltage RMS value	$U_{jpRMS} = 1.7773k_n^{-1}(1 + k_s)V_{sR}$	$U_{jRMSs} = 0.5818k_n^{-1}(1 + k_s)V_{sR}$
phase current RMS value	I_{jpRMS} $= 0.1694k_n I_{sR}\sqrt{1 - 0.955\cos 2\theta}$	I_{jsRMS} $= 0.5176k_n I_{sR}\sqrt{1 - 0.955\cos 2\theta}$

Reinjection switches

The reinjection switch voltage rating is twice that of the previous scheme, and the current rating is half of the previous scheme. The RMS current ratings of the GTO's and diodes depend on the power angle θ. Figure 3.13 shows the relations between I_{jGRMS}, I_{jDRMS} and θ.

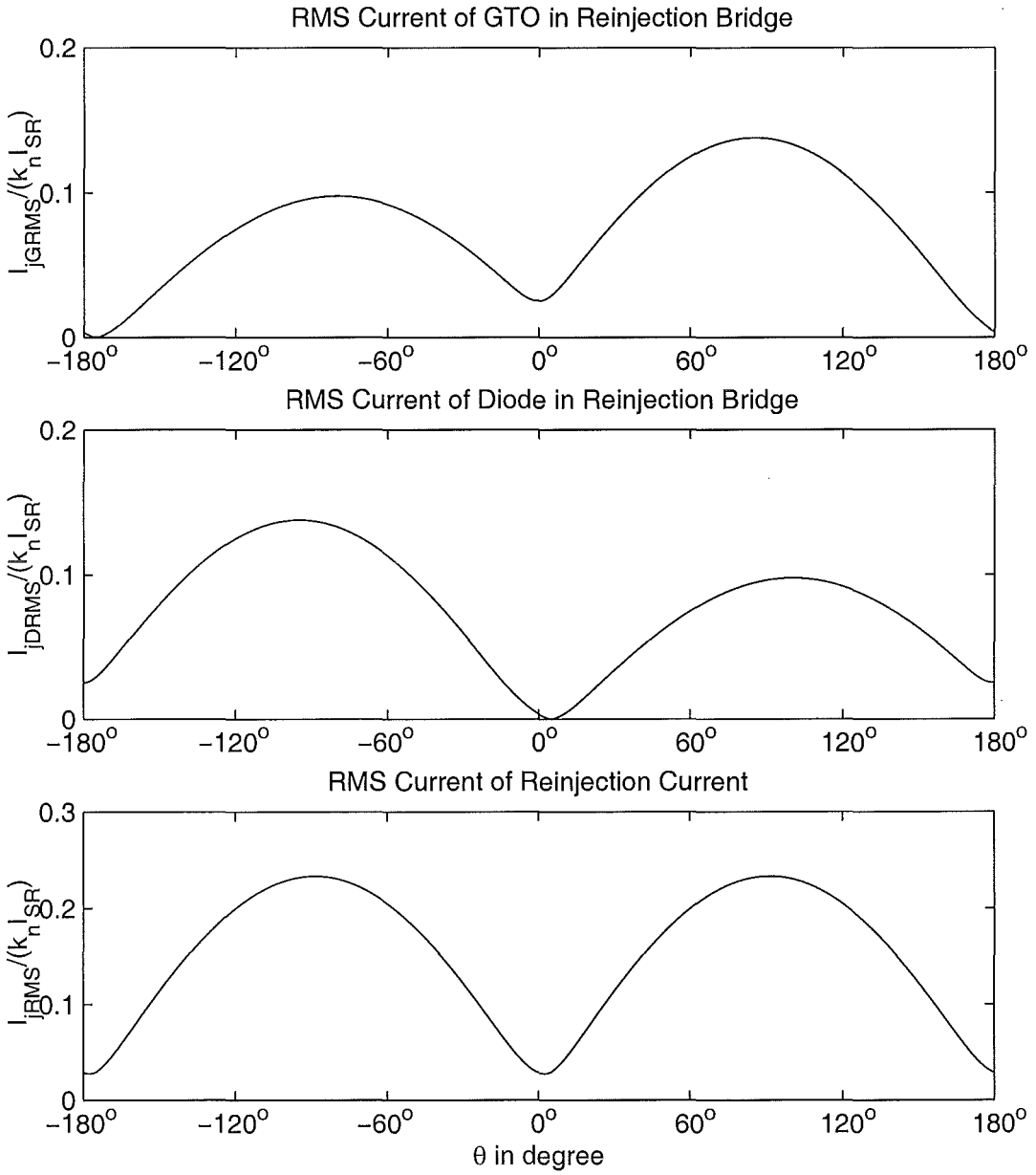


Figure 3.13 The Reinjection Switch RMS Current Versus Power Angle

The maximum RMS current for the reinjection GTO and Diode is $I_{jGDRMSmax} = 0.1376 k_n I_{SR}$, while their minimum RMS current is 0.

D.C. side capacitance

The rated dc average voltage of the two dc side capacitors is

$$U_{dcR} = \frac{\pi k_n^{-1}\sqrt{2}V_{AR}}{4[1+2(4\cos(\frac{\pi}{36})\sin(\frac{\pi}{12})-1)k_j]} \approx 1.0884k_n^{-1}(1+k_s)V_{SR}, \tag{3.147}$$

The peak to peak value of the ripple voltage for a conventional 6-pulse convertor system is

$$V_{ppr6} = \frac{\sqrt{2}k_n I_{SR}}{\omega C_6}[1-\cos(\pi/6)] \approx \frac{0.1895k_n I_{sR}}{\omega C_6} \tag{3.148}$$

For the reinjection system a full cycle of the steady state current of the dc capacitor is given by

$$i_{dc}(\omega t) = \begin{cases} \sqrt{2}k_n I_{SR}[(1-k_j)\sin(\omega t-\pi/6) & \\ \qquad +k_j\sin(\omega t)] & 0<\omega t<\pi/18 \\ \sqrt{2}k_n I_{SR}\sin(\omega t-\pi/6) & \pi/18<\omega t<\pi/9 \\ \sqrt{2}k_n I_{SR}[(1+k_j)\sin(\omega t-\pi/6) & \\ \qquad -k_j\sin(\omega t)] & \pi/9<\omega t<\pi/6 \\ \sqrt{2}k_n I_{SR}[(1+k_j)\sin(\omega t-\pi/6) & \\ \qquad -k_j\sin(\omega t-\pi/3)] & \pi/6<\omega t<2\pi/9 \\ \sqrt{2}k_n I_{SR}\sin(\omega t-\pi/6) & 2\pi/9<\omega t<5\pi/18 \\ \sqrt{2}k_n I_{SR}[(1-k_j)\sin(\omega t-\pi/6) & \\ \qquad +k_j\sin(\omega t-\pi/3)] & 5\pi/18<\omega t<\pi/3 \end{cases} \tag{3.149}$$

The dc capacitor ripple voltage of the reinjection system can be obtained by integration of the current, i.e.

$$v_{dc}(\omega t) = \begin{cases} \frac{\sqrt{2}k_n I_{SR}}{\omega C}[(1-k_j)(\cos(\pi/6)-\cos(\omega t-\pi/6)) & \\ \quad +k_j(1-\cos\omega t)] + V_{j0} & 0<\omega t<\frac{\pi}{18} \\ \frac{\sqrt{2}k_n I_{sR}}{\omega C}[\cos(\pi/9)-\cos(\omega t-\pi/6)] + V_{j0} & \frac{\pi}{18}<\omega t<\frac{\pi}{9} \\ \frac{\sqrt{2}k_n I_{sR}}{\omega C}[(1+k_j)(\cos(\pi/18)-\cos(\omega t-\pi/6)) & \\ \quad -k_j(\cos(\pi/9)-\cos\omega t)] + V_{j0} & \frac{\pi}{9}<\omega t<\frac{\pi}{6} \\ \frac{\sqrt{2}k_n I_{sR}}{\omega C}[(1+k_j)(1-\cos(\omega t-\pi/6)) & \\ \quad -k_j(\cos(\pi/6)-\cos(\omega t-\pi/3))] + V_{j0} & \frac{\pi}{6}<\omega t<\frac{2\pi}{9} \\ \frac{\sqrt{2}k_n I_{sR}}{\omega C}[\cos(\pi/18)-\cos(\omega t-\pi/6)] + V_{j0} & \frac{2\pi}{9}<\omega t<\frac{5\pi}{18} \\ \frac{\sqrt{2}k_n I_{sR}}{\omega C}[(1-k_j)(\cos(\pi/9)-\cos(\omega t-\pi/6)) & \\ \quad +k_j(\cos(\pi/18)-\cos\omega t-\pi/3)] + V_{j0} & \frac{5\pi}{18}<\omega t<\frac{\pi}{3} \end{cases} \tag{3.150}$$

where $V_{j0} = (\sqrt{2}/2-\sqrt{6}/4)k_n I_{sR}/(\omega C)$. The ripple voltage peak to peak value of the

reinjection system, V_{ppR}, can be derived from the equation above, and is given by

$$V_{ppR} = \frac{\sqrt{2}k_n I_{sR}}{\omega C}[1 - \cos(\pi/6)] \approx \frac{0.1895 k_n I_{sR}}{\omega C}. \tag{3.151}$$

As $V_{ppr6} = V_{ppR}$, the reinjection system must use the same size of capacitors as the conventional 6-pulse converter for the same ripple amplitude.

3.4 CONCLUSIONS

The Multi-Level ESEDS-Reinjection VSC is implemented by adding a reinjection self-commutated bridge and a reinjection transformer. The voltage waveforms across the two main bridges are the multi-level approximation of a fully symmetrical ESEDS waveform with minimum THD voltage for the specified level number.

The Multi-Level ESEDS-Reinjection configuration is not suited to high level numbers, because these would require complicated structures for the reinjection transformer and bridge.

The Multi-Level ESEDS-Reinjection VSC with a reinjection transformer provides the commutation condition of low voltage stress for the main bridge switches. Although that is not an exact ZVS soft switching condition, the switching losses can still be greatly reduced.

The main advantages of the Multi-Level ESEDS-Reinjection configuration are the absence of capacitor voltage balance problems and the free control of active and reactive powers, because there is no need to draw the currents with dc component from internal nodes of the dc capacitor bank. The main disadvantage is the need of a reinjection transformer with relatively high power losses despite its small size (for its operation frequency is six times the fundamental frequency).

The parallel and series connected main bridge schemes are suited for different requirements. The parallel scheme reduces the size of capacitor by a factor of 9 when compared to the 12-pulse converter, but requires a higher rated reinjection transformer; the series scheme needs the same size of capacitor as the 6-pulse converter, but requires a lower rated reinjection transformer and a reinjection bridge of lower current but higher voltage ratings.

Chapter 4

THE MLVR WAVEFORM GENERATING CIRCUIT

4.1 INTRODUCTION

Due to the low voltage ratings of the power switch devices a high voltage self-commutated converter system requires either the direct series connection of power switches or the series combination of converter bridges. Because the series combination of converter bridges needs isolated transformer windings for the individual bridges, this solution is uneconomical for high power and high voltage applications. The direct series connection of power switches is an effective solution, but presents steady and dynamic voltage balancing problems that requires the use of special control strategies and topological structures. The **multi-level conversion** concept has been developed to solve the steady and dynamic voltage balancing problems by means of asynchronous firing control of the series connected power switches and complicated converter topological structures.

The use of **soft switching** techniques reduces switching losses in the power switches and improves their performance. The main problem with soft switching for high power converters is the complexity of the extra circuit required to provide the ZVS or ZCS conditions.

The multi-level voltage reinjection (MLVR) concept discussed in this chapter combines the advantages of the reinjection, multi-level conversion and soft switching concepts to form a high performance ac-dc converters for high power applications.

The use of fully symmetrical multi-level reinjection voltage waveforms either ESEDS or Linear symmetrical reinjection provides step by step variant voltages to the main bridges and a zero voltage level in which the power switches change their switching states. This solution has the following effects:

1. The step by step voltage variation reduces the harmonic distortion and the dV/dt stress at the dc and ac sides. Thus the use of harmonic and high frequency filters is not required.

2. The provision of a controllable length period of zero voltage condition ensures

that the series connected switches in the main bridges change their switching state synchronously without the dynamic voltage balance problem. Thus only resistors in parallel with the series connected switching devices are needed for steady voltage balancing.

3. The zero voltage switching condition starts before the switching process and finishes after the switching process, thus the storage energy in the parasitic capacitors and stray inductors can be returned to the system, instead of being consumed in the switching devices and their snubbers. The converter main bridges are thus of simple structure without snubber requirements.

Having explained that the step voltage simplifies the main bridges design as well as their firing control and topological structure, the question remaining is the implementation of the periodically varying MLVR waveforms for the main bridges.

The fully symmetrical multi-level reinjection waveforms across the two main bridges can be decomposed into their dc and ac components, and these have been generated in the previous chapter by adding and subtracting an isolated ac voltage source to the dc voltage of the two main bridges. However the need for isolation requires the use of a reinjection transformer and winding limitations results in lower level numbers; and moreover that scheme operates without the advantages of the exact soft switching condition.

Another way of generating the fully symmetrical reinjection voltage waveforms is to supply the dc source voltage to the two main bridges via a controllable voltage divider. The dc voltage divider distributes the dc voltage to the bridges in periodically varying multi-level steps with zero voltage level. In this way only one circuit is used to generate the required waveforms to the two main bridges, and thus the cost and complexity are reduced.

Although each pole (a phase leg of a 3-phase converter) in conventional multi-level voltage source converters can be treated as a controllable dc voltage divider and used to generate the required waveforms, their topological structure is very complex, particularly for high level numbers. Therefore there is a need to simplify the topological structure of high level numbers.

The single phase multi-level diode clamped (MLDC) converter will be the main subject of discussion, but possible ideas for the development of the multi-level capacitor clamped (MLCC) VSC and multi-level cascaded H-bridge (MLCHB) VSC will also be given.

4.2 SWITCHING DEVICE CLAMPED TOPOLOGY STRUCTURE

For voltage source converters the high dc voltage has to be shared between series connected capacitors, and similarly, a number of power switches need to be connected

in series to withstand the high voltage, which is much higher than their individual voltage rating. Thus there are multiple intermediate nodes available for multi-level purpose, and thus only the addition of clamping diodes or clamping valves add to the converter cost.

The following discussion on the topological structure for high voltage application aims at reducing the number of clamping switches for the multi-level reinjection circuit. The reinjection solution achieves good steady and dynamic voltage balance of the main bridge switches; this is partly due to the fact that the main bridge switch commutations occur at zero voltage level and that the voltages across the two main bridges are controlled to vary level by level.

An increase in the level number provides further harmonic reduction and improves the steady and dynamic voltage balance because the switches are clamped to the capacitors with equal voltage, and the output voltage waveform is controlled to change level by level.

However, the level number can not be too high due to the additional costs involved. The following topological configurations are described in the next subsections to reduced the number of clamping switches:

1. Series Connected Main Switches and Independent Diode clamping Paths
2. Series Connected Main Switches and Asymmetrical switch Clamping Paths
3. Binary Grouped Controllable Asymmetrical switch paths

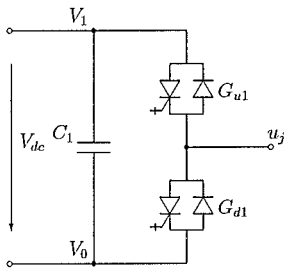
The following symbols are used to compare the different topological configurations: m is the level number, V_{dc} is the rated dc voltage of the converter system obtained from some stable dc source, $V_L = V_{dc}/(m-1)$ is the voltage across every dc capacitor, V_L is the standard nominal voltage unit, both for the dc capacitor and also for the clamping switch or diode and main switch assembly.

4.2.1 Diode Clamped Topology

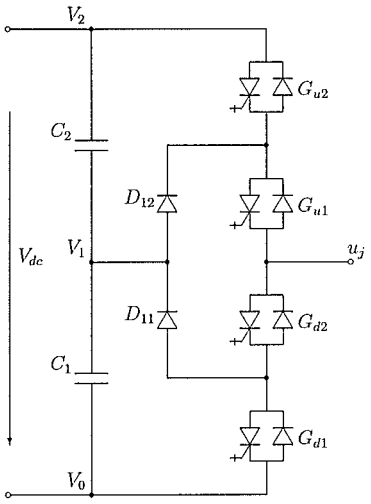
Figures 4.1 and 4.2 show one phase of the topological structures of the MLDC-VSC (Multi-Level Diode Clamped Voltage Source Converter), from two-level to m-level. In the m-level converter the clamping diodes connected with every clamping node contain not two but $m-1$ units, because the maximum blocking voltage across the clamping diodes is related to its position in the diode clamping network.

With reference to Figure 4.2, the clamping node with potential V_i is connected by a group of diodes to the node between valves G_{ui} and $G_{u(i+1)}$, and the maximum and minimum potentials of this node are V_{m-1} and V_i respectively.

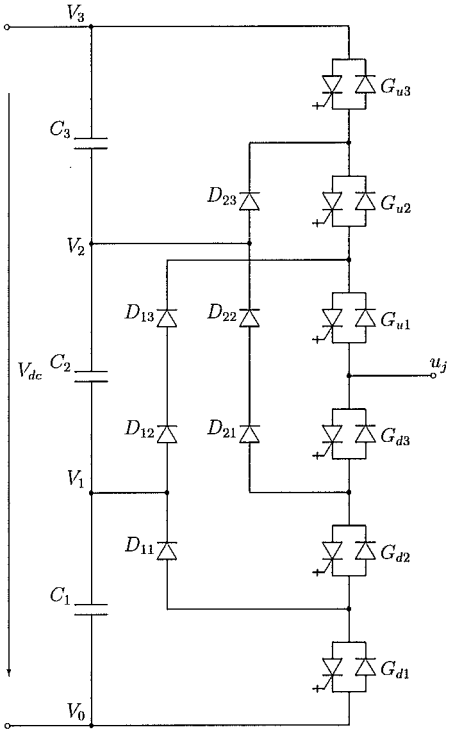
V_i is also connected to the node between valves G_{di} and $G_{d(i+1)}$, of which the maximum and minimum potential are V_i and V_0, thus the maximum voltage across the path



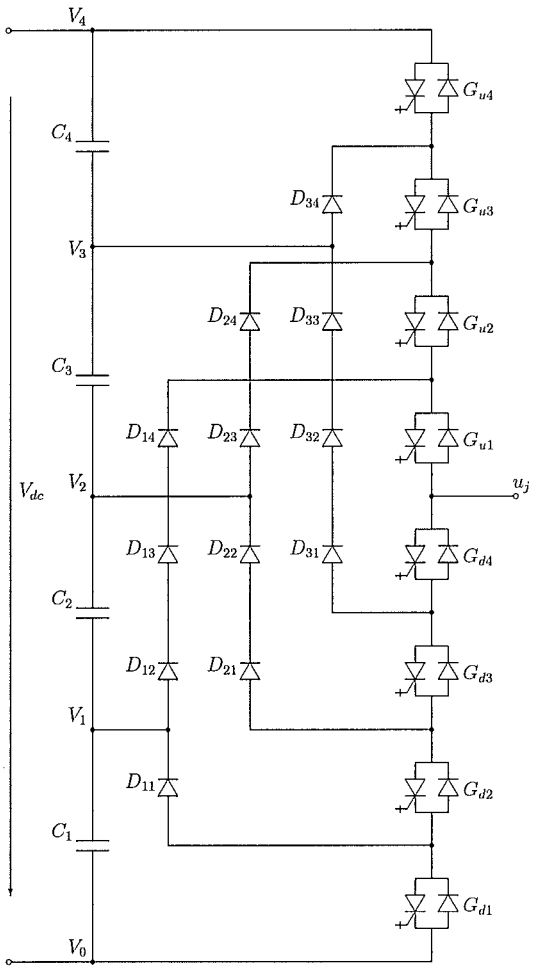
(a). $two-level$



(b). $three-level$



(c). $four-level$



(d). $five-level$

Figure 4.1 The Topological Structures of MLDC-VSC

from the node with potential V_i to the node between G_{ui} and $G_{u(i+1)}$ is $V_{m-1} - V_i = (m-1-i)V_L$; also the maximum voltage across the path from the node with potential V_i to the node between G_{di} and $G_{d(i+1)}$ is $V_i - V_0 = iV_L$.

Thus the number of the clamping diodes connected with every level node is $(m-1)$, and the clamping path from the node with potential V_i to the main upper switches is formed by $(m-1-i)$ clamping diodes, while the clamping path from the node with potential V_i to the main down switches is formed by i clamping diodes. For a m-level converter there are $(m-2)$ inner nodes needed to be clamped to, therefore the number of the total clamping diodes is given by

$$N_{CD} = (m-1) \times (m-2) \tag{4.1}$$

The required number of main switches is easier to determine. Since the output u_j (referring to Figure 4.2) is varied from V_0 to $V_{(m-1)}$ for a m-level converter, the maximum voltage across the path from the output terminal to the lowest level node is $V_{(m-1)} - V_0 = (m-1)V_L$, and the maximum voltage across the path from the highest level node to the output terminal is also $V_{(m-1)} - V_0 = (m-1)V_L$. The number of the main switches is therefore $2(m-1)$.

The switching patterns for generating m levels are listed in Table 4.1. The firing principle of the MLDC-VSC is to obtain V_i at the output terminal u_j, the $(m-1)$ main switches between the two nodes connected with the i^{th} clamping diode branch (connected to the node with potential V_i) are fired to on-state, while the remaining $(m-1)$ switches are in off-state. In Table 4.1 '1' indicates on-state and '0' is off-state.

4.2.2 Asymmetrical Switch Clamped Topology

The MLDC-VSC structure needs less main switches but more clamping diodes due to its independent clamping path structure. The number of the clamping diodes is nearly proportional to the square of the level number m.

The multi-level VSC requires its output terminal to be connected to the different potential nodes in the appropriate time interval to produce the required voltage waveform. In every interval only one path to the node is in on-state, while all of other possible paths are in off-state. This operating feature causes the potential of the multi-level VSC output terminal to vary and the blocking voltage across the off-state paths also varies. Thus it is possible to optimize the topological structure by common use of the off-state switches in series for different paths, i.e. by appropriate combination of different paths from different level nodes to the output terminal to reduce the number of the clamping switches.

The Multi-Level Asymmetrical Switch (with voltage blocking ability in one direction) Clamping (MLASC) topological structures from 2 to $m-levels$ are shown in Figures 4.3,

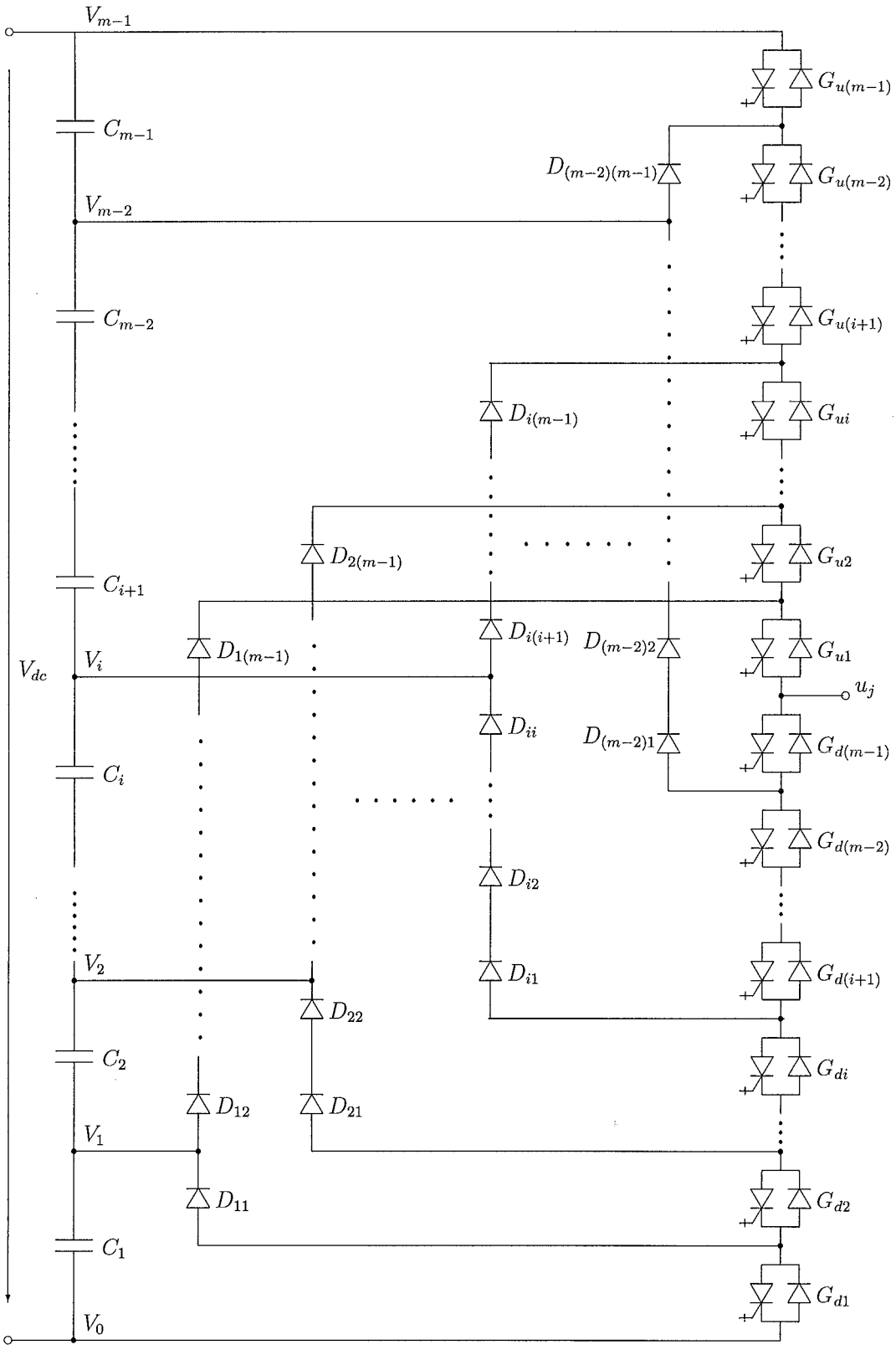


Figure 4.2 The Topological Structure of m-level MLDC-VSC

Table 4.1 Switching Patterns of MLDC-VSC

u_j	V_0	V_1	$\cdots$	V_i	$\cdots\cdots$	$V_{(m-j)}$	$\cdots$	$V_{(m-2)}$	$V_{(m-1)}$
$G_{u(m-1)}$	0	0	$\cdots$	0	$\cdots$	0	$\cdots$	0	1
$G_{u(m-2)}$	0	0	$\cdots$	0	$\cdots$	0	$\cdots$	1	1
$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	1	$\cdots$
$G_{u(m-j+1)}$	0	0	$\cdots$	0	$\cdots$	0	$\cdots$	$\cdots$	1
$G_{u(m-j)}$	0	0	$\cdots$	0	$\cdots$	1	$\cdots$	1	1
$G_{u(m-j-1)}$	0	0	$\cdots$	0	$\cdots$	1	$\cdots$	1	1
$\cdots$	$\cdots$	0	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$
$G_{u(i+1)}$	0	0	$\cdots$	0	$\cdots$	1	$\cdots$	1	1
G_{ui}	0	0	$\cdots$	1	$\cdots$	1	$\cdots$	1	1
$G_{u(i-1)}$	0	0	$\cdots$	1	$\cdots$	1	$\cdots$	1	1
$\cdots$	$\cdots$	0	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$
G_{u2}	0	0	$\cdots$	1	$\cdots$	1	$\cdots$	1	1
G_{u1}	0	1	$\cdots$	1	$\cdots$	1	$\cdots$	1	1
$G_{d(m-1)}$	1	1	$\cdots$	1	$\cdots$	1	$\cdots$	1	0
$G_{d(m-2)}$	1	1	$\cdots$	1	$\cdots$	1	$\cdots$	0	0
$\cdots$	$\cdots$	1	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$
$G_{d(m-j+1)}$	1	1	$\cdots$	1	$\cdots$	1	$\cdots$	0	0
$G_{d(m-j)}$	1	1	$\cdots$	1	$\cdots$	0	$\cdots$	0	0
$G_{d(m-j-1)}$	1	1	$\cdots$	1	$\cdots$	0	$\cdots$	0	0
$\cdots$	$\cdots$	1	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	0	$\cdots$
$G_{d(i+2)}$	1	1	$\cdots$	1	$\cdots$	0	$\cdots$	0	0
$G_{d(i+1)}$	1	1	$\cdots$	1	$\cdots$	0	$\cdots$	0	0
G_{di}	1	1	$\cdots$	0	$\cdots$	0	$\cdots$	0	0
$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$
G_{d2}	1	1	$\cdots$	0	$\cdots$	0	$\cdots$	0	0
G_{d1}	1	0	$\cdots$	0	$\cdots$	0	$\cdots$	0	0

4.4 and 4.5. With reference to Figure 4.4, the $\frac{m}{2}$ paths from level $V_{(\frac{m}{2})} \cdots V_{(m-1)}$ to the output terminal (denoted with symbol u_j) are formed by the clamping switches (the horizonal ones of the upper half circuit in Figure 4.4) and main switches (the vertical ones in Figure 4.4) of the valves G_{u1} to $G_{u(m-1)}$. $\frac{m}{2}$ valves of the main switches (i.e. valves G_{u1} to $G_{u(\frac{m}{2})}$) are shared by those paths. Similarly the $\frac{m}{2}$ paths from level $V_0 \cdots V_{(\frac{m}{2}-1)}$ to the output terminal are formed by the horizonal clamping switches of the lower half circuit, and main switches of the valves G_{d1} to $G_{d(m-1)}$. $\frac{m}{2}$ valves of the main switches (i.e. valves $G_{d(\frac{m}{2})}$ to $G_{d(m-1)}$) are shared by those paths. Each clamping path in the upper half circuit consists of force-commutated switches and anti-parallel freewheeling diodes to allow the flow of current from level nodes to the output terminal, while each clamping path in the lower half circuit consists of force-commutated switches and freewheeling diodes to allow the flow of current from the output terminal to level nodes. This structure ensures that the voltages across switch units $G_{u(\frac{m}{2}+1)} \cdots G_{(m-1)}$ and G_{d1} to $G_{d(\frac{m}{2}-1)}$, are within the nominal level voltage at the steady state conditions, i.e. they are clamped to stable and equal voltage levels.

The commonly shared valves, i.e. valves $G_{d(\frac{m}{2})} \cdots G_{d(m-1)}$ and $G_{u1} \cdots G_{u(\frac{m}{2})}$ are not clamped to individual voltage levels. Therefore some arrangement must be made for balancing the steady state voltages across them, but no dynamic balancing problem occurs due to the output voltage being changed level by level.

For a m-level converter there are $(m-2)$ inner level nodes, if m is even, and the number of the total clamping switches is

$$N_{CSme} = (\frac{m}{2} - 1) \times \frac{m}{2} = \frac{m(m-2)}{4} \tag{4.2}$$

if m is odd, the number of the total clamping switches is

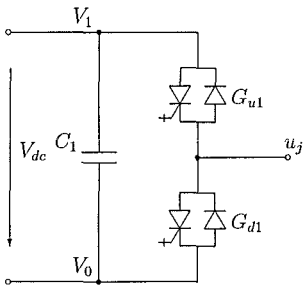
$$N_{CSmo} = (\frac{m-1}{2} + 1) \times \frac{m-1}{2} = \frac{m^2-1}{4} \tag{4.3}$$

The switching patterns to output m levels are listed in Tables 4.2, 4.3, 4.4, 4.5. In the tables logic symbol '1' is used for on-state and '0' for off state, and symbol '×' indicate an arbitrary state of on or off. There are two paths from the node with potential $V_{(\frac{m-1}{2})}$ to the output terminal when m is odd, as shown in Figure 4.3 and 4.5. Thus the connection from the node with potential $V_{(\frac{m-1}{2})}$ to the output terminal has multiple choices; to show these multiple choices the symbols '∇' and '$\triangle$' in Table 4.4 are used to illustrate that the two possible paths are formed by all of '∇' or '$\triangle$' in the same column being in on state. Tables 4.4 and 4.5 list the switch patterns to generate individual output levels. As the switching patterns in Table 4.5 are similar to those of the MLDC-VSC, the forced commutated switches in the two paths from the clamping node with potential $V_{(\frac{m-1}{2})}$ to the output terminal can be removed, requiring only freewheel diodes. That means the switch number can be reduced by $(m-1)$, if the switching pattern in Table 4.5 is used.

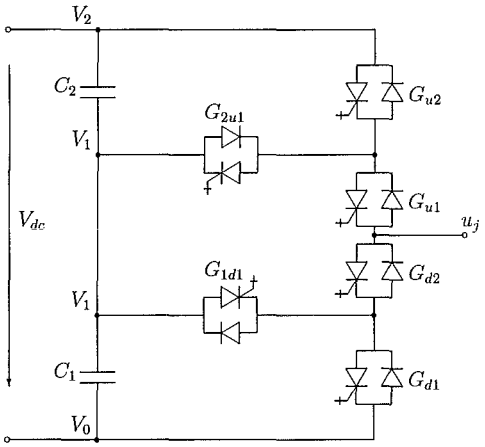
4.2.3 Binary Grouped Multi-Path Topology

The Multi-Level Asymmetrical Switch Clamping structure described above uses the main switches to block the forward voltage, but not the clamping switches. An effective way of reducing the switches needed for the multi-level conversion further, is the common use of switches by different paths to share the voltage stress across them.

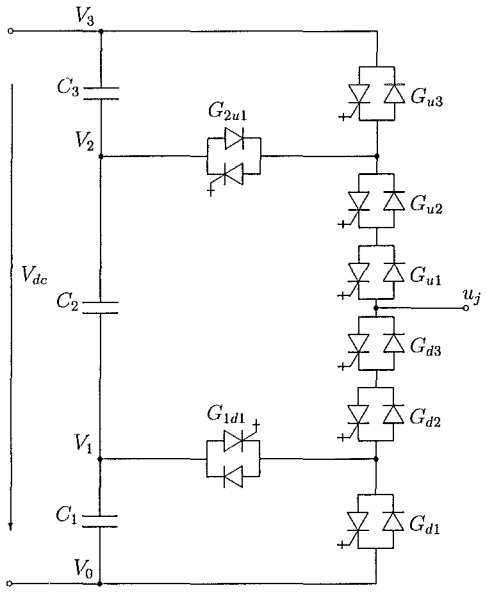
The multi-level voltage source converter is a combination of a multi-level output dc source consisting of series connected equal dc sources, each with voltage V_L, and a switch assembly which provides the controllable bidirectional current paths from the dc voltage sources to the converter output terminal. In a m-level converter there are m controllable paths to access the m different voltage level poles. At any instant only one path is in on-state to output a specific voltage level and provide a bidirectional current channel between the converter output terminal and the specific level pole of the dc



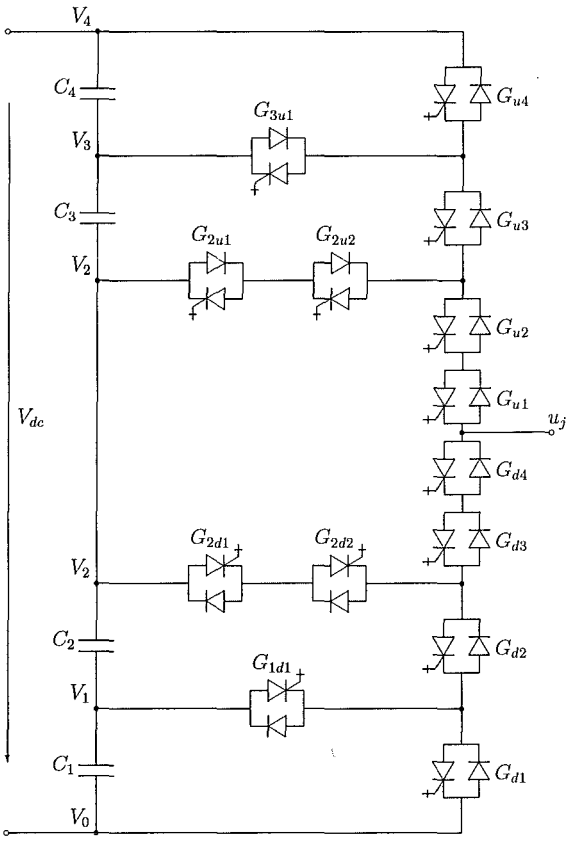
(a). *two – level*



(b). *three – level*



(c). *four – level*



(d). *five – level*

Figure 4.3 The Topological Structures of MLASC-VSC

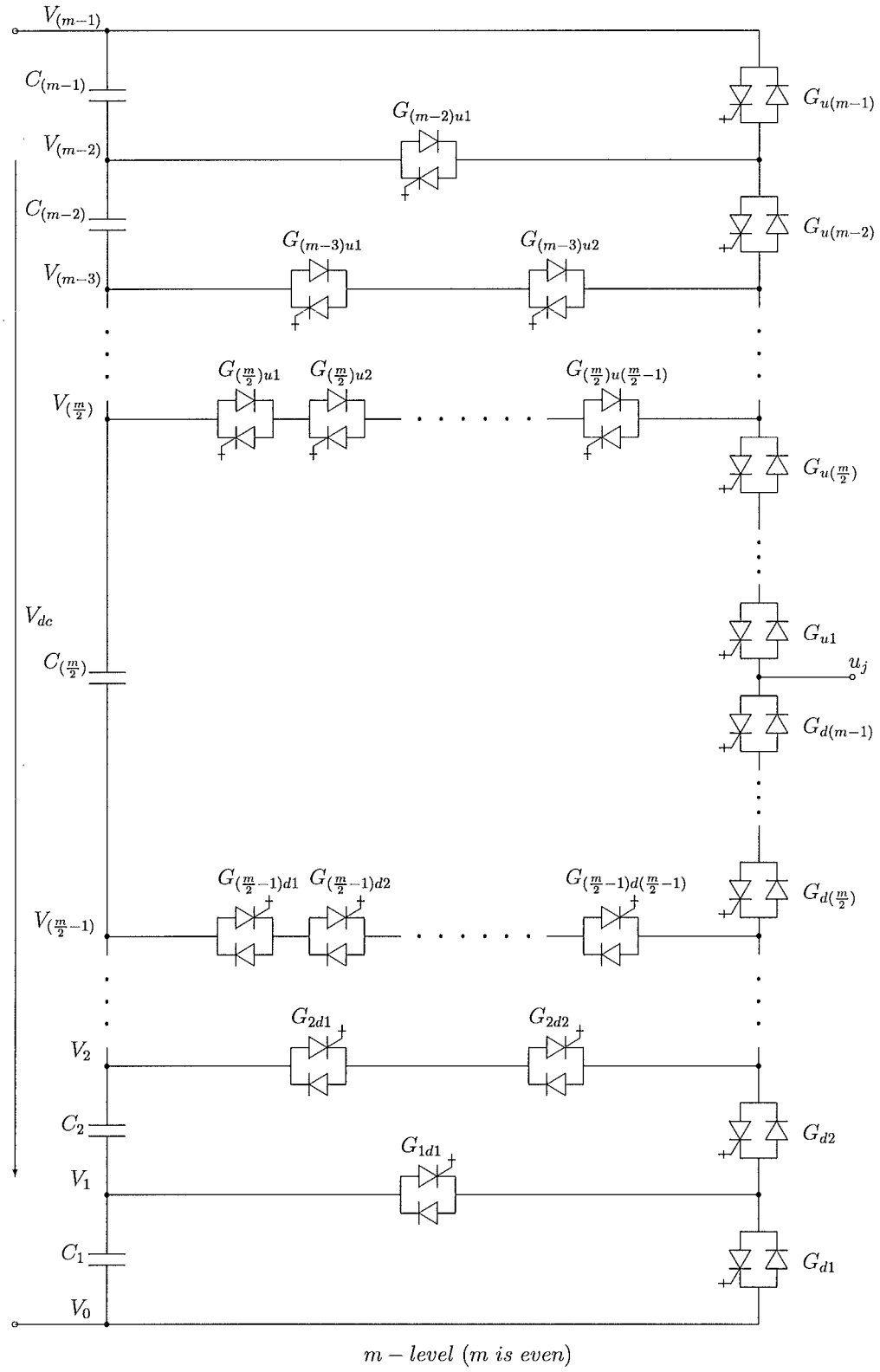


Figure 4.4 The Even-Level Topological Structures of MLASC-VSC

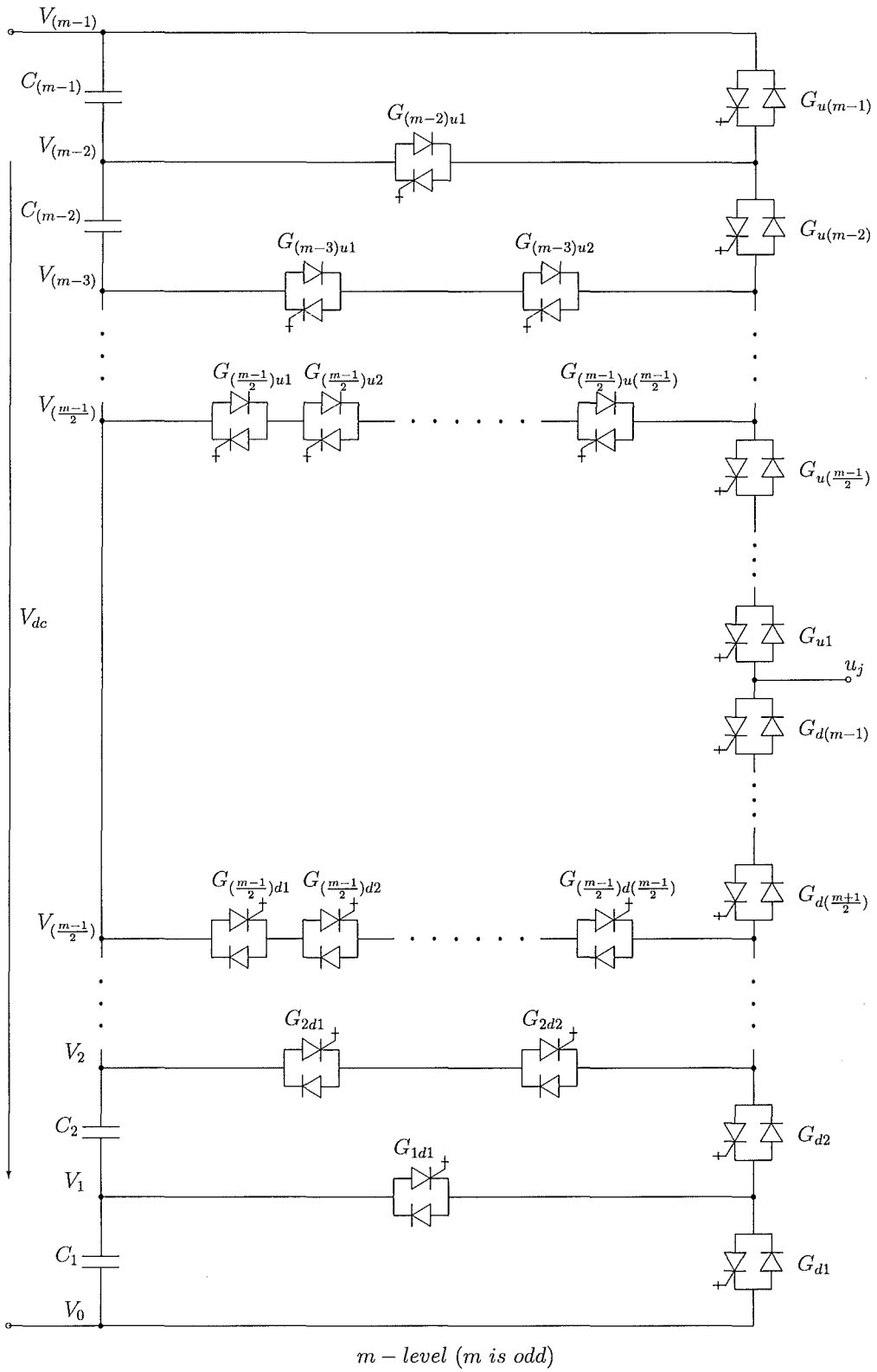
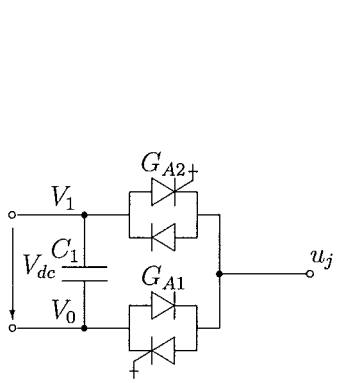
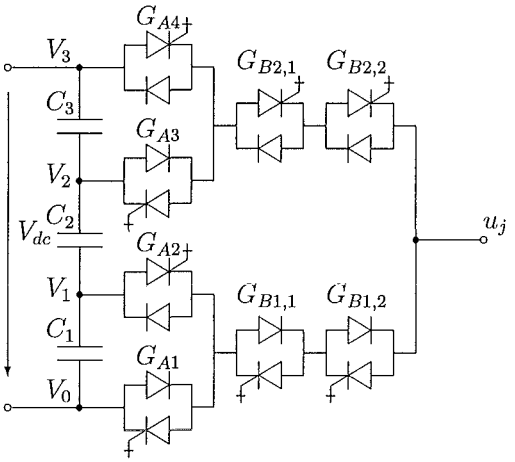


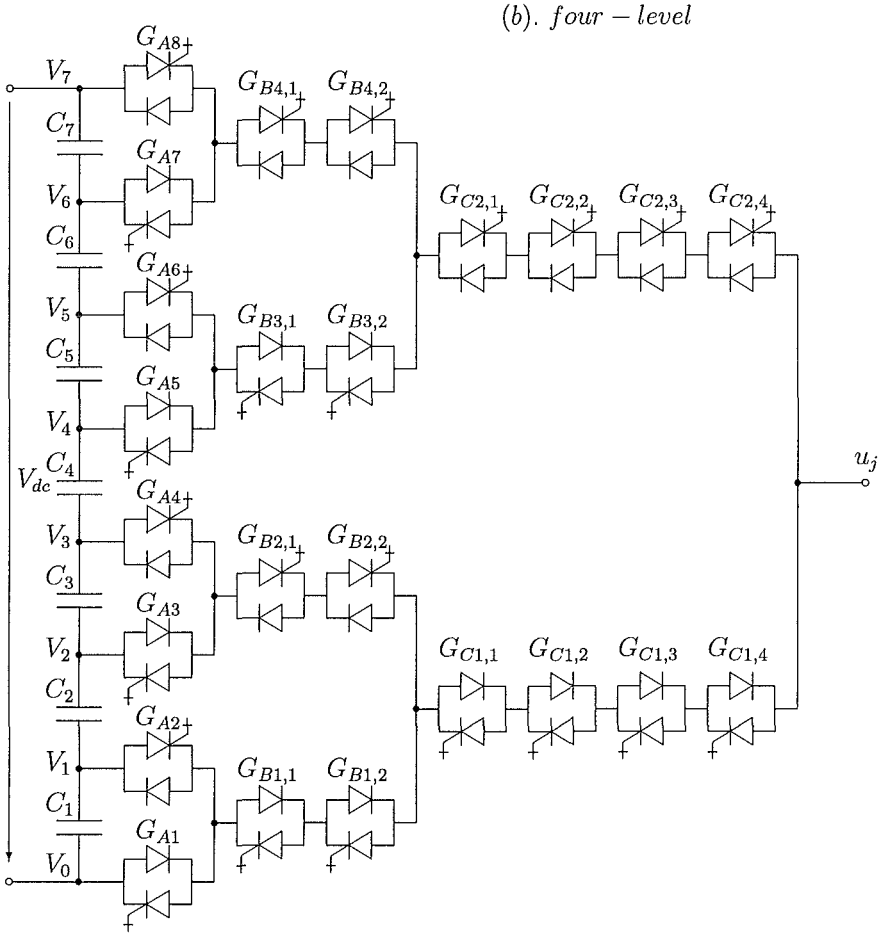
Figure 4.5 The Odd-level Topological Structures of MLASC-VSC



$(a).\ two-level$



$(b).\ four-level$



$(c).\ eight-level$

Figure 4.6 The Topological Structures of BGASMP-VSC

Table 4.2 Switching Patterns A_e

u_j	V_0	$\cdots$	V_i	$\cdots$	$V_{(\frac{m}{2}-1)}$	$V_{(\frac{m}{2})}$	$\cdots$	$V_{(m-j)}$	$\cdots$	$V_{(m-1)}$
$G_{u(m-1)}$	0	$\cdots$	0	$\cdots$	0	0	$\cdots$	0	$\cdots$	1
$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$
$G_{u(m-j+1)}$	0	$\cdots$	0	$\cdots$	0	0	$\cdots$	0	$\cdots$	1
$G_{u(m-j)}$	0	$\cdots$	0	$\cdots$	0	0	$\cdots$	1	$\cdots$	1
$G_{u(m-j-1)}$	0	$\cdots$	0	$\cdots$	0	0	$\cdots$	1	$\cdots$	1
$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$
$G_{u(\frac{m}{2}+1)}$	0	$\cdots$	0	$\cdots$	0	0	$\cdots$	1	$\cdots$	1
$G_{u(\frac{m}{2})}$	0	$\cdots$	0	$\cdots$	0	1	$\cdots$	1	$\cdots$	1
$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$
G_{u1}	0	$\cdots$	0	$\cdots$	0	1	$\cdots$	1	$\cdots$	1
$G_{d(m-1)}$	1	$\cdots$	1	$\cdots$	1	0	$\cdots$	0	$\cdots$	0
$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$
$G_{d(\frac{m}{2})}$	1	$\cdots$	1	$\cdots$	1	0	$\cdots$	0	$\cdots$	0
$G_{d(\frac{m}{2}-1)}$	1	$\cdots$	1	$\cdots$	0	0	$\cdots$	0	$\cdots$	0
$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$
$G_{d(i+2)}$	1	$\cdots$	1	$\cdots$	0	0	$\cdots$	0	$\cdots$	0
$G_{d(i+1)}$	1	$\cdots$	1	$\cdots$	0	0	$\cdots$	0	$\cdots$	0
G_{di}	1	$\cdots$	0	$\cdots$	0	0	$\cdots$	0	$\cdots$	0
$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$
G_{d1}	1	$\cdots$	0	$\cdots$	0	0	$\cdots$	0	$\cdots$	0
$G_{(m-2)u1}$	$\times$	$\cdots$	$\times$	$\cdots$	$\times$	0	$\cdots$	0	$\cdots$	0
$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$
$G_{(m-j)u1}\cdots$ $G_{(m-j)u(j-1)}$	$\times$	$\cdots$	$\times$	$\cdots$	$\times$	0	0	1	$\cdots$	0
$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$
$G_{(\frac{m}{2})u1}\cdots$ $G_{(\frac{m}{2})d(\frac{m}{2}-1)}$	$\times$	$\cdots$	$\times$	$\cdots$	$\times$	1	$\cdots$	0	$\cdots$	0
$G_{(\frac{m}{2}-1)d1}\cdots$ $G_{(\frac{m}{2}-1)d(\frac{m}{2}-1)}$	0	$\cdots$	0	$\cdots$	1	$\times$	$\cdots$	$\times$	$\cdots$	$\times$
$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$
$G_{id1}\cdots$ G_{idi}	0	$\cdots$	1	$\cdots$	0	$\times$	$\cdots$	$\times$	$\cdots$	$\times$
$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$
G_{1d1}	0	$\cdots$	0	$\cdots$	0	$\times$	$\cdots$	$\times$	$\cdots$	$\times$

sources, while the remaining $(m-1)$ paths must be in off-state to prevent short circuit. The voltages across the $(m-1)$ blocking paths change with the converter output voltage, because the dc sources side terminals of the $(m-1)$ blocking paths are connected to the specific voltage levels, while their other terminals are connected to the varying voltage converter output terminal. If the voltage drop across the on-state path is ignored, the voltages across the blocking paths are V_L, $2V_L$, $3V_L, \cdots, (m-2)V_L$, $(m-1)V_L$. Thus the number of switches needed for the different paths vary with the converter output voltage.

Table 4.3 Switching Patterns B_e

u_j	V_0	$\cdots$	V_i	$\cdots$	$V_{(\frac{m}{2}-1)}$	$V_{(\frac{m}{2})}$	$\cdots$	$V_{(m-j)}$	$\cdots$	$V_{(m-1)}$
$G_{u(m-1)}$	0	$\cdots$	0	$\cdots$	0	0	$\cdots$	0	$\cdots$	1
$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$
$G_{u(m-j+1)}$	0	$\cdots$	0	$\cdots$	0	0	$\cdots$	0	$\cdots$	1
$G_{u(m-j)}$	0	$\cdots$	0	$\cdots$	0	0	$\cdots$	1	$\cdots$	1
$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$
$G_{u(\frac{m}{2})}$	0	$\cdots$	0	$\cdots$	0	1	$\cdots$	1	$\cdots$	1
$G_{u(\frac{m}{2}-1)}$	0	$\cdots$	0	$\cdots$	1	1	$\cdots$	1	$\cdots$	1
$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$
$G_{u(i+1)}$	0	$\cdots$	0	$\cdots$	1	1	$\cdots$	1	$\cdots$	1
G_{ui}	0	$\cdots$	1	$\cdots$	1	1	$\cdots$	1	$\cdots$	1
$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$
G_{u1}	0	$\cdots$	1	$\cdots$	1	1	$\cdots$	1	$\cdots$	1
$G_{d(m-1)}$	1	$\cdots$	1	$\cdots$	1	1	$\cdots$	1	$\cdots$	0
$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$
$G_{d(m-j+1)}$	1	$\cdots$	1	$\cdots$	1	1	$\cdots$	1	$\cdots$	0
$G_{d(m-j)}$	1	$\cdots$	1	$\cdots$	1	1	$\cdots$	0	$\cdots$	0
$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$
$G_{d(\frac{m}{2}+1)}$	1	$\cdots$	1	$\cdots$	1	1	$\cdots$	0	$\cdots$	0
$G_{d(\frac{m}{2})}$	1	$\cdots$	1	$\cdots$	1	0	$\cdots$	0	$\cdots$	0
$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$
$G_{d(i+1)}$	1	$\cdots$	1	$\cdots$	0	0	$\cdots$	0	$\cdots$	0
G_{di}	1	$\cdots$	0	$\cdots$	0	0	$\cdots$	0	$\cdots$	0
$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$
G_{d1}	1	$\cdots$	0	$\cdots$	0	0	$\cdots$	0	$\cdots$	0
$G_{(m-2)u1}$	$\times$	$\cdots$	$\times$	$\cdots$	$\times$	0	$\cdots$	0	$\cdots$	0
$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$
$G_{(m-j)u1}\cdots$ $G_{(m-j)u(j-1)}$	$\times$	$\cdots$	$\times$	$\cdots$	$\times$	0	0	1	$\cdots$	0
$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$
$G_{(\frac{m}{2})u1}\cdots$ $G_{(\frac{m}{2})d(\frac{m}{2}-1)}$	$\times$	$\cdots$	$\times$	$\cdots$	$\times$	1	$\cdots$	0	$\cdots$	0
$G_{(\frac{m}{2}-1)d1}\cdots$ $G_{(\frac{m}{2}-1)d(\frac{m}{2}-1)}$	0	$\cdots$	0	$\cdots$	1	$\times$	$\cdots$	$\times$	$\cdots$	$\times$
$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$
$G_{id1}\cdots$ G_{idi}	0	$\cdots$	1	$\cdots$	0	$\times$	$\cdots$	$\times$	$\cdots$	$\times$
$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$
G_{1d1}	0	$\cdots$	0	$\cdots$	0	$\times$	$\cdots$	$\times$	$\cdots$	$\times$

In the Binary Grouped Asymmetrical Switch Multi-Path Voltage Source Converter (BGASMP-VSC), there are m paths from the m individual levels to the output terminal but only m switches belong to individual paths, all other switches are commonly used by binary grouped paths (at least by 2 paths).

The BGASMP-VSC topological structure series shown in Figure 4.6 for 2, 4 and 8

Table 4.4 Switching Patterns A_o

u_j	V_0	V_1	$\cdots$	V_i	$\cdots$	$V_{(\frac{m-1}{2})}$	$\cdots$	$V_{(m-j)}$	$\cdots$	$V_{(m-1)}$
$G_{u(m-1)}$	0	0	$\cdots$	0	$\cdots$	0	$\cdots$	0	$\cdots$	1
$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$
$G_{u(m-j+1)}$	0	0	$\cdots$	0	$\cdots$	0	$\cdots$	0	$\cdots$	1
$G_{u(m-j)}$	0	0	$\cdots$	0	$\cdots$	0	$\cdots$	1	$\cdots$	1
$G_{u(m-j-1)}$	0	0	$\cdots$	0	$\cdots$	0	$\cdots$	1	$\cdots$	1
$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$
$G_{u(\frac{m+1}{2})}$	0	0	$\cdots$	0	$\cdots$	0	$\cdots$	1	$\cdots$	1
$G_{u(\frac{m-1}{2})}$	0	0	$\cdots$	0	$\cdots$	$\triangle$	$\cdots$	1	$\cdots$	1
$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$
G_{u1}	0	0	$\cdots$	0	$\cdots$	$\triangle$	$\cdots$	1	$\cdots$	1
$G_{d(m-1)}$	1	1	$\cdots$	1	$\cdots$	∇	$\cdots$	0	$\cdots$	0
$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	0	$\cdots$	0
$G_{d(\frac{m+1}{2})}$	1	1	$\cdots$	1	$\cdots$	∇	$\cdots$	0	$\cdots$	0
$G_{d(\frac{m-1}{2})}$	1	1	$\cdots$	1	$\cdots$	0	$\cdots$	0	$\cdots$	0
$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$
$G_{d(i+2)}$	1	1	$\cdots$	1	$\cdots$	0	$\cdots$	0	$\cdots$	0
$G_{d(i+1)}$	1	1	$\cdots$	1	$\cdots$	0	$\cdots$	0	$\cdots$	0
G_{di}	1	1	$\cdots$	0	$\cdots$	0	$\cdots$	0	$\cdots$	0
$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$
G_{d2}	1	1	$\cdots$	0	$\cdots$	0	$\cdots$	0	$\cdots$	0
G_{d1}	1	0	$\cdots$	0	$\cdots$	0	$\cdots$	0	$\cdots$	0
$G_{(m-2)u1}$	$\times$	$\times$	$\cdots$	$\times$	$\cdots$	0	$\cdots$	0	$\cdots$	0
$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$
$G_{(m-j)u1}\cdots$ $G_{(m-j)u(j-1)}$	$\times$	$\times$	$\cdots$	$\times$	$\cdots$	0	$\cdots$	1	$\cdots$	0
$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$
$G_{(\frac{m-1}{2})u1}\cdots$ $G_{(\frac{m-1}{2})u(\frac{m-1}{2})}$	$\times$	$\times$	$\cdots$	$\times$	$\cdots$	$\triangle$	$\cdots$	0	$\cdots$	0
$G_{(\frac{m-1}{2})d1}\cdots$ $G_{(\frac{m-1}{2})d(\frac{m-1}{2})}$	0	0	$\cdots$	0	$\cdots$	∇	$\cdots$	$\times$	$\cdots$	$\times$
$\cdots$	$\cdots$	0	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$
$G_{id1}\cdots$ G_{idi}	0	0	$\cdots$	1	$\cdots$	0	$\cdots$	$\times$	$\cdots$	$\times$
$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$
G_{1d1}	0	1	$\cdots$	0	$\cdots$	0	$\cdots$	$\times$	$\cdots$	$\times$

levels converters has a pyramid-like structure. It can be extended to any number of levels, and the level number m is achieved with the minimum number of switches.

For the m($\log_2 m = n$) level single phase converter, in the first stage A, m paths are needed to be controlled individually to the output terminal. By binary combination of the first stage outputs there are $\frac{m}{2}$ paths in the second stage B, and the maximum voltage difference between the two adjacent outputs of the second stage is $(2 \times 2 - 1)$

Table 4.5 Switching Patterns B_o

u_j	V_0	V_1	$\cdots$	V_i	$\cdots$	$V_{(\frac{m-1}{2})}$	$\cdots$	$V_{(m-j)}$	$\cdots$	$V_{(m-1)}$
$G_{u(m-1)}$	0	0	$\cdots$	0	$\cdots$	0	$\cdots$	0	$\cdots$	1
$\cdots$	$\cdots$	0	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$
$G_{u(m-j+1)}$	0	0	$\cdots$	0	$\cdots$	0	$\cdots$	0	$\cdots$	1
$G_{u(m-j)}$	0	0	$\cdots$	0	$\cdots$	0	$\cdots$	1	$\cdots$	1
$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$
$G_{u(\frac{m+1}{2})}$	0	0	$\cdots$	0	$\cdots$	0	$\cdots$	1	$\cdots$	1
$G_{u(\frac{m-1}{2})}$	0	0	$\cdots$	0	$\cdots$	1	$\cdots$	1	$\cdots$	1
$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$
$G_{u(i+1)}$	0	0	$\cdots$	0	$\cdots$	1	$\cdots$	1	$\cdots$	1
G_{ui}	0	0	$\cdots$	1	$\cdots$	1	$\cdots$	1	$\cdots$	1
$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$
G_{u1}	0	1	$\cdots$	1	$\cdots$	1	$\cdots$	1	$\cdots$	1
$G_{d(m-1)}$	1	1	$\cdots$	1	$\cdots$	1	$\cdots$	1	$\cdots$	0
$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$
$G_{d(m-j+1)}$	1	1	$\cdots$	1	$\cdots$	1	$\cdots$	1	$\cdots$	0
$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$
$G_{d(\frac{m+1}{2})}$	1	1	$\cdots$	1	$\cdots$	1	$\cdots$	0	$\cdots$	0
$G_{d(\frac{m-1}{2})}$	1	1	$\cdots$	1	$\cdots$	0	$\cdots$	0	$\cdots$	0
$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$
$G_{d(i+1)}$	1	1	$\cdots$	1	$\cdots$	0	$\cdots$	0	$\cdots$	0
G_{di}	1	1	$\cdots$	0	$\cdots$	0	$\cdots$	0	$\cdots$	0
$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$
G_{d2}	1	1	$\cdots$	0	$\cdots$	0	$\cdots$	0	$\cdots$	0
G_{d1}	1	0	$\cdots$	0	$\cdots$	0	$\cdots$	0	$\cdots$	0
$G_{(m-2)u1}$	$\times$	$\times$	$\cdots$	$\times$	$\cdots$	0	$\cdots$	0	$\cdots$	0
$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$
$G_{(m-j)u1}\cdots$ $G_{(m-j)u(j-1)}$	$\times$	$\times$	$\cdots$	$\times$	$\cdots$	0	0	1	$\cdots$	0
$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$
$G_{(\frac{m-1}{2})u1}\cdots$ $G_{(\frac{m-1}{2})u(\frac{m-1}{2})}$	$\times$	$\times$	$\cdots$	$\times$	$\cdots$	1	$\cdots$	0	$\cdots$	0
$G_{(\frac{m-1}{2})d1}\cdots$ $G_{(\frac{m-1}{2})d(\frac{m-1}{2})}$	0	0	$\cdots$	0	$\cdots$	1	$\cdots$	$\times$	$\cdots$	$\times$
$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$
$G_{id1}\cdots$ G_{idi}	0	0	$\cdots$	1	$\cdots$	0	$\cdots$	$\times$	$\cdots$	$\times$
$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$
G_{1d1}	0	1	$\cdots$	0	$\cdots$	0	$\cdots$	$\times$	$\cdots$	$\times$

times the level voltage V_L. Therefore three switches are needed to withstand this maximum voltage; since one of them is already provided in the first stage, only two must be series connected in the second stage. By the binary combination of the second stage outputs there are only $\frac{m}{2\times 2}$ paths in the third stage C, and the maximum voltage

Table 4.6 Switching Patterns BGASMP-VSC

u_j	V_0	V_1	V_2	V_3	V_4	V_5	V_6	V_7
G_{A1}	1	0	0	0	0	0	0	0
G_{A2}	0	1	0	0	0	0	0	0
G_{A3}	0	0	1	0	0	0	0	0
G_{A4}	0	0	0	1	0	0	0	0
G_{A5}	0	0	0	0	1	0	0	0
G_{A6}	0	0	0	0	0	1	0	0
G_{A7}	0	0	0	0	0	0	1	0
G_{A8}	0	0	0	0	0	0	0	1
$G_{B1,1}$	1	1	0	0	0	0	0	0
$G_{B1,2}$	1	1	0	0	0	0	0	0
$G_{B2,1}$	0	0	1	1	0	0	0	0
$G_{B2,1}$	0	0	1	1	0	0	0	0
$G_{B3,1}$	0	0	0	0	1	1	0	0
$G_{B3,2}$	0	0	0	0	1	1	0	0
$G_{B4,1}$	0	0	0	0	0	0	1	1
$G_{B4,2}$	0	0	0	0	0	0	1	1
$G_{C1,1}$	1	1	1	1	0	0	0	0
$G_{C1,2}$	1	1	1	1	0	0	0	0
$G_{c1,3}$	1	1	1	1	0	0	0	0
$G_{c1,4}$	1	1	1	1	0	0	0	0
$G_{c2,1}$	0	0	0	0	1	1	1	1
$G_{c2,2}$	0	0	0	0	1	1	1	1
$G_{c2,3}$	0	0	0	0	1	1	1	1
$G_{C2,4}$	0	0	0	0	1	1	1	1

difference of every adjacent two output of the grouped two paths of the second stage switches are $(2 \times 2 \times 2 - 1)$ times the level voltage V_L. Therefore seven switches are needed to withstand this maximum voltage, and taking into account the switches in the first and second stages, four others must be series-connected in the third stage. In general therefore there are $n(= \log_2 m)$ stages, every stage needing m switches to commonly share the maximum blocking voltage; for every stage the inputs are twice the outputs, and the number of total switches needed is given by

$$N_{Snum} = m \log_2 m \tag{4.4}$$

The switch patterns for generating individual levels at the converter output terminal are listed in Table 4.6. It clearly shows that the switches in the stages close to the converter output terminal are used by more paths, while the switches connected directly with the series connected dc source levels are only used by the individual paths.

4.3 CAPACITOR CLAMPED AND H-BRIDGE TOPOLOGY STRUCTURE

The topological structure of **the multi-level capacitor clamped VSC** (MLCC-VSC), also referred to as multi-level floating capacitor or imbricated cell multi-level VSC, instead of switching devices uses clamping capacitors to form a multi-level dc voltage divider. Because the clamping capacitors function as independent floating dc voltage sources, these dc sources can be freely combined by the self-commutated switching device to produce the multi-level output voltage as well as clamping the voltage across the switching devices connected to them. The independent nature of these floating capacitors makes it difficult to reduce their number. Therefore a large number of them is required to generate the MLVR waveforms (nearly the square of the level number), which makes it prohibitive for high level number applications.

The voltage synthesis in MLCC-VSC has more flexibility than MLDC-VSC, because in MLCC-VSC there are multiple switching state combinations for generating a particular output level. The redundant combinations permit to alternate the current direction through the capacitors; thus the clamping capacitor voltages can be controlled by choosing the appropriate switching combinations. Although the selection of a switching combinations becomes very complicated when level number is high, the MLCC-VSC structure is a possible choice to be used as the dc voltage divider to generate the required MLVR waveforms without capacitor voltage balancing problems.

The **Multi-Level Cascaded H-bridge VSC** (MLCHB-VSC) can generate high level numbers with fewer H-bridge cells and without the need of clamping devices. The MLVR stair-case waveforms vary from zero to the dc source voltage level in one direction. Although the cascaded H-bridge multi-level voltage divider is capable of producing a bipolar output voltage, it has to operate in the unipolar mode to prevent short-circuit via the freewheel diodes of the main bridge switches.

The H-Bridge Voltage Divider with m-levels, shown in Figure 4.7, produces the MLVR stair-case waveforms without the requirement of isolated dc source for each cell; the individual cells can be powered by the common dc source.

To form an m-level voltage divider $2(m-1)$ H-bridge cells are needed, the voltage of the dc capacitor in every cell being $V_L = U_{dc}/(m-1)$. The ac output voltage of every cell in an H-bridge divider generates one level of the follow 3:

1. the dc capacitor voltage with positive polarity (when S_{H1} and S_{H4} are on and S_{H2} and S_{H3} off; this is referred as logic state $+1$),

2. the dc capacitor voltage with negative polarity (when S_{H1} and S_{H4} are off and S_{H2} and S_{H3} on; this is referred as logic state -1),

3. zero voltage (when S_{H1} and S_{H2} are on and S_{H3} and S_{H4} off, or the reverse combination; this is referred as logic state 0).

By controlling the appropriate switches in every cell, V_{top}, the combined voltage of the top $(m-1)$ cells (HB_{B1} to $HB_{B(m-1)}$, referred as group BH_B) can be: 0, V_L, $2V_L$, $\cdots$, $(m-1)V_L$; similarly V_{bot}, the combined voltage of the bottom $(m-1)$ cells (HB_{A1} to $HB_{A(m-1)}$, referred as group BH_A) can also be: 0, V_L, $2V_L$, $\cdots$, $(m-1)V_L$; moreover, the condition $V_{top} + V_{bot} = U_{dc}$, $V_{top} \geq 0$ and $V_{bot} \geq 0$ must be ensured, to match the dc voltage U_{dc} and provide unipolar voltages to the two main bridges. Thus the reinjection voltage $u_j = V_{bot}$ can be controlled to output any level voltage of the m possible levels.

A particular $u_j = iV_L$ $(i = 1, 2, \cdots, m-1)$ can be generated by a large number of possible switching state combinations, for example; if $m \geq 3$ the total number of possible switching state combinations is $3^{(m-1)}$ for the top and bottom groups.

As an example Table 4.7 shows for m=4, all possible combinations for the bottom group, the number of possible switching state combinations to generate a particular output level being:

$$u_j = 3V_L \quad \left\{ \begin{array}{c} V_{top} = 0 \\ V_{bot} = 3V_L \end{array} \right\} \quad \begin{array}{l} \text{7 combinations for group } BH_B \text{ and} \\ \text{1 combination for group } BH_A; \end{array}$$

$$u_j = 2V_L \quad \left\{ \begin{array}{c} V_{top} = V_L \\ V_{bot} = 2V_L \end{array} \right\} \quad \begin{array}{l} \text{6 combinations for group } BH_B \text{ and} \\ \text{3 combinations for group } BH_A; \end{array}$$

$$u_j = V_L \quad \left\{ \begin{array}{c} V_{top} = 2V_L \\ V_{bot} = V_L \end{array} \right\} \quad \begin{array}{l} \text{3 combinations for group } BH_B \text{ and} \\ \text{6 combinations for group } BH_A; \end{array}$$

$$u_j = 0 \quad \left\{ \begin{array}{c} V_{top} = 3V_L \\ V_{bot} = 0 \end{array} \right\} \quad \begin{array}{l} \text{1 combinations for group } BH_B \text{ and} \\ \text{7 combinations for group } BH_A; \end{array}$$

Usable Combinations

V_{bot}	0	0	0	0	0	0	0	1	1	1	1	1	1	2	2	2	3
V_{A1}	0	0	0	1	1	−1	−1	0	0	1	1	1	−1	0	1	1	1
V_{A2}	0	1	−1	0	−1	0	1	0	1	0	1	−1	1	1	0	1	1
V_{A3}	0	−1	1	−1	0	1	0	1	0	0	−1	1	1	1	1	0	1

Unusable Combinations

V_{bot}	−1	−1	−1	−1	−1	−1	−2	−2	−2	−3
V_{A1}	0	0	1	−1	−1	−1	0	−1	−1	−1
V_{A2}	0	−1	−1	0	1	−1	−1	0	−1	−1
V_{A3}	−1	0	−1	0	−1	1	−1	−1	0	−1

Table 4.7 Switching State Combinations of 3 H-Bridges

With larger m, the total number of possible switching state combinations increases sharply and so does the number of switching state combinations able to be used to generate a particular level. Thus by choosing the appropriate combinations for every

required level the voltage of every capacitor in the H-bridges can be controlled, i.e. the capacitor voltage can be maintained at the required value. The great number of redundant switching state combinations makes the selection of the optimized combinations very difficult, a matter that requires further investigation.

The number of the switches required by the H-Bridge Controllable Voltage Divider structure is proportional to the level number m [$N_{MLCHB} = 8(m-1)$]. However proportionality factor of 8 is too high, and only a sizeable reduction will make this alternative acceptable.

4.4 CONCLUSIONS

This chapter has discussed the generation of the voltage reinjection waveforms. Different types of the controllable dc voltage dividers have been investigated in terms of topology, number of switches required and control flexibility. The conclusions are given as follows:

1. The multi-level fully symmetrical voltage reinjection waveforms can be generated by a controllable voltage divider without the need for isolation transformers. The two main bridges have to be connected in series if they are powered by this controllable voltage divider.

2. For high voltage application the capacitors have to be series connected to share the high dc voltage, only additional power switches required to form the controllable divider add to the converter cost; and also these switches are not involved in the dc current path, their current ratings are relatively low as compared with the main bridge switches.

3. The MLDC-VSC (Multi-Level Diode Clamping VSC), MLASC-VSC (Multi-Level Asymmetrical Switch Clamping VSC), BGASMP-VSC (Binary Grouped Asymmetrical Switch Multi-Path VSC), MLCC-VSC (Multi-Level Capacitor Clamping VSC) and MLCHB-VSC (Multi-Level Cascaded H-bridge VSC) can all be used as the controllable voltage divider.

4. The controllable voltage divider based on the MLASC-VSC or BGASMP-VSC topological structures uses less switches, but presents capacitor voltage balancing problems.

5. The controllable voltage divider based on the MLCC-VSC or MLCHB-VSC topological structures uses more clamping capacitors for the MLCC-VSC and more switches for the MLCHB-VSC, but presents no capacitor voltage balancing problems.

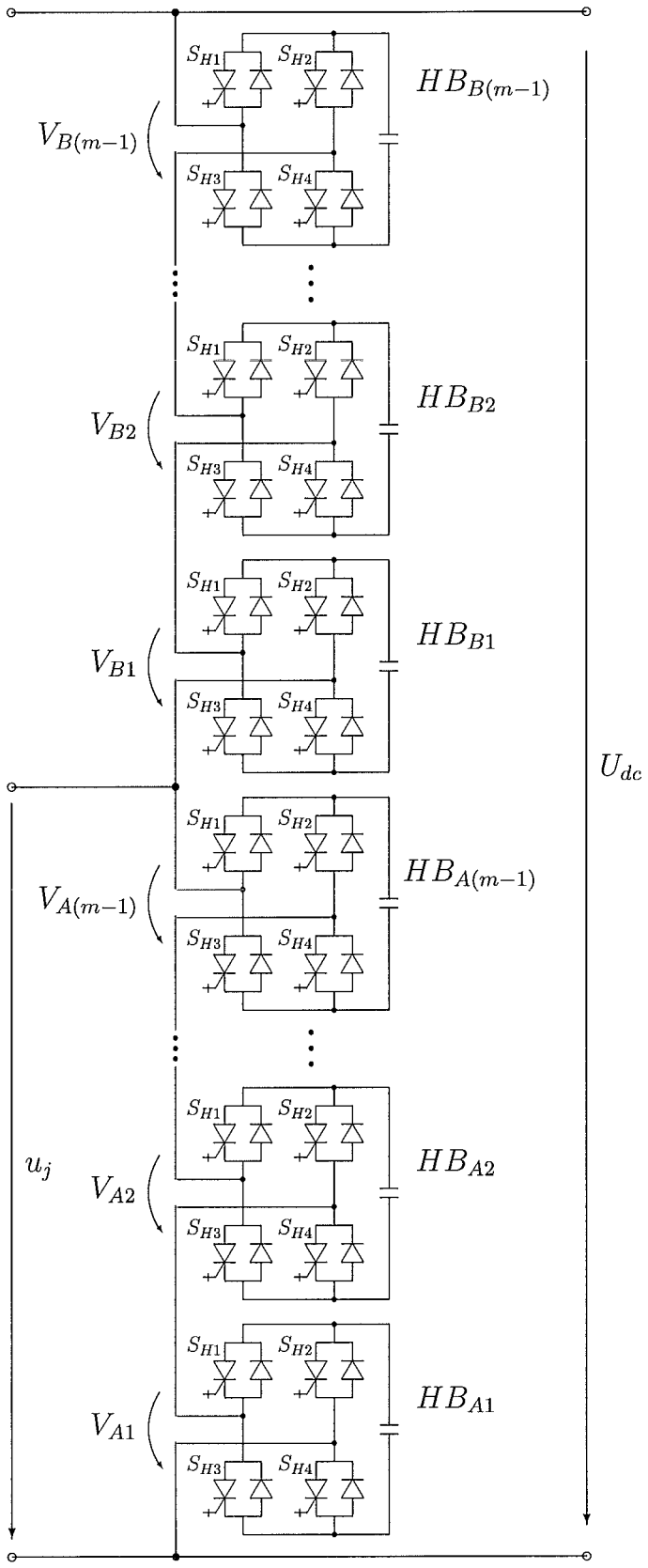


Figure 4.7 The Controllable H-Bridge Voltage Divider

Chapter 5

ANALYSIS OF THE MLVR–VSC

5.1 INTRODUCTION

Among the multi-level dc voltage reinjection (MLVR) circuits discussed in the previous chapter, the asymmetrical switch clamped VSC (MLASC-VSC) structure seems to be the most attractive configuration for generating the required reinjection waveforms, because for level numbers greater than five the harmonic content of the MLVR-VSC is well within the present standards and the MLASC-VSC structure uses fewer switching devices than the MLDC-VSC, MLCC-VSC and MLCHB-VSC configurations.

For high voltage and high power application, low reinjection levels result in high level voltage ($V_L = U_{dc}/[m-1]$), and require several switches connected in series to withstand the high level voltage. However, the level voltage can not be very high to limit dV/dt and achieve dynamic voltage balance of the series connected switches.

Therefore, the choice of level number is a compromise between the use of a high frequency filter for limiting dV/dt and the complicated circuit needed to ensure the dynamic voltage balance of series connected switches in the reinjection waveform generation circuit. For level numbers lower than 10, the MLASC-VSC structure is still the appropriate choice; for very high level numbers the BGASMP-VSC and MLCHB-VSC can be considered, particularly the MLCHB-VSC structure because of the absence of capacitor voltage balance problems.

Regardless of the type of reinjection circuit used to generate the multi-level reinjection voltage, the analysis in this chapter refers to a 12-pulse converter system with the two main bridges supplied by the multi-level reinjection voltage; the common term used is MLVR-VSC and the waveform analysis is general (based on m-level configuration); although all the illustrations in this chapter use the 8-level configuration as the test example.

5.2 OPERATING PRINCIPLE OF THE MLVR-VSC

5.2.1 The Circuit Description

The test MLVR-VSC configuration is based on the basic twelve-pulse converter scheme and uses the MLASC-VSC structure as the reinjection circuit to provide the reinjection voltage waveforms across the two six-pulse converters; the required waveforms were derived in chapter 2.

To simplify the development the following symbols are used to describe the proposed MLVR-VSC configuration: m is the level number, U_{dc} is the dc source voltage, and the dc voltage across the two series connected 6-pulse bridges; $V_L = \frac{U_{dc}}{m-1}$ is the voltage across every dc capacitor in the capacitor bank; V_L is also used as the standard nominal voltage unit both for the dc capacitors and for the switching devices in the main bridges and reinjection circuit.

In the illustrated MLVR-VSC, (shown in Figure 5.1 for an example of 8 levels), the dc side capacitor is split into $(m-1)$ cascade connected units to provide the m accessible voltage levels. The GTO-Diode pair valves connected to the capacitor bank and the dc capacitors form a controllable multi-level voltage divider. By turning on the appropriate pairs, i.e. providing a unique path from the reinjection circuit output terminal u_j to the required voltage level, the reinjection circuit output voltage u_j can be any of the possible m voltage levels.

The upper dc output terminal of the bridge connected to the Y/Δ interface transformer is permanently connected to the highest voltage level, while the lower dc output terminals of the bridge connected to the Y/Y interface transformer is permanently connected to the lowest voltage level. The second terminal of each bridge is connected to the reinjection circuit output terminal u_j. Thus the voltages across the two bridges can be adjusted simultaneously by controlling u_j, the reinjection circuit output voltage. This connection arrangement ensures that the fully symmetrical linear reinjection waveforms are supplied to the two main bridges.

Since the level voltage V_L is defined as the standard nominal voltage unit for the capacitors and switching devices, each switching arm in the two main bridges consists of $m-1$ standard switching devices to withstand the highest voltage across them $[U_{dc} = (m-1)V_L)]$. In Figure 5.1, which illustrates the $m = 8$ configuration, the switching symbol of every arm in the main bridges (i.e. $S_{\Delta 1}$ to $S_{\Delta 6}$ and S_{Y1} to S_{Y6}) represents $m-1 = 7$ series connected power switch units to withstand the high voltage.

On the other hand, the voltages across the reinjection switch branches depend on their position in the reinjection circuit network, as described in chapter 4. Therefore, for clarity each of the reinjection switches in Figure 5.1 (i.e. S_{j1} to S_{j14} connected in series to withstand the high voltage) and (S_{h1}, S_{h21}, $\cdots$, S_{h6} used to provide the controllable clamping paths to the levels) represents a power switch unit.

To reduce the number of switches, the reinjection switches (S_{j4} to S_{j11}) in Figure 5.1 are common to the different paths from the reinjection output terminals to some of the required levels. Thus these switches can not be directly clamped to the corresponding levels and need to use large resistors in parallel to balance the steady state voltage; their dynamic voltage balance can be achieved by asynchronous firing control to ensure the voltage increment across them is the level voltage V_L.

However the current ratings of the main bridge and reinjection switches are different due to the reinjection switch currents being only the ac components of the bridge output currents. Moreover, for very high voltage applications and relative low level numbers, the level voltage V_L will be higher than the rating of presently available switching devices, thus each switch symbol represents a chain of series-connected power switches with steady and dynamic voltage balance accessories.

Comparing the proposed MLVR-VSC with the conventional 12-pulse VSC where the two main bridges are supplied by the same dc voltage source, the much higher quality output waveform avoids the need for lower order harmonic filters and the filters used to overcome the high dv/dt problems; also the controllable zero voltage switching condition simplifies the main bridge structure by eliminating the complicated circuits used for the switching dynamic voltage balancing and the snubbers for absorbing the stray inductive and parasitic capacitive energy.

Unlike the present multi-level diode clamped voltage source converter (MLDC-VSC), where the clamping diodes are an integral part of the power circuit, in the proposed MLVR-VSC the power conversion (main bridges) and pulse-forming (reinjection circuit) circuits are kept separate. Both configurations use the same dc voltage source paralleled with $m-1$ series connected capacitors (where m is the level number), and in both cases the fundamental frequency modulation control is used to reduce the switching frequency. The two configurations require the same number of main switches $[12(m-1)]$; however while the 12-pulse MLDC-VSC requires $6(m-1)(m-2)$ clamping diodes, the MLVR-VSC reinjection circuit needs $\frac{(m-1)(m+7)-1}{4}$ (for even m) or $\frac{(m-1)(m+9)}{4}$ (for odd m) extra lower current rating switches.

As an example the MLVR-VSC shown in Figure 5.1, has 84 main switches and 26 reinjection switches; whereas the 12-pulse MLDC-VSC requires 84 main switches and 256 clamping diodes as well as a complex network of high voltage connections. One phase-pole of the later configuration is shown in Figure 5.2, the complete configuration having six of these phase poles.

5.2.2 The Firing Control of MLVR-VSC

The m-level reinjection circuit in the MLVR-VSC, functions as a controllable voltage divider, and provides m possible voltage levels to the two main bridge common node (neutral point). By proper firing control of the reinjection switches the voltage divider

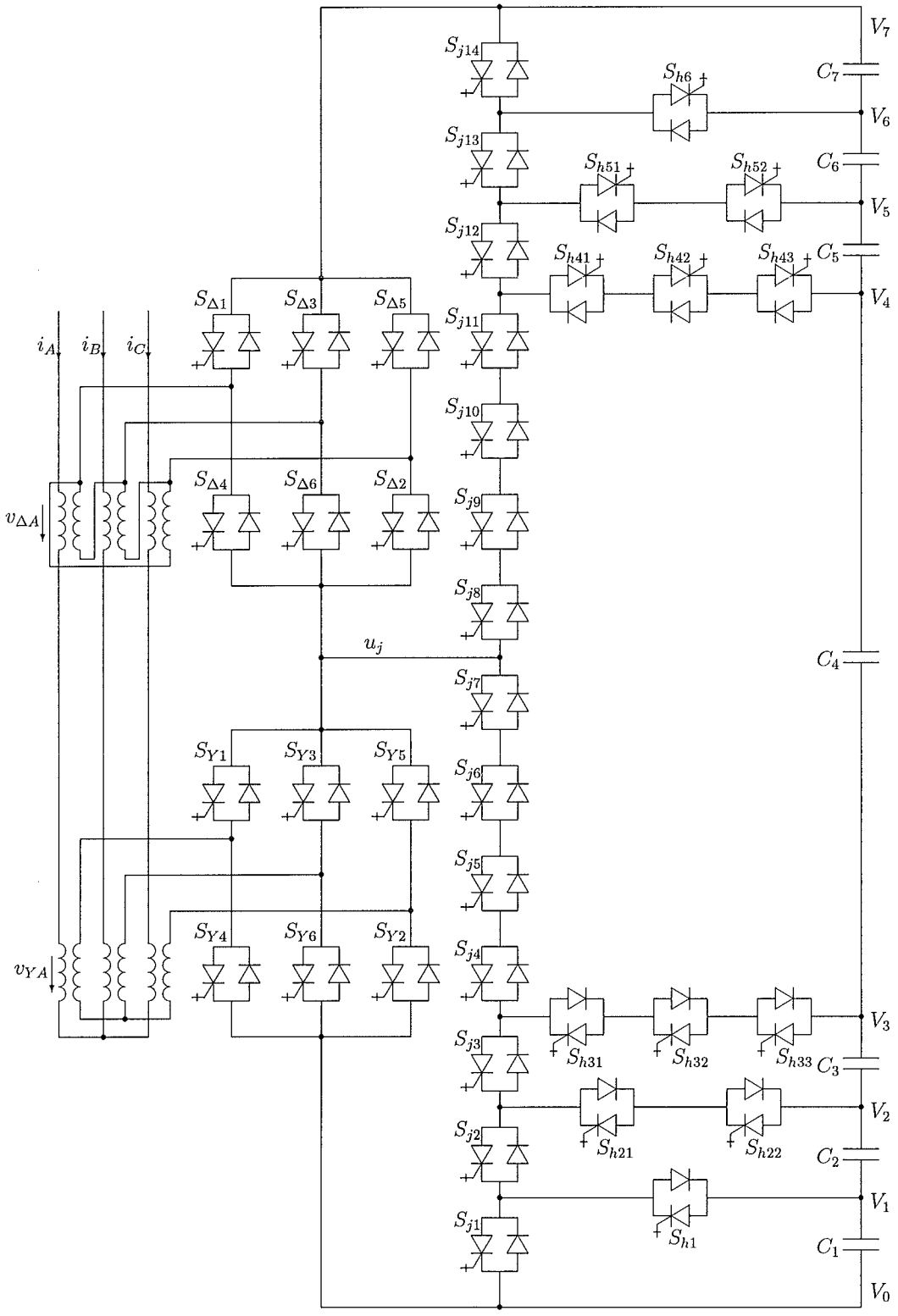


Figure 5.1 The Basic Structure of 8-level MLVR-VSC

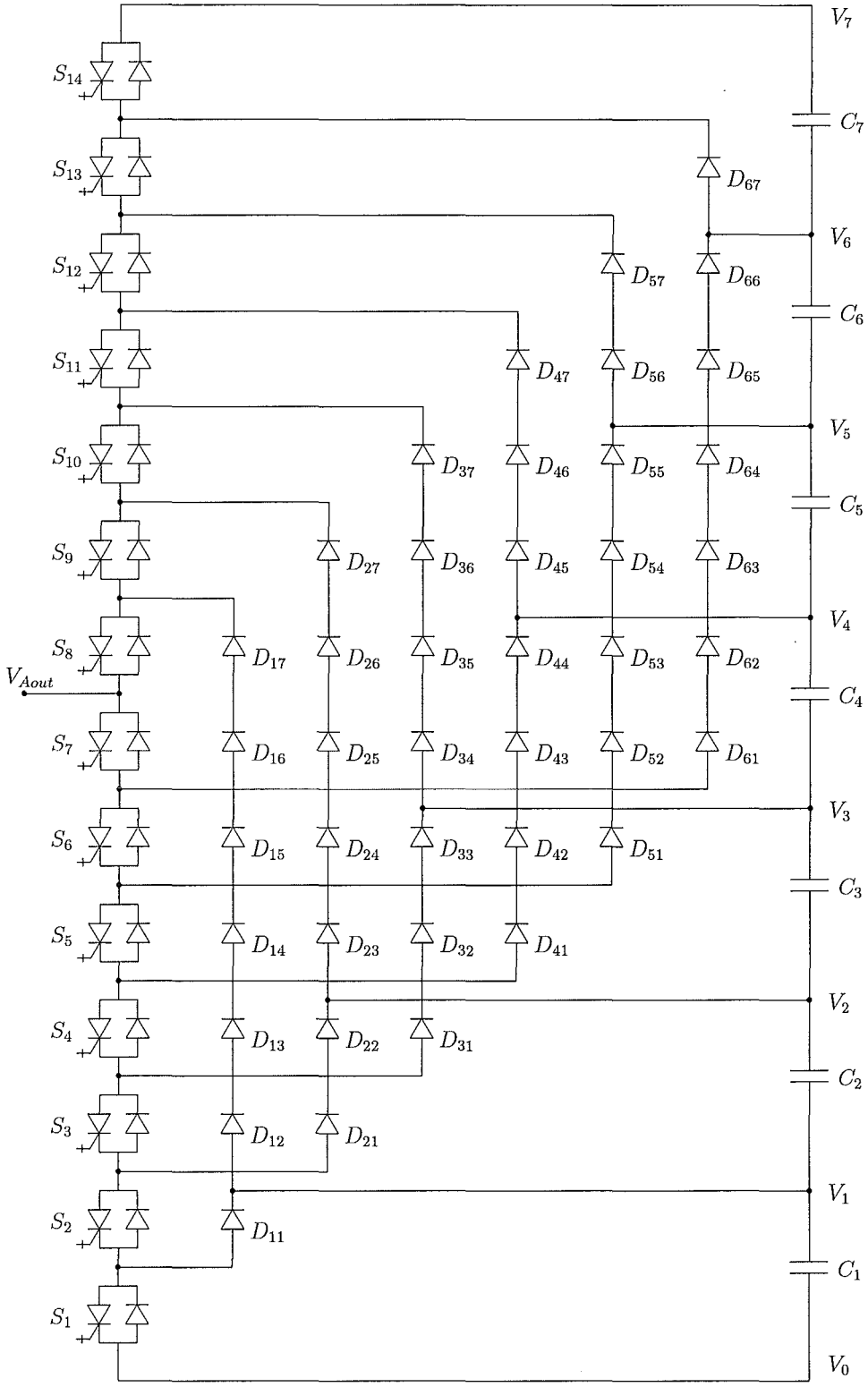


Figure 5.2 One Phase-pole of an 8-level MLDC-VSC

outputs the required reinjection voltage u_j. The voltages across the two main bridges are determined by the dc voltage U_{dc} and the reinjection voltage u_j (referring to Figure 5.1), thus to produce the required voltages at each of the main bridge ac output terminals the main bridge switches must be controlled synchronously with the reinjection switches.

To generate the required level of the reinjection voltage u_j, a switching path between the reinjection circuit output terminal and the required level has to be provided. There are m possible switching paths between the m level nodes and the reinjection circuit output terminal $(S_1, S_2, \cdots, S_m)$, and at any instance only one switching path is in ON-state (opening) while all of others are OFF-state (blocking). For the example scheme of $m = 8$ in Figure 5.1, the following switch combinations are used to provide the bidirectional current paths between the neutral point and the required levels to generate the reinjection voltage (u_j):

$u_j = v_0$ (S_{j1} to S_{j7}) are ON and the remaining switches OFF
(referred as switching path S_1)

$u_j = v_1$ (S_{j2} to S_{j7} and S_{h1}) are ON and the remaining switches OFF
(referred as switching path S_2)

$u_j = v_2$ (S_{j3} to S_{j7} and S_{h21} to S_{h22}) are ON and the remaining switches OFF
(referred as switching path S_3)

$u_j = v_3$ (S_{j4} to S_{j7} and S_{h31} to S_{h33}) are ON and the remaining switches OFF
(referred as switching path S_4)

$u_j = v_4$ (S_{j8} to S_{j11} and S_{h41} to S_{h43}) are ON and the remaining switches OFF
(referred as switching path S_5)

$u_j = v_5$ (S_{j8} to S_{j12} and S_{h51} to S_{h52}) are ON and the remaining switches OFF
(referred as switching path S_6)

$u_j = v_6$ (S_{j8} to S_{j13} and S_{h61}) are ON and the remaining switches OFF
(referred as switching path S_7)

$u_j = v_7$ (S_{j8} to S_{j14}) are ON and the remaining switches OFF
(referred as switching path S_8)

To generate the required reinjection voltage waveforms in real time, the m switching paths need to be controlled in a particular time sequence. The linearly increasing and decreasing reinjection waveform requires the following time sequence of the switching paths for the m-level waveform $[\cdots, S_2, S_1, S_2, \cdots, S_{m-1}, S_m, S_{m-1}, \cdots, S_2, S_1, S_2, \cdots]$. The simplest firing control logic of the switching paths is the use of an equal interval for every switching path, thus depending on the requirement of the linear reinjection

waveforms, every reinjection switching path in the sequence is in ON-state for $\frac{\pi}{6(m-1)}$ (in radian) or $\frac{30^o}{(m-1)}$ (in degree).

Figure 5.3 illustrates the firing control of the MLVR-VSC system. There are three concentric annuluses representing the on-state combinations of the three groups of switches in Figure 5.1. The center one is divided into six equal sectors to express the six on-state combinations of the six valves (S_{Y1} to S_{Y6}) in the main bridge connected to the Y/Y connection transformer; the middle one is also divided into six equal sectors to express the six on-state combinations of the six valves ($S_{\Delta 1}$ to $S_{\Delta 6}$) in the main bridge connected to the Y/Δ connection transformer; the third one is divided equally into $12(m-1)$ sectors, and every $2(m-1)$ sectors forms a group, that corresponds to an on-state sequence of the reinjection switches.

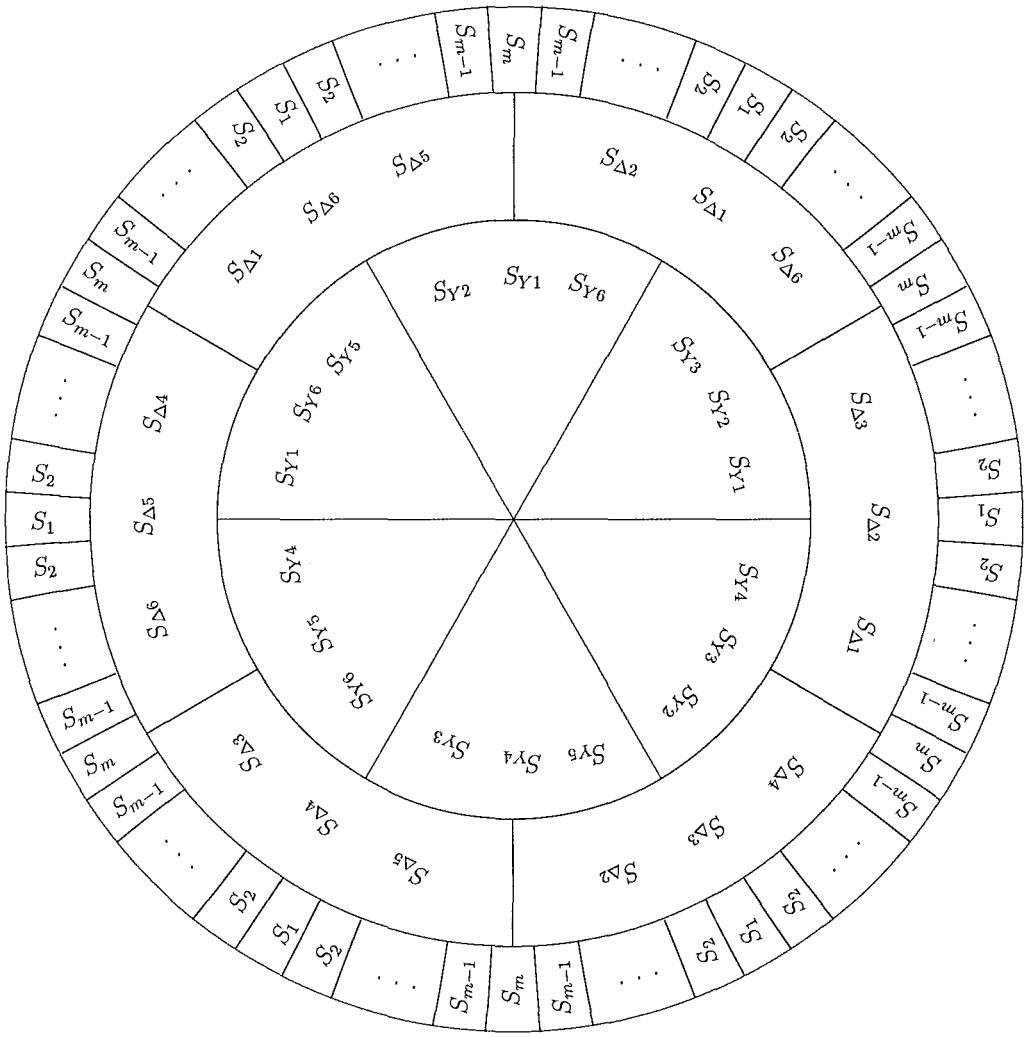


Figure 5.3 Firing Sequence of the Proposed MLVR-VSC

The on-state combinations denoted by the three concentric annuluses rotate in the clockwise direction corresponding to the switch state changes in the time domain; at any

instant, i.e. at any angle position of a rotating vector, the on-state combinations of the three switch groups can be determined by the switches that appear in the appropriate area where the vector is located, otherwise the switches are in the off-state.

To synchronize the reinjection path control sequence with the firing control sequence of the main bridge switches and to meet the main bridges zero voltage commutation condition, the two main bridge switches and the reinjection switching paths firing control are arranged such that the main bridge switch commutations take place at the center of the zero voltage interval. This is achieved by clamping the corresponding bridges for a time interval, i.e. opening the switching paths S_1 to clamp the Y/Y bridge or S_m to clamp the Y/Δ bridge.

This arrangement is illustrated in Figure 5.3, where the middle of the S_1 sectors coincides with the boundary between the sectors of the center annulus; that means that the commutation of the Y/Y bridge takes place at the center of the time interval, in which the reinjection path S_1 is in on-state; similarly every middle of the S_m sectors corresponds to a commutation in the Y/Δ bridge. When the reinjection switching path S_1 is in on-state, the Y/Y bridge is short-circuited; while when S_m is in on-state, the Y/Δ bridge is short-circuited; thus the zero voltage commutation condition is always achieved for the switches in the main bridges.

The two standard six-pulse bridges in the MLVR-VSC are controlled exactly the same way as in the conventional 12-pulse converter. Thus the firing control logic of the main bridge is independent on the level number m, only the reinjection switching control logic complexity increases with the level number.

5.3 ANALYSIS OF VOLTAGE WAVEFORMS

To simplify the description the voltage waveforms of the MLVR-VSC are derived under the following ideal conditions: the capacitances of all the dc side series connected capacitors are infinite; the on-state voltage drop of all forced-commutated switches in the system is zero; the off-state impedance of all forced-commutated switches is infinite; all the freewheeling diodes are ideal diodes; the leakage reactance of the main transformers is negligible. The turns ratios of the interface transformers are the same as those of the conventional 12-pulse converter, i.e. $N_1 : N_2 = k_n$ for the Y/Y connected transformer and $N_1 : \sqrt{3}N_2 = kn/\sqrt{3}$ for the Y/Δ connected transformer respectively. The dc supply voltage U_{dc} is equally shared by the (m-1) series connected capacitors. The voltages across all capacitors are constant and will have the same value $V_L = U_{dc}/(m-1)$ at any instant under the assumption of the infinite capacitance.

The voltage waveforms of the proposed MLVR-VSC for an 8-level example are shown in Figure 5.4. These are

- (a) V_{YY}/U_{dc}, Voltage across the bridge connected to the Y/Y interface transformer
- (b) $V_{Y\Delta}/U_{dc}$, Voltage across the bridge connected to the Y/Δ interface transformer
- (c) V_{YA}/U_{dc}, Voltage across the primary winding of the Y/Y interface transformer
- (d) $V_{\Delta A}/U_{dc}$, Voltage across the primary winding of the Y/Δ interface transformer
- (e) V_A/U_{dc}, Output AC Voltage of the proposed converter
- (f) The output voltage spectrum of the proposed converter

It is clearly shown in Figures 5.4 (a) and (b), that the voltages across the two main bridges are changed every 60^o in the sequence [0, V_L, $2V_L$, $\cdots$ $(m-1)V_L$, $(m-2)V_L$, $\cdots$, V_L, 0], increased and decreased step by step; and zero voltages occur around the points (0^o, 60^o, 120^o, 180^o, 240^o, 300^o, 360^o) and (30^o, 90^o, 150^o, 210^o, 270^o, 330^o) for the Y/Y and Y/Δ connection bridges respectively. As the switch commutations of the main bridges take place at these points, zero voltage switching is achieved.

The m-level reinjection voltage that changes every $30^o/(m-1)$ level by level is applied to the two main bridges, and this level by level varying voltage is distributed to the interface transformer secondary windings via the on-state switches in the main bridges. V_{Ya} the voltage across the secondary phase 'a' winding (bridge side) of the Y/Y connection interface transformer is part of the voltage across the bridge: one third in the interval 0^o to 60^o; two third in the interval 60^o to 120^o; one third in the interval 120^o to 180^o; from 180^o to 360^o it is a repetition of the voltage in the period from 0^o to 180^o but in reverse direction.

A secondary winding of the Y/Δ connection interface transformer is directly connected to the bridge terminal through the on-state valves or short circuited by the on-state valves, thus $V_{\Delta a}$ the voltage across the secondary phase 'a' winding of the Y/Δ connection interface transformer is the voltage across the bridge or zero: zero in the interval 0^o to 30^o; the bridge voltage in the interval 30^o to 150^o; zero in the interval 150^o to 180^o; from 180^o to 360^o it is a repetition of the voltage in the period from 0^o to 180^o but in reverse direction.

The primary (power system side) phase 'a' voltages V_{YA} and $V_{\Delta A}$ coupled from the secondary winding voltages V_{Ya} and $V_{\Delta a}$ are shown in Figure 5.4 (c) and (d), and their sum forms the reinjection converter system output voltage V_A (shown in Figure 5.4 (e)).

The general expressions for the proposed MLVR-VSC with the reinjection voltage being m-level, and dc voltage U_{dc} equally divided into $V_L = U_{dc}/(m-1)$ levels can be derived from:

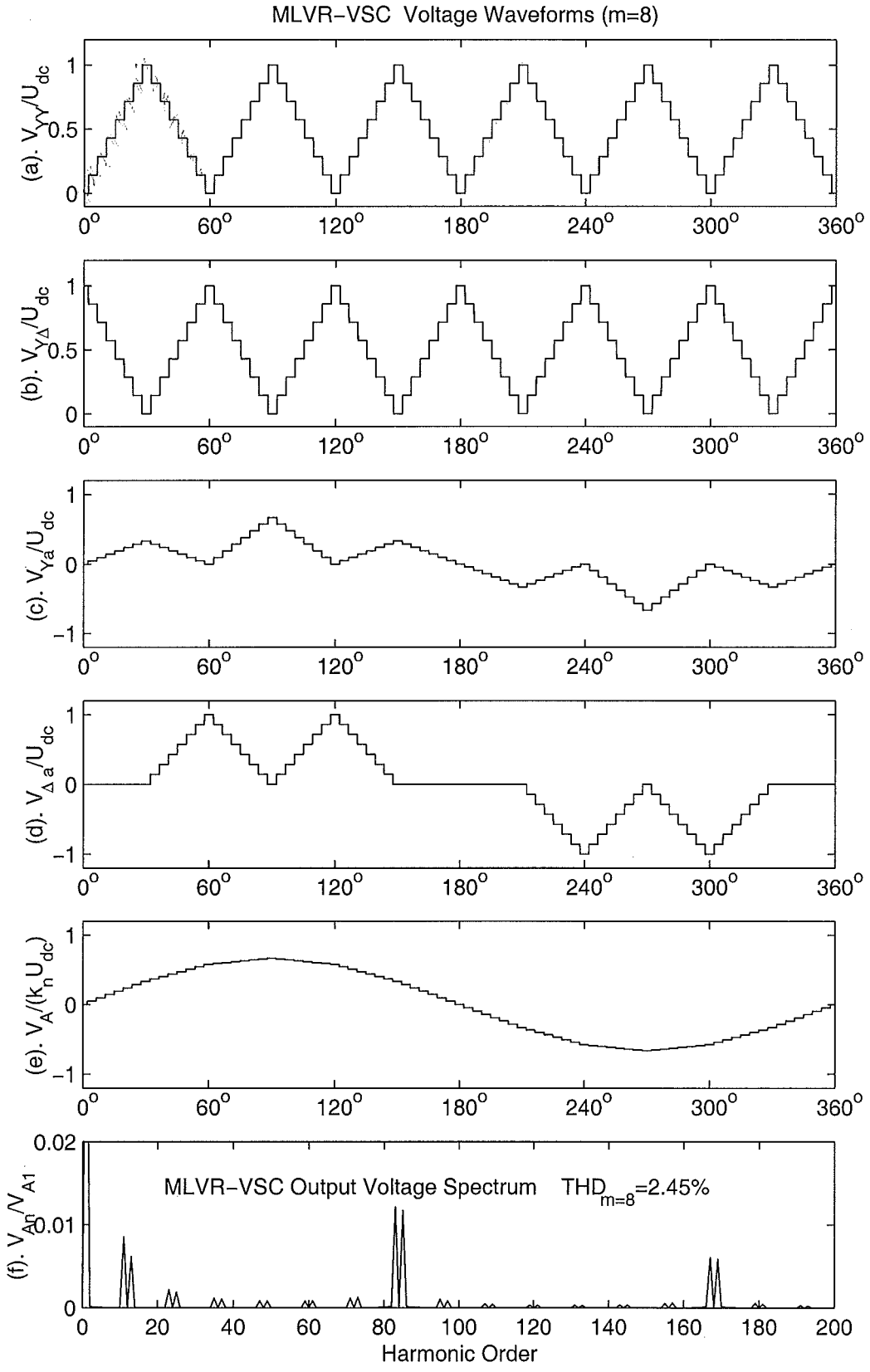


Figure 5.4 Voltage Waveforms of 8-Level MLVR-VSC

the voltage across the Y/Y connection bridge

$$V_{YY}(\omega t)=\begin{cases} iV_L & \frac{(2i-1)\pi}{12(m-1)}<\omega t<\frac{(2i+1)\pi}{12(m-1)} & i=0,1,\cdots,m-1 \\ (m-i-1)V_L & \frac{(2i-1)\pi}{12(m-1)}+\frac{\pi}{6}<\omega t<\frac{(2i+1)\pi}{12(m-1)}+\frac{\pi}{6} & i=1,2,\cdots,m-1 \\ iV_L & \frac{(2i-1)\pi}{12(m-1)}+\frac{\pi}{3}<\omega t<\frac{(2i+1)\pi}{12(m-1)}+\frac{\pi}{3} & i=1,2,\cdots,m-1 \\ (m-i-1)V_L & \frac{(2i-1)\pi}{12(m-1)}+\frac{\pi}{2}<\omega t<\frac{(2i+1)\pi}{12(m-1)}+\frac{\pi}{2} & i=1,2,\cdots,m-1 \\ iV_L & \frac{(2i-1)\pi}{12(m-1)}+\frac{2\pi}{3}<\omega t<\frac{(2i+1)\pi}{12(m-1)}+\frac{2\pi}{3} & i=1,2,\cdots,m-1 \\ (m-i-1)V_L & \frac{(2i-1)\pi}{12(m-1)}+\frac{5\pi}{6}<\omega t<\frac{(2i+1)\pi}{12(m-1)}+\frac{5\pi}{6} & i=1,2,\cdots,m-1 \\ iV_L & \frac{(2i-1)\pi}{12(m-1)}+\pi<\omega t<\frac{(2i+1)\pi}{12(m-1)}+\pi & i=1,2,\cdots,m-1 \\ (m-i-1)V_L & \frac{(2i-1)\pi}{12(m-1)}+\frac{7\pi}{6}<\omega t<\frac{(2i+1)\pi}{12(m-1)}+\frac{7\pi}{6} & i=1,2,\cdots,m-1 \\ iV_L & \frac{(2i-1)\pi}{12(m-1)}+\frac{4\pi}{3}<\omega t<\frac{(2i+1)\pi}{12(m-1)}+\frac{4\pi}{3} & i=1,2,\cdots,m-1 \\ (m-i-1)V_L & \frac{(2i-1)\pi}{12(m-1)}+\frac{3\pi}{2}<\omega t<\frac{(2i+1)\pi}{12(m-1)}+\frac{3\pi}{2} & i=1,2,\cdots,m-1 \\ iV_L & \frac{(2i-1)\pi}{12(m-1)}+\frac{5\pi}{3}<\omega t<\frac{(2i+1)\pi}{12(m-1)}+\frac{5\pi}{3} & i=1,2,\cdots,m-1 \\ (m-i-1)V_L & \frac{(2i-1)\pi}{12(m-1)}+\frac{11\pi}{6}<\omega t<\frac{(2i+1)\pi}{12(m-1)}+\frac{11\pi}{6} & i=1,2,\cdots,m-1 \end{cases} \tag{5.1}$$

and the voltage across the Y/Δ connection bridge

$$V_{Y\Delta}(\omega t)=\begin{cases} (m-i-1)V_L & \frac{(2i-1)\pi}{12(m-1)}<\omega t<\frac{(2i+1)\pi}{12(m-1)} & i=0,1,\cdots,m-1 \\ iV_L & \frac{(2i-1)\pi}{12(m-1)}+\frac{\pi}{6}<\omega t<\frac{(2i+1)\pi}{12(m-1)}+\frac{\pi}{6} & i=1,2,\cdots,m-1 \\ (m-i-1)V_L & \frac{(2i-1)\pi}{12(m-1)}+\frac{\pi}{3}<\omega t<\frac{(2i+1)\pi}{12(m-1)}+\frac{\pi}{3} & i=1,2,\cdots,m-1 \\ iV_L & \frac{(2i-1)\pi}{12(m-1)}+\frac{\pi}{2}<\omega t<\frac{(2i+1)\pi}{12(m-1)}+\frac{\pi}{2} & i=1,2,\cdots,m-1 \\ (m-i-1)V_L & \frac{(2i-1)\pi}{12(m-1)}+\frac{2\pi}{3}<\omega t<\frac{(2i+1)\pi}{12(m-1)}+\frac{2\pi}{3} & i=1,2,\cdots,m-1 \\ iV_L & \frac{(2i-1)\pi}{12(m-1)}+\frac{5\pi}{6}<\omega t<\frac{(2i+1)\pi}{12(m-1)}+\frac{5\pi}{6} & i=1,2,\cdots,m-1 \\ (m-i-1)V_L & \frac{(2i-1)\pi}{12(m-1)}+\pi<\omega t<\frac{(2i+1)\pi}{12(m-1)}+\pi & i=1,2,\cdots,m-1 \\ iV_L & \frac{(2i-1)\pi}{12(m-1)}+\frac{7\pi}{6}<\omega t<\frac{(2i+1)\pi}{12(m-1)}+\frac{7\pi}{6} & i=1,2,\cdots,m-1 \\ (m-i-1)V_L & \frac{(2i-1)\pi}{12(m-1)}+\frac{4\pi}{3}<\omega t<\frac{(2i+1)\pi}{12(m-1)}+\frac{4\pi}{3} & i=1,2,\cdots,m-1 \\ iV_L & \frac{(2i-1)\pi}{12(m-1)}+\frac{3\pi}{2}<\omega t<\frac{(2i+1)\pi}{12(m-1)}+\frac{3\pi}{2} & i=1,2,\cdots,m-1 \\ (m-i-1)V_L & \frac{(2i-1)\pi}{12(m-1)}+\frac{5\pi}{3}<\omega t<\frac{(2i+1)\pi}{12(m-1)}+\frac{5\pi}{3} & i=1,2,\cdots,m-1 \\ iV_L & \frac{(2i-1)\pi}{12(m-1)}+\frac{11\pi}{6}<\omega t<\frac{(2i+1)\pi}{12(m-1)}+\frac{11\pi}{6} & i=1,2,\cdots,m-1 \end{cases} \tag{5.2}$$

The converter side phase winding voltage of the Y/Y connection interface transformer

is given by

$$V_{Ya}(\omega t)=\begin{cases}
\frac{iV_L}{3} & \frac{(2i-1)\pi}{12(m-1)}<\omega t<\frac{(2i+1)\pi}{12(m-1)} & i=0,1,\cdots,m-1\\
\frac{(m-i-1)V_L}{3} & \frac{(2i-1)\pi}{12(m-1)}+\frac{\pi}{6}<\omega t<\frac{(2i+1)\pi}{12(m-1)}+\frac{\pi}{6} & i=1,2,\cdots,m-1\\
\frac{2iV_L}{3} & \frac{(2i-1)\pi}{12(m-1)}+\frac{\pi}{3}<\omega t<\frac{(2i+1)\pi}{12(m-1)}+\frac{\pi}{3} & i=1,2,\cdots,m-1\\
\frac{2(m-i-1)V_L}{3} & \frac{(2i-1)\pi}{12(m-1)}+\frac{\pi}{2}<\omega t<\frac{(2i+1)\pi}{12(m-1)}+\frac{\pi}{2} & i=1,2,\cdots,m-1\\
\frac{iV_L}{3} & \frac{(2i-1)\pi}{12(m-1)}+\frac{2\pi}{3}<\omega t<\frac{(2i+1)\pi}{12(m-1)}+\frac{2\pi}{3} & i=1,2,\cdots,m-1\\
\frac{(m-i-1)V_L}{3} & \frac{(2i-1)\pi}{12(m-1)}+\frac{5\pi}{6}<\omega t<\frac{(2i+1)\pi}{12(m-1)}+\frac{5\pi}{6} & i=1,2,\cdots,m-1\\
\frac{-iV_L}{3} & \frac{(2i-1)\pi}{12(m-1)}+\pi<\omega t<\frac{(2i+1)\pi}{12(m-1)}+\pi & i=1,2,\cdots,m-1\\
\frac{-(m-i-1)V_L}{3} & \frac{(2i-1)\pi}{12(m-1)}+\frac{7\pi}{6}<\omega t<\frac{(2i+1)\pi}{12(m-1)}+\frac{7\pi}{6} & i=1,2,\cdots,m-1\\
\frac{-2iV_L}{3} & \frac{(2i-1)\pi}{12(m-1)}+\frac{4\pi}{3}<\omega t<\frac{(2i+1)\pi}{12(m-1)}+\frac{4\pi}{3} & i=1,2,\cdots,m-1\\
\frac{-2(m-i-1)V_L}{3} & \frac{(2i-1)\pi}{12(m-1)}+\frac{3\pi}{2}<\omega t<\frac{(2i+1)\pi}{12(m-1)}+\frac{3\pi}{2} & i=1,2,\cdots,m-1\\
\frac{-iV_L}{3} & \frac{(2i-1)\pi}{12(m-1)}+\frac{5\pi}{3}<\omega t<\frac{(2i+1)\pi}{12(m-1)}+\frac{5\pi}{3} & i=1,2,\cdots,m-1\\
\frac{-(m-i-1)V_L}{3} & \frac{(2i-1)\pi}{12(m-1)}+\frac{11\pi}{6}<\omega t<\frac{(2i+1)\pi}{12(m-1)}+\frac{11\pi}{6} & i=1,2,\cdots,m-1
\end{cases} \tag{5.3}$$

and the Fourier components of $V_{Ya}(\omega t)$ are

$$\begin{aligned}
V_{Yan}&=\frac{2}{\pi}\int_0^{\pi}V_{YA}(\omega t)\sin(n\omega t)d(\omega t)\\
&=\frac{8[1-(-1)^n]U_{dc}}{\sqrt{3}n\pi(m-1)}\sin[\frac{n\pi}{12(m-1)}]\cos(\frac{n\pi}{6})\Big[\sum_{i=1}^{m-1}i\sin(\frac{n\pi}{6}+\frac{in\pi}{6(m-1)})\\
&\quad+2\sum_{i=1}^{m-1}i\sin(\frac{n\pi}{6})\cos(\frac{in\pi}{6(m-1)})\Big] \qquad for\ \ m\geq 3,\ \ n=1,2,3,\cdots
\end{aligned} \tag{5.4}$$

The converter side phase winding voltage of the Y/Δ connection interface transformer

is given by

$$V_{\Delta a}(\omega t)=\begin{cases} 0 & 0<\omega t<\frac{\pi}{6}-\frac{\pi}{12(m-1)} \\ iV_L & \frac{(2i-1)\pi}{12(m-1)}+\frac{\pi}{6}<\omega t<\frac{(2i+1)\pi}{12(m-1)}+\frac{\pi}{6} \quad i=0,1,\cdots,m-1 \\ (m-i-1)V_L & \frac{(2i-1)\pi}{12(m-1)}+\frac{\pi}{3}<\omega t<\frac{(2i+1)\pi}{12(m-1)}+\frac{\pi}{3} \quad i=1,2,\cdots,m-1 \\ iV_L & \frac{(2i-1)\pi}{12(m-1)}+\frac{\pi}{2}<\omega t<\frac{(2i+1)\pi}{12(m-1)}+\frac{\pi}{2} \quad i=1,2,\cdots,m-1 \\ (m-i-1)V_L & \frac{(2i-1)\pi}{12(m-1)}+\frac{2\pi}{3}<\omega t<\frac{(2i+1)\pi}{12(m-1)}+\frac{2\pi}{3} \quad i=1,2,\cdots,m-1 \\ 0 & \frac{\pi}{12(m-1)}+\frac{5\pi}{6}<\omega t<\pi \\ 0 & \pi<\omega t<\frac{7\pi}{6}+\frac{\pi}{12(m-1)} \\ -iV_L & \frac{(2i-1)\pi}{12(m-1)}+\frac{7\pi}{6}<\omega t<\frac{(2i+1)\pi}{12(m-1)}+\frac{7\pi}{6} \quad i=1,2,\cdots,m-1 \\ -(m-i-1)V_L & \frac{(2i-1)\pi}{12(m-1)}+\frac{4\pi}{3}<\omega t<\frac{(2i+1)\pi}{12(m-1)}+\frac{4\pi}{3} \quad i=1,2,\cdots,m-1 \\ -iV_L & \frac{(2i-1)\pi}{12(m-1)}+\frac{3\pi}{2}<\omega t<\frac{(2i+1)\pi}{12(m-1)}+\frac{3\pi}{2} \quad i=1,2,\cdots,m-1 \\ -(m-i-1)V_L & \frac{(2i-1)\pi}{12(m-1)}+\frac{5\pi}{3}<\omega t<\frac{(2i+1)\pi}{12(m-1)}+\frac{5\pi}{3} \quad i=1,2,\cdots,m-1 \\ 0 & \frac{\pi}{12(m-1)}+\frac{11\pi}{6}<\omega t<2\pi \end{cases} \tag{5.5}$$

and the Fourier components of the waveform $V_{\Delta a}(\omega t)$ are

$$\begin{aligned} V_{\Delta an} &= \frac{2}{\pi}\int_0^{\pi} V_{\Delta a}(\omega t)\sin(n\omega t)d(\omega t) \\ &= \frac{8[1-(-1)^n]U_{dc}}{\sqrt{3}n\pi(m-1)}\sin[\frac{n\pi}{12(m-1)}]\cos(\frac{n\pi}{6})\Big[\sum_{i=1}^{m-2} i\sin(\frac{n\pi}{3}+\frac{in\pi}{6(m-1)}) \\ &\quad +(m-1)\sin(\frac{n\pi}{6})\Big] \qquad for \quad m\geq 3, \quad n=1,2,3,\cdots \end{aligned} \tag{5.6}$$

The converter system output phase voltage $V_A(\omega t)$ is the sum of the voltage $V_{Ya}(\omega t)$ and voltage $V_{\Delta a}(\omega t)$ i.e.

$$V_A(\omega t) = k_n[V_{Ya}(\omega t)+\frac{1}{\sqrt{3}}V_{\Delta a}(\omega t)] \tag{5.7}$$

where k_n is the turns ratio of the Y/Y interface transformer. An alternative way of

expressing it is:

$$\frac{V_A(\omega t)}{k_n V_L}=\begin{cases}
\frac{i}{3} & 0<\omega t<\frac{\pi}{6}-\frac{\pi}{12(m-1)} \\
\frac{m-1-i+i\sqrt{3}}{3} & \frac{(2i-1)\pi}{12(m-1)}+\frac{\pi}{6}<\omega t<\frac{(2i+1)\pi}{12(m-1)}+\frac{\pi}{6} \quad i=0,1,\cdots,m-1 \\
\frac{2i+\sqrt{3}(m-1-i)}{3} & \frac{(2i-1)\pi}{12(m-1)}+\frac{\pi}{3}<\omega t<\frac{(2i+1)\pi}{12(m-1)}+\frac{\pi}{3} \quad i=1,2,\cdots,m-1 \\
\frac{2(m-1-i)+i\sqrt{3}}{3} & \frac{(2i-1)\pi}{12(m-1)}+\frac{\pi}{2}<\omega t<\frac{(2i+1)\pi}{12(m-1)}+\frac{\pi}{2} \quad i=1,2,\cdots,m-1 \\
\frac{i+\sqrt{3}(m-i-1)}{3} & \frac{(2i-1)\pi}{12(m-1)}+\frac{2\pi}{3}<\omega t<\frac{(2i+1)\pi}{12(m-1)}+\frac{2\pi}{3} \quad i=1,2,\cdots,m-1 \\
\frac{m-1-i}{3} & \frac{(2i-1)\pi}{12(m-1)}+\frac{5\pi}{6}<\omega t<\frac{(2i+1)\pi}{12(m-1)}+\frac{5\pi}{6} \quad i=1,2,\cdots,m-1 \\
\frac{-i}{3} & \frac{(2i-1)\pi}{12(m-1)}+\pi<\omega t<\frac{(2i+1)\pi}{12(m-1)}+\pi \quad i=1,2,\cdots,m-1 \\
\frac{-(m-i-1)-\sqrt{3}i}{3} & \frac{(2i-1)\pi}{12(m-1)}+\frac{7\pi}{6}<\omega t<\frac{(2i+1)\pi}{12(m-1)}+\frac{7\pi}{6} \quad i=1,2,\cdots,m-1 \\
\frac{-2i-\sqrt{3}(m-i-1)}{3} & \frac{(2i-1)\pi}{12(m-1)}+\frac{4\pi}{3}<\omega t<\frac{(2i+1)\pi}{12(m-1)}+\frac{4\pi}{3} \quad i=1,2,\cdots,m-1 \\
\frac{-2(m-i-1)-i\sqrt{3}}{3} & \frac{(2i-1)\pi}{12(m-1)}+\frac{3\pi}{2}<\omega t<\frac{(2i+1)\pi}{12(m-1)}+\frac{3\pi}{2} \quad i=1,2,\cdots,m-1 \\
\frac{-i-\sqrt{3}(m-i-1)}{3} & \frac{(2i-1)\pi}{12(m-1)}+\frac{5\pi}{3}<\omega t<\frac{(2i+1)\pi}{12(m-1)}+\frac{5\pi}{3} \quad i=1,2,\cdots,m-1 \\
\frac{-(m-i-1)}{3} & \frac{(2i-1)\pi}{12(m-1)}+\frac{11\pi}{6}<\omega t<\frac{(2i+1)\pi}{12(m-1)}+\frac{11\pi}{6} \quad i=1,2,\cdots,m-1
\end{cases} \tag{5.8}$$

This expression clearly indicates that the reinjection converter system output voltage is a stair case waveform with $12\times(m-1)+1$ steps, and the waveform is equivalent to those of a $12\times(m-1)$-pulse or a $6\times(m-1)$-level system.

Its Fourier components are given by

$$V_{An}=\frac{8[1-(-1)^n]k_nU_{dc}}{3n\pi(m-1)}\sin(\frac{n\pi}{12(m-1)})\cos(\frac{n\pi}{6})\Big[\cos(\frac{n\pi}{6})+\frac{\sqrt{3}}{2}\Big]\Big[(m-1)\sin(\frac{n\pi}{6}) +\sqrt{3}\sum_{i=1}^{m-2}i\sin(\frac{n\pi}{6}+\frac{in\pi}{6(m-1)})-\sum_{i=1}^{m-2}i\sin(\frac{in\pi}{6(m-1)})\Big]$$
$$for \quad m\geq 3, \quad n=1,2,3,\cdots \tag{5.9}$$

The fundamental peak value of the converter system output voltage can be obtained directly from Equation 5.9, i.e.

$$V_{A1}=\frac{16k_nU_{dc}}{\pi(m-1)}\sin(\frac{\pi}{12(m-1)})\Big[\frac{(m-1)}{2}+\sum_{i=1}^{m-2}i\cos(\frac{\pi}{6}-\frac{i\pi}{6(m-1)})\Big] \tag{5.10}$$

The phase output RMS voltage of the converter system can be derived based on Equa-

tion 5.8, i.e.

$$\begin{aligned} V_{ARMS} &= \sqrt{\tfrac{1}{\pi}\int_0^{\pi} V_A^2(\omega t)d(\omega t)} \\ &= \tfrac{\sqrt{4+\sqrt{3}}}{3\sqrt{3}}\tfrac{k_n U_{dc}}{m-1}\sqrt{(m-1)^2+\tfrac{11-6\sqrt{3}}{13}} = \tfrac{\sqrt{4+\sqrt{3}}}{3\sqrt{3}}k_n U_{dc}\sqrt{1+\tfrac{11-6\sqrt{3}}{13(m-1)^2}} \end{aligned} \quad (5.11)$$

The the output voltage total harmonic distortion (THD_V) is given by

$$\begin{aligned} THD_{V_A} &= \sqrt{\tfrac{2V_{Arms}^2}{V_{A1}^2}-1} \\ &= \sqrt{\frac{\pi^2(4+\sqrt{3})(m-1)^2[1+\frac{11-6\sqrt{3}}{13(m-1)^2}]}{27\times 128\sin^2(\frac{\pi}{12(m-1)})[\frac{(m-1)}{2}+\sum_{i=1}^{m-2} i\cos(\frac{\pi}{6}-\frac{i\pi}{6(m-1)})]^2}-1} \end{aligned} \quad (5.12)$$

5.4 ANALYSIS OF THE OUTPUT CURRENT WAVEFORMS

The high power converters are normally connected to the power system directly. In such cases if the source impedance is not significant the power system seen from the interface transformer primary terminals can be modelled as an ideal three phase voltage source V_s, i.e.

$$\mathbf{V_s}(\omega t) = \begin{bmatrix} v_{sA}(\omega t) \\ v_{sB}(\omega t) \\ v_{sC}(\omega t) \end{bmatrix} = \begin{bmatrix} V_{sm}\sin(\omega t+\phi) \\ V_{sm}\sin(\omega t-120^o+\phi) \\ V_{sm}\sin(\omega t+120^o+\phi) \end{bmatrix} \quad (5.13)$$

Under the assumptions that the capacitances of the capacitors on the converter dc side are infinite, the on-state voltage drop of all force commutated switches in the converter system is ignored, the off-state impedances of all force commutated switches in the

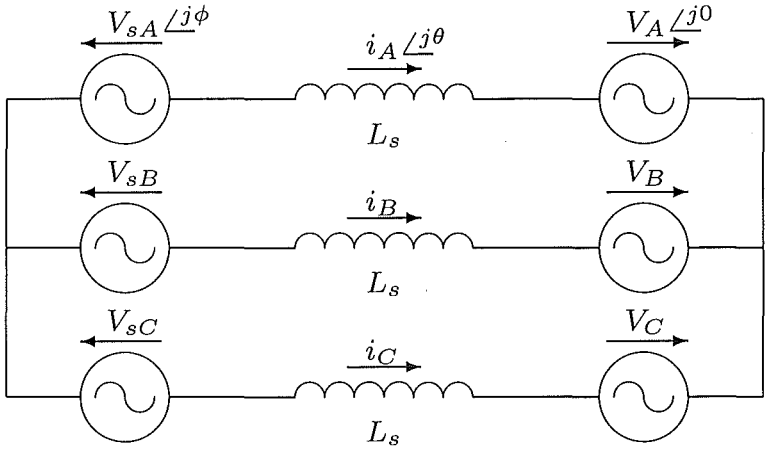


Figure 5.5 The Reinjection VSC System Model

converter system is infinite, and all the freewheel diodes are ideal, the converter seen

from the interface transformer secondary terminals can be modelled as a voltage source V_o, without internal impedance but with harmonics, i.e.

$$\mathbf{V_o}(\omega\mathbf{t}) = \begin{bmatrix} v_a(\omega t) \\ v_b(\omega t) \\ v_c(\omega t) \end{bmatrix} = \begin{bmatrix} \sum_{n=1}^{\infty} V_{An} \sin(n\omega t) \\ \sum_{n=1}^{\infty} V_{An} \sin(n\omega t - 120^o) \\ \sum_{n=1}^{\infty} V_{An} \sin(n\omega t + 120^o) \end{bmatrix}. \tag{5.14}$$

These two voltage sources are connected together via the interface transformer. If the interface transformer is perfectly balanced and the winding resistance and core loses are ignored, the two voltage sources are connected by L_s, the leakage inductance of the interface transformer.

The output current waveforms of the converter system can then be obtained by analysis of the simple model in Figure 5.5. The output current vector

$$\mathbf{I_o}(\omega\mathbf{t}) = [i_a(\omega t) \;\; i_b(\omega t) \;\; i_c(\omega t)]^T \tag{5.15}$$

is governed by the equation

$$L_s \frac{\mathbf{dI_o}(\omega\mathbf{t})}{\mathbf{dt}} = \mathbf{V_s}(\omega\mathbf{t}) - \mathbf{V_o}(\omega\mathbf{t}) \tag{5.16}$$

or

$$\mathbf{I_o}(\omega\mathbf{t}) = \frac{1}{X_s} \int_0^{\omega\mathbf{t}} [\mathbf{V_s}(\omega\mathbf{t}) - \mathbf{V_o}(\omega\mathbf{t})]\mathbf{d}(\omega\mathbf{t}) + \mathbf{I_o}(\mathbf{0}) \tag{5.17}$$

where $X_s = \omega L_s$ is the leakage reactance of the interface transformer. In the steady state $I_o(\omega t)|_{\omega t=0} = -I_o(\omega t)|_{\omega t=\pi}$, and therefore $I_o(0)$ can be determined from

$$\mathbf{I_o}(\mathbf{0}) = -\frac{V_{sm}}{X_s} \begin{bmatrix} \cos(\phi) \\ \cos(\phi - 120^o) \\ \cos(\phi + 120^o) \end{bmatrix} + \frac{1}{2X_s} \int_0^{\pi} \mathbf{V_o}(\omega\mathbf{t})\mathbf{d}(\omega\mathbf{t}) \tag{5.18}$$

Thus the output current vector can be expressed as

$$\mathbf{I_o}(\omega\mathbf{t}) = \mathbf{F_o}(\omega\mathbf{t}) - \mathbf{F_s}(\omega\mathbf{t}) \tag{5.19}$$

where,

$$\mathbf{F_o}(\omega\mathbf{t}) = \begin{bmatrix} f_a(\omega t) \\ f_b(\omega t) \\ f_c(\omega t) \end{bmatrix} \qquad \mathbf{F_s}(\omega\mathbf{t}) = \frac{V_{sm}}{X_s} \begin{bmatrix} \cos(\omega t + \phi) \\ \cos(\omega t + \phi - 120^o) \\ \cos(\omega t + \phi + 120^o) \end{bmatrix}$$

The right side of Equation 5.19 consists of two parts determined by the converter output voltage and the source voltage. The former part, $F_O(\omega t)$ can be expressed in

terms of harmonic components and the time functions for different time intervals. The harmonic component expression can be obtained by substituting expression 5.14 into equation 5.19, i.e.

$$\mathbf{I_o}(\omega t) = \begin{bmatrix} i_a(\omega t) \\ i_b(\omega t) \\ i_c(\omega t) \end{bmatrix} = \begin{bmatrix} \sum_{n=2}^{\infty} \frac{1}{nX_S} V_{An} \cos(n\omega t) \\ \sum_{n=2}^{\infty} \frac{1}{nX_S} V_{An} \cos(n\omega t - 120^o) \\ \sum_{n=2}^{\infty} \frac{1}{nX_S} V_{An} \cos(n\omega t + 120^o) \end{bmatrix} + \begin{bmatrix} \frac{1}{\omega L_s}[V_{A1}\cos(\omega t) - V_{sm}\cos(\omega t + \phi)] \\ \frac{1}{\omega L_s}[V_{A1}\cos(\omega t - 120^o) - V_{sm}\cos(\omega t - 120^o + \phi)] \\ \frac{1}{\omega L_s}[V_{A1}\cos(\omega t + 120^o) - V_{sm}\cos(\omega t + 120^o + \phi)] \end{bmatrix} \tag{5.20}$$

Equation 5.20 shows that the harmonic content of the output currents are caused solely by the harmonic components of the converter output voltages, and therefore for a specified voltage waveform, the harmonic current injections can be reduced only by increasing the leakage reactance of the interface transformer.

For simplicity, under balanced operating conditions, the current waveform can be analyzed using the amplitude and phase angle of the individual frequency component of a single phase(phase 'a' for example). The fundamental component amplitude of the phase output current, I_{A1} is given by

$$I_{A1} = \frac{1}{\omega L_s}\sqrt{V_{sm}^2 + V_{A1}^2 - 2V_{sm}V_{A1}\cos(\phi)} = \frac{V_{A1}}{\omega L_s}k \tag{5.21}$$

The n^{th} order harmonic amplitude of the output current is

$$I_{An} = \frac{V_{An}}{n\omega L_s} \tag{5.22}$$

Once the converter system output voltage waveform is fixed, i.e. V_{A1}, V_{Am} and ϕ have been determined, the output current spectrum becomes

$$I_{An}/I_{A1} = \frac{1}{n\sqrt{1 + \frac{V_{sm}^2}{V_{A1}^2} - 2\frac{V_{sm}}{V_{A1}}\cos(\phi)}}\frac{V_{An}}{V_{A1}} = \frac{1}{nk}\frac{V_{An}}{V_{A1}}, \tag{5.23}$$

which shows that the current spectrum can be simply obtained by dividing the output voltage spectrum by nk (where n is the harmonic order, and k the specific operation condition of the output voltage related to the source voltage, is given by $k = \sqrt{1 + \frac{V_{sm}^2}{V_{A1}^2} - 2\frac{V_{sm}}{V_{A1}}\cos(\phi)}$). From Equations 5.21 and 5.23 it is clear that the percentage harmonic will increase when the fundamental component of the output current is decreased.

Equation 5.20 is not in a suitable form to obtain the output current waveform and the output current RMS value. Instead, the output current waveform described by

Equation 5.19 can be obtained by the direct integration of the output voltage in the stair case shaped waveforms. The direct integration of the phase 'a' output voltage provides the multi-slope time domain function, the first element of $\mathbf{F_o}(\omega\mathbf{t})$ in Equation 5.19,

$$f_a(\omega t) = [\tfrac{1}{2X_s}\int_0^{\pi} V_A(\omega t)d(\omega t) - \int_0^{\omega t}\tfrac{V_A(\omega t)}{X_s}d(\omega t)]$$

The first part of $f_a(\omega t)$ is given by

$$\begin{aligned} f_o &= \frac{1}{2X_s}\int_0^{\pi} V_A(\omega t)d(\omega t) \\ &= \frac{\pi k_n U_{dc}}{12X_s(m-1)^2}\sum_{i=1}^{m-1}\{\frac{i}{3} + \frac{2i+\sqrt{3}(m-1-i)}{3} + \frac{(m-1-i)+\sqrt{3}i}{3} \\ &\quad + \frac{[2(m-1-i)+\sqrt{3}i]}{3} + \frac{[i+\sqrt{3}(m-1-i)]}{3} + \frac{(m-1-i)}{3}\} \\ &= \frac{\pi(4+2\sqrt{3})k_n U_{dc}}{36X_s} \end{aligned} \tag{5.24}$$

The second part of $f_a(\omega t)$ is derived based on Equation 5.8, it is given by

$$f_p(\omega t) = \frac{1}{k_n U_{dc}}\int_0^{\omega t} V_A(\omega t)d(\omega t)$$

$$= \begin{cases} \frac{c_i}{3} + \frac{i(\omega t - a_i)}{3(m-1)} & a_i < \omega t < b_i \\ \frac{\pi}{36} + \frac{a_i + (\sqrt{3}-1)c_i + [1+\frac{(\sqrt{3}-1)i}{m-1}](\omega t - a_i - \pi/6)}{3} & a_i + \frac{\pi}{6} < \omega t < b_i + \frac{\pi}{6} \\ \frac{(2+\sqrt{3})\pi}{36} + \frac{\sqrt{3}a_i + (2-\sqrt{3})c_i + [\sqrt{3}+\frac{(2-\sqrt{3})i}{m-1}](\omega t - a_i - \pi/3)}{3} & a_i + \frac{\pi}{3} < \omega t < b_i + \frac{\pi}{3} \\ \frac{(4+2\sqrt{3})\pi}{36} + \frac{2a_i - (2-\sqrt{3})c_i + [2-\frac{(2-\sqrt{3})i}{m-1}](\omega t - a_i - \pi/2)}{3} & a_i + \frac{\pi}{2} < \omega t < b_i + \frac{\pi}{2} \\ \frac{(6+3\sqrt{3})\pi}{36} + \frac{\sqrt{3}a_i - (\sqrt{3}-1)c_i + [\sqrt{3}-\frac{(\sqrt{3}-1)i}{m-1}](\omega t - a_i - 2\pi/3)}{3} & a_i + \frac{2\pi}{3} < \omega t < b_i + \frac{2\pi}{3} \\ \frac{(7+4\sqrt{3})\pi}{36} + \frac{a_i - c_i + [1-\frac{i}{m-1}](\omega t - a_i - 5\pi/6)}{3} & a_i + \frac{5\pi}{6} < \omega t < b_i + \frac{5\pi}{6} \\ \frac{(8+4\sqrt{3})\pi}{36} - \frac{c_i + [\frac{i}{m-1}](\omega t - a_i - \pi)}{3} & a_i + \pi < \omega t < b_i + \pi \\ \frac{(7+4\sqrt{3})\pi}{36} - \frac{a_i + (\sqrt{3}-1)c_i + [1+\frac{(\sqrt{3}-1)i}{m-1}](\omega t - a_i - 7\pi/6)}{3} & a_i + \frac{7\pi}{6} < \omega t < b_i + \frac{7\pi}{6} \\ \frac{(6+3\sqrt{3})\pi}{36} - \frac{\sqrt{3}a_i + (2-\sqrt{3})c_i + [\sqrt{3}+\frac{(2-\sqrt{3})i}{m-1}](\omega t - a_i - 4\pi/3)}{3} & a_i + \frac{4\pi}{3} < \omega t < b_i + \frac{4\pi}{3} \\ \frac{(4+2\sqrt{3})\pi}{36} - \frac{2a_i - (2-\sqrt{3})c_i + [2-\frac{(2-\sqrt{3})i}{m-1}](\omega t - a_i - 3\pi/2)}{3} & a_i + \frac{3\pi}{2} < \omega t < b_i + \frac{3\pi}{2} \\ \frac{(2+\sqrt{3})\pi}{36} - \frac{\sqrt{3}a_i - (\sqrt{3}-1)c_i + [\sqrt{3}-\frac{(\sqrt{3}-1)i}{m-1}](\omega t - a_i - 5\pi/3)}{3} & a_i + \frac{5\pi}{3} < \omega t < b_i + \frac{5\pi}{3} \\ \frac{\pi}{36} - \frac{a_i - c_i + [1-\frac{i}{m-1}](\omega t - a_i - 11\pi/6)}{3} & a_i + \frac{11\pi}{6} < \omega t < b_i + \frac{11\pi}{6} \end{cases} \tag{5.25}$$

where $a_i = \frac{(2i-1)\pi}{12(m-1)}$ $b_i = \frac{(2i+1)\pi}{12(m-1)}$ $c_i = \frac{(i-1)i\pi}{12(m-1)^2}$. The symbols a_i, b_i, c_i, i in Equation 5.25

are for $i=1,2,\cdots,m-1$.

Based on this time domain multi-slope function the output RMS current can be derived as follows:

$$\begin{aligned} f_a(\omega t) &= [\tfrac{1}{2X_s}\int_0^{\pi} V_A(\omega t)d(\omega t) - \int_0^{\omega t}\tfrac{V_A(\omega t)}{X_s}d(\omega t)] \\ &= f_o - \tfrac{k_n U_{dc}}{X_s} f_p(\omega t) \\ &= \tfrac{k_n U_{dc}}{X_s}[\tfrac{\pi(4+2\sqrt{3})}{36} - f_p(\omega t)] = \tfrac{k_n U_{dc}}{X_s} f_s(\omega t) \end{aligned}$$

$$f_s(\omega t)=\begin{cases} \frac{(4+2\sqrt{3})\pi}{36} - \frac{c_i}{3} - \frac{i(\omega t-a_i)}{3(m-1)} & a_i<\omega t<b_i \\ \frac{(3+2\sqrt{3})\pi}{36} - \frac{a_i+(\sqrt{3}-1)c_i+[1+\frac{(\sqrt{3}-1)i}{m-1}](\omega t-a_i-\pi/6)}{3} & a_i+\frac{\pi}{6}<\omega t<b_i+\frac{\pi}{6} \\ \frac{(2+\sqrt{3})\pi}{36} - \frac{\sqrt{3}a_i+(2-\sqrt{3})c_i+[\sqrt{3}+\frac{(2-\sqrt{3})i}{m-1}](\omega t-a_i-\pi/3)}{3} & a_i+\frac{\pi}{3}<\omega t<b_i+\frac{\pi}{3} \\ -\frac{2a_i-(2-\sqrt{3})c_i+[2-\frac{(2-\sqrt{3})i}{m-1}](\omega t-a_i-\pi/2)}{3} & a_i+\frac{\pi}{2}<\omega t<b_i+\frac{\pi}{2} \\ -\frac{(2+\sqrt{3})\pi}{36} - \frac{\sqrt{3}a_i-(\sqrt{3}-1)c_i+[\sqrt{3}-\frac{(\sqrt{3}-1)i}{m-1}](\omega t-a_i-2\pi/3)}{3} & a_i+\frac{2\pi}{3}<\omega t<b_i+\frac{2\pi}{3} \\ -\frac{(3+2\sqrt{3})\pi}{36} - \frac{a_i-c_i+[1-\frac{i}{m-1}](\omega t-a_i-5\pi/6)}{3} & a_i+\frac{5\pi}{6}<\omega t<b_i+\frac{5\pi}{6} \\ -\frac{(4+2\sqrt{3})\pi}{36} + \frac{c_i+[\frac{i}{m-1}](\omega t-a_i-\pi)}{3} & a_i+\pi<\omega t<b_i+\pi \\ -\frac{(3+2\sqrt{3})\pi}{36} + \frac{a_i+(\sqrt{3}-1)c_i+[1+\frac{(\sqrt{3}-1)i}{m-1}](\omega t-a_i-7\pi/6)}{3} & a_i+\frac{7\pi}{6}<\omega t<b_i+\frac{7\pi}{6} \\ -\frac{(2+\sqrt{3})\pi}{36} + \frac{\sqrt{3}a_i+(2-\sqrt{3})c_i+[\sqrt{3}+\frac{(2-\sqrt{3})i}{m-1}](\omega t-a_i-4\pi/3)}{3} & a_i+\frac{4\pi}{3}<\omega t<b_i+\frac{4\pi}{3} \\ \frac{2a_i-(2-\sqrt{3})c_i+[2-\frac{(2-\sqrt{3})i}{m-1}](\omega t-a_i-3\pi/2)}{3} & a_i+\frac{3\pi}{2}<\omega t<b_i+\frac{3\pi}{2} \\ \frac{(2+\sqrt{3})\pi}{36} + \frac{\sqrt{3}a_i-(\sqrt{3}-1)c_i+[\sqrt{3}-\frac{(\sqrt{3}-1)i}{m-1}](\omega t-a_i-5\pi/3)}{3} & a_i+\frac{5\pi}{3}<\omega t<b_i+\frac{5\pi}{3} \\ \frac{(3+2\sqrt{3})\pi}{36} + \frac{a_i-c_i+[1-\frac{i}{m-1}](\omega t-a_i-11\pi/6)}{3} & a_i+\frac{11\pi}{6}<\omega t<b_i+\frac{11\pi}{6} \end{cases} \tag{5.26}$$

where $a_i=\frac{(2i-1)\pi}{12(m-1)}$ $b_i=\frac{(2i+1)\pi}{12(m-1)}$ $c_i=\frac{(i-1)i\pi}{12(m-1)^2}$, and symbols a_i, b_i, c_i, i in Equation 5.26 are also for $i=1,2,\cdots,m-1$.

Thus the output current RMS value, I_{ARMS} can be derived from

$$I_{ARMS} = \sqrt{I_{A1RMS}^2 + \frac{1}{2\pi}\int_0^{2\pi} f_a^2(\omega t)d\omega t - \frac{V_{A1}^2}{2X_s^2}} \tag{5.27}$$

where

$$I_{A1RMS} = \frac{V_{A1}}{\sqrt{2}X_s}\sqrt{1+\frac{V_{sm}^2}{V_{A1}^2} - 2\frac{V_{sm}}{V_{A1}}\cos\phi} = \frac{V_{A1}}{\sqrt{2}X_s}k \tag{5.28}$$

and

$$\frac{1}{2\pi}\int_0^{2\pi} f_a^2(\omega t)d\omega t = \frac{1}{\pi}[\frac{k_n U_{dc}}{X_s}]^2 \int_0^{\pi} f_s^2(\omega t)d\omega t$$

The integration $\int_0^{\pi} f_s^2(\omega t)d\omega t$ is calculated based on Equation 5.26,

$$\begin{aligned}
\int_0^{\pi} f_s^2(\omega t)d\omega t = &\sum_{i=1}^{m-1}\int_{a_i}^{b_i} \left[\tfrac{(4+2\sqrt{3})\pi}{36} - \tfrac{c_i}{3} - \tfrac{ix}{3(m-1)}\right]^2 dx \\
&+\sum_{i=1}^{m-1}\int_{\frac{\pi}{6}+a_i}^{\frac{\pi}{6}+b_i} \left[\tfrac{(3+2\sqrt{3})\pi}{36} - \tfrac{a_i+(\sqrt{3}-1)c_i+[1+\frac{(\sqrt{3}-1)i}{m-1}](\omega t-a_i-\pi/6)}{3}\right]^2 d\omega t \\
&+\sum_{i=1}^{m-1}\int_{\frac{\pi}{3}+a_i}^{\frac{\pi}{3}+b_i} \left[\tfrac{(2+\sqrt{3})\pi}{36} - \tfrac{\sqrt{3}a_i+(2-\sqrt{3})c_i+[\sqrt{3}+\frac{(2-\sqrt{3})i}{m-1}](\omega t-a_i-\pi/3)}{3}\right]^2 d\omega t \\
&+\sum_{i=1}^{m-1}\int_{\frac{\pi}{2}+a_i}^{\frac{\pi}{2}+b_i} \left[\tfrac{2a_i-(2-\sqrt{3})c_i+[2-\frac{(2-\sqrt{3})i}{m-1}](\omega t-a_i-\pi/2)}{3}\right]^2 d\omega t \\
&+\sum_{i=1}^{m-1}\int_{\frac{2\pi}{3}+a_i}^{\frac{2\pi}{3}+b_i} \left[\tfrac{(2+3\sqrt{3})\pi}{36} + \tfrac{\sqrt{3}a_i-(\sqrt{3}-1)c_i+[\sqrt{3}-\frac{(\sqrt{3}-1)i}{m-1}](\omega t-a_i-2\pi/3)}{3}\right]^2 d\omega t \\
&+\sum_{i=1}^{m-1}\int_{\frac{5\pi}{6}+a_i}^{\frac{5\pi}{6}+b_i} \left[\tfrac{(3+2\sqrt{3})\pi}{36} + \tfrac{a_i-c_i+[1-\frac{i}{m-1}](\omega t-a_i-5\pi/6)}{3}\right]^2 d\omega t \\
= &\sum_{i=1}^{m-1}\int_0^{B} \left[\tfrac{(4+2\sqrt{3})\pi}{36} - \tfrac{c_i}{3} - \tfrac{ix}{3(m-1)}\right]^2 dx \\
&+\sum_{i=1}^{m-1}\int_0^{B} \left[\tfrac{(3+2\sqrt{3})\pi}{36} - \tfrac{a_i+(\sqrt{3}-1)c_i+[1+\frac{(\sqrt{3}-1)i}{m-1}]x}{3}\right]^2 dx \\
&+\sum_{i=1}^{m-1}\int_0^{B} \left[\tfrac{(2+\sqrt{3})\pi}{36} - \tfrac{\sqrt{3}a_i+(2-\sqrt{3})c_i+[\sqrt{3}+\frac{(2-\sqrt{3})i}{m-1}]x}{3}\right]^2 dx \\
&+\sum_{i=1}^{m-1}\int_0^{B} \left[\tfrac{2a_i-(2-\sqrt{3})c_i+[2-\frac{(2-\sqrt{3})i}{m-1}]x}{3}\right]^2 dx \\
&+\sum_{i=1}^{m-1}\int_0^{B} \left[\tfrac{(2+3\sqrt{3})\pi}{36} + \tfrac{\sqrt{3}a_i-(\sqrt{3}-1)c_i+[\sqrt{3}-\frac{(\sqrt{3}-1)i}{m-1}]x}{3}\right]^2 dx \\
&+\sum_{i=1}^{m-1}\int_0^{B} \left[\tfrac{(3+2\sqrt{3})\pi}{36} + \tfrac{a_i-c_i+[1-\frac{i}{m-1}]x}{3}\right]^2 dx \\
= &\tfrac{\pi^3}{10\times 18^3}\left[(636+357\sqrt{3}) + \tfrac{5(4+\sqrt{3})}{(m-1)^2} + \tfrac{2(2-\sqrt{3})}{(m-1)^4}\right]
\end{aligned}$$

where $B = b_i - a_i = \frac{\pi}{6(m-1)}$, and m is the number of the reinjection voltage levels. Thus the integration $\frac{1}{2\pi}\int_0^{2\pi} f_a^2(\omega t)d\omega t$ can be given in the form of

$$\frac{1}{2\pi}\int_0^{2\pi} f_a^2(\omega t)d\omega t = P(m)\frac{V_{A1}^2}{2X_s^2} \tag{5.29}$$

where

$$V_{A1}=\frac{16k_nU_{dc}}{\pi(m-1)}\sin(\frac{\pi}{12(m-1)})[\frac{(m-1)}{2}+\sum_{i=1}^{m-2}i\cos(\frac{\pi}{6}-\frac{i\pi}{6(m-1)})]$$

$$P(m)=\frac{\pi^4(m-1)^2[(636+357\sqrt{3})+\frac{5(4+\sqrt{3})}{(m-1)^2}+\frac{2(2-\sqrt{3})}{(m-1)^4}]}{5\times16^2\times18^3\sin^2(\frac{\pi}{12(m-1)})[\frac{(m-1)}{2}+\sum_{i=1}^{m-2}i\cos(\frac{\pi}{6}-\frac{i\pi}{6(m-1)})]^2} \tag{5.30}$$

Equation 5.30 shows that $P(m)$ is only related to the reinjection voltage level number m and therefore when m is fixed, $P(m)$ is a constant. Its minimum value $1+7.797347826\times 10^{-7}$ is reached when m tends to infinity, this means that a pure sinusoidal waveform can not be produced by equally dividing the dc voltage into very large number of levels; its practical maximum value is $1+5.096940954\times10^{-6}$ for $m=3$.

Thus the output current RMS value, I_{ARMS} can be simplified as

$$I_{ARMS}=\frac{V_{A1}}{\sqrt{2}X_s}\sqrt{k^2+P(m)-1} \tag{5.31}$$

and the Total Harmonic Distortion of the output current (THD_I)

$$THD_{I_A}=\sqrt{\frac{I_{ARMS}^2}{I_{A1RMS}^2}-1}=\sqrt{\frac{k^2+P(m)-1}{k^2}-1}=\frac{\sqrt{P(m)-1}}{k} \tag{5.32}$$

It is clear that the Total Harmonic Distortion of the output current is dependent on the operation conditions index k and $P(m)$, which is determined by the reinjection level number m; i.e. for a fixed reinjection level number, THD_I is only determined by the operating index k, which is related to the amplitude percentage V_{sm}/V_{A1} and phase angle difference ϕ between the output voltage fundamental and the source voltage. For a specified operation condition (i.e. k is fixed), the minimum THD_I is achieved when $P(m)$ reaches its minimum value(i.e. the level number m tends to infinity). Because the minimum value of $P(m)$ is greater than one, the output current THD_I can not be reduced to zero by increasing reinjection voltage levels.

Another expression for the operation condition index k can be obtained from Equation 5.28, i.e.

$$k=I_{A1RMS}\cdot\frac{\sqrt{2}X_s}{V_{A1}}=\frac{1}{V_{A1}/V_{sm}}\cdot\frac{I_{A1RMS}}{I_{Arated}}\cdot\frac{X_s}{(V_{sm}/\sqrt{2})/I_{Arated}} \tag{5.33}$$

In equation 5.33 the rated output current I_{Arated} and the source voltage V_{sm} are set as the current and voltage base, thus the output current total harmonic distortion THD_I is related to the nominal voltage V_{A1}/V_{sm}, the nominal current I_{A1RMS}/I_{Arated} and the nominal reactance $\frac{X_s}{(V_{sm}/\sqrt{2})/I_{Arated}}$. Under the rated operation conditions, i.e. the converter system output rated voltages and currents, the output current total harmonic

distortion THD_I is solely determined by the nominal reactance $\frac{X_s}{(V_{sm}/\sqrt{2})/I_{Arated}}$.

Based on Equation 5.19 and Equation 5.25, the output current waveforms at some specific operation conditions for $m = 8$ are plotted in Figure 5.6, the corresponding spectra of the output current waveforms are shown in Figure 5.7.

5.5 ANALYSIS OF THE SYSTEM CURRENT WAVEFORMS

5.5.1 Main Bridge Current Waveforms

Because the primary (power system side) windings of the two converter interface transformers are connected in series, the primary winding currents are the converter system output currents. Under the assumption of perfect mutual coupling, the secondary (i.e. the converter side) winding currents are related to the primary side currents by the turn ratios of the main interface transformers, i.e. $k_n : 1$(for Y/Y) and $k_n : \sqrt{3}$(for Y/Δ). The Following expressions can be written for the converter side phase currents of the Y/Y and Y/Δ connection interface transformers:

$$\begin{aligned} \mathbf{I_{YY}}(\omega\mathbf{t}) &= [i_{Ya}(\omega t) \quad i_{Yb}(\omega t) \quad i_{Yc}(\omega t)]^T \\ = k_n\mathbf{I_o}(\omega\mathbf{t}) &= k_n[i_a(\omega t) \quad i_b(\omega t) \quad i_c(\omega t)]^T \end{aligned} \tag{5.34}$$

$$\begin{aligned} \mathbf{I_{Y\Delta p}}(\omega\mathbf{t}) &= [i_{\Delta ap}(\omega t) \quad i_{\Delta bp}(\omega t) \quad i_{\Delta cp}(\omega t)]^T \\ = \frac{k_n}{\sqrt{3}}\mathbf{I_o}(\omega\mathbf{t}) &= \frac{k_n}{\sqrt{3}}[i_A(\omega t) \quad i_B(\omega t) \quad i_C(\omega t)]^T \end{aligned} \tag{5.35}$$

and the line current vector is the same as the phase current vector for the Y/Y connection transformer, but the line current vector for the Y/Δ connection transformer becomes

$$\begin{aligned} \mathbf{I_{Y\Delta}}(\omega\mathbf{t}) &= [i_{\Delta a}(\omega t) \quad i_{\Delta b}(\omega t) \quad i_{\Delta c}(\omega t)]^T \\ = k_n\mathbf{I_o}(\omega\mathbf{t} + \mathbf{30^o}) &= k_n[i_A(\omega t + 30^o) \quad i_B(\omega t + 30^o) \quad i_C(\omega t + 30^o)]^T \end{aligned} \tag{5.36}$$

The dc side currents of these two six-pulse converters are determined by the interface transformer secondary currents and the switching state combinations of the valves in the two main converters. For steady operation with the time reference specified by Equation 5.14, the dc side currents can be described by the interface transformer currents and the

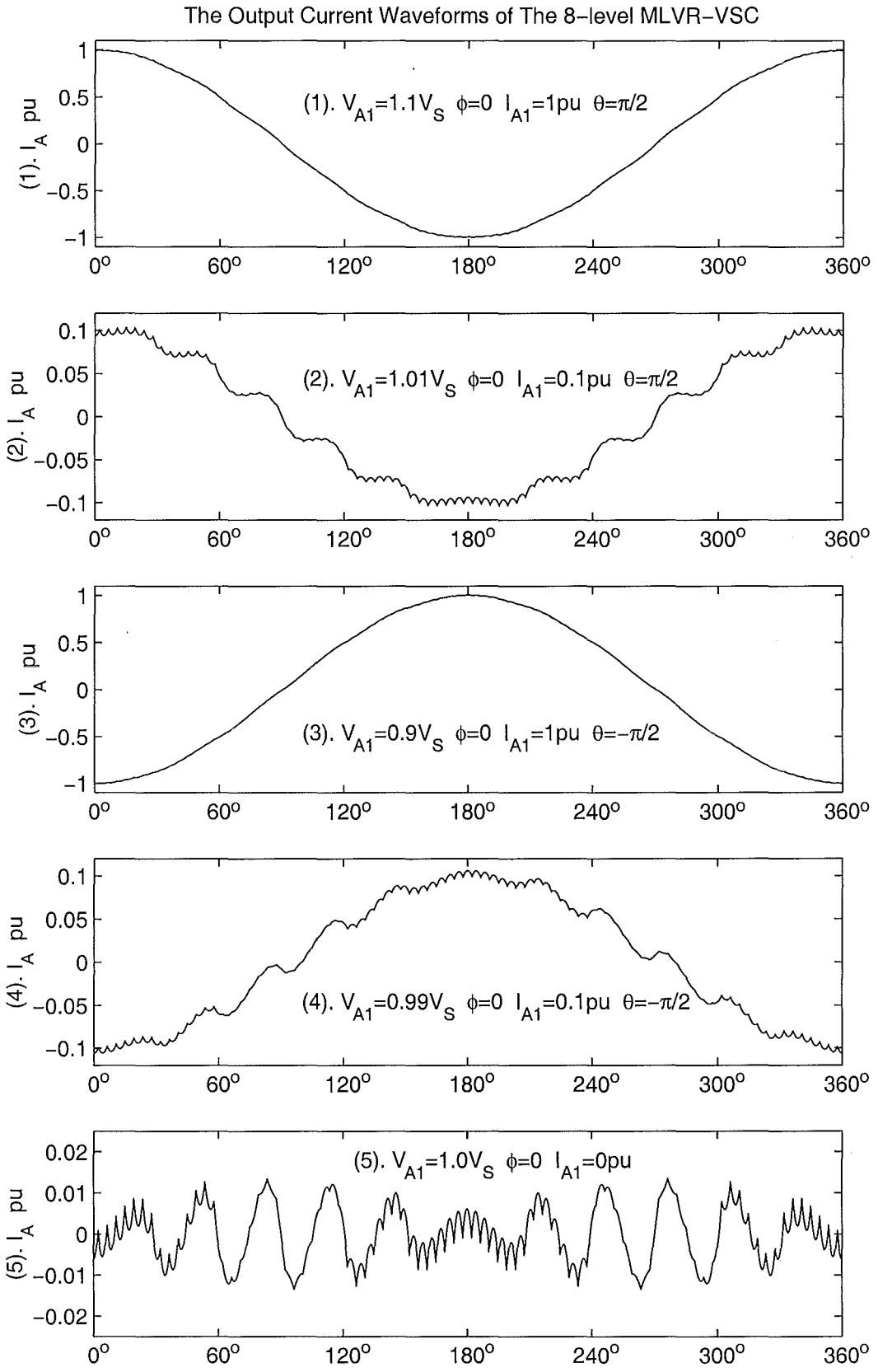


Figure 5.6 The Output Current Waveforms of the 8-level MLVR-VSC

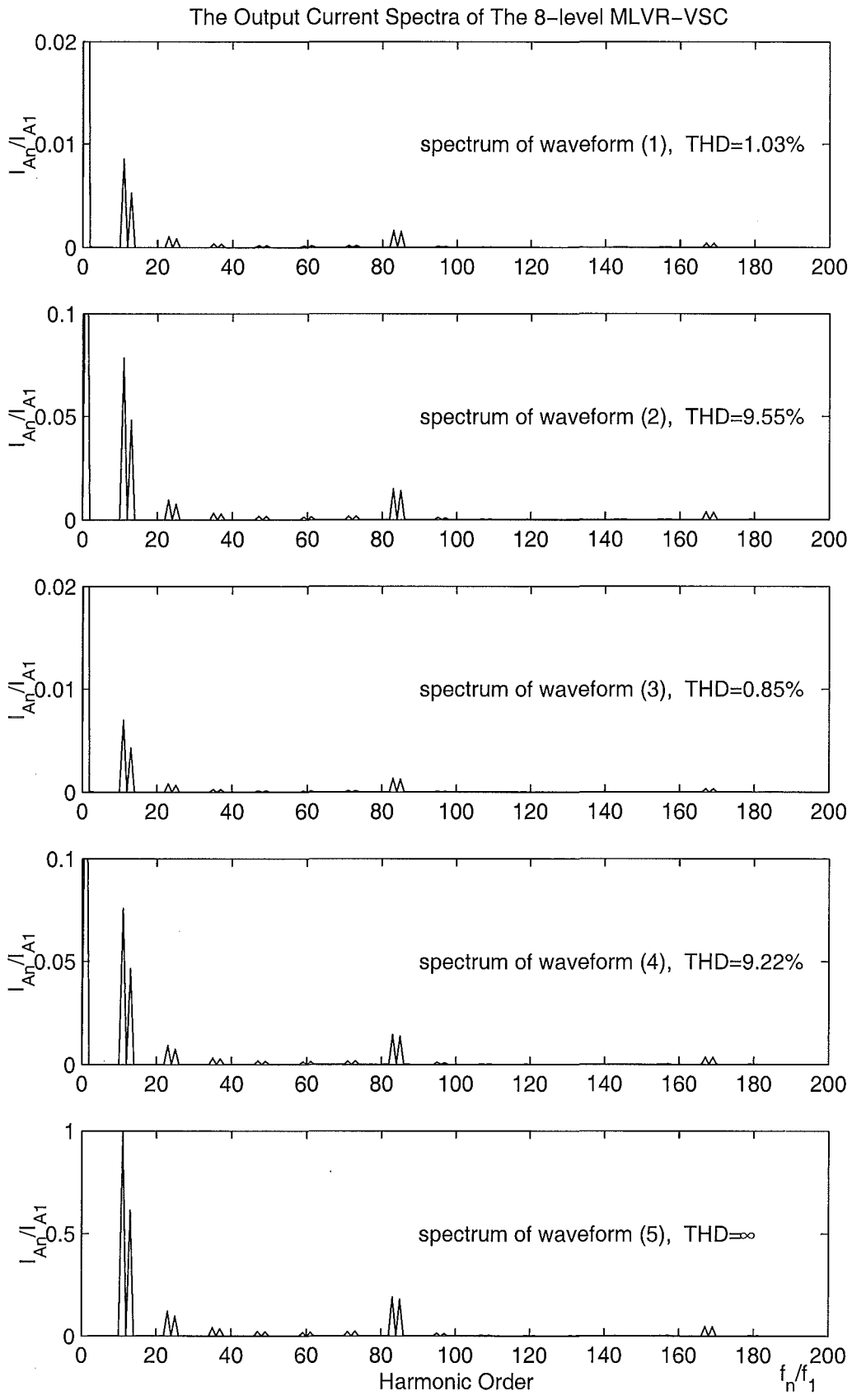


Figure 5.7 The Output Current Spectra of the 8-level MLVR-VSC

switching functions, $\mathbf{f_{s\Delta}}$ and $\mathbf{f_{sY}}$ for Y/Y and Y/Δ connection converters respectively.

$$\mathbf{f_{sY}}(\omega t) = \begin{cases} [\ 0 \quad -1 \quad 0\ ] & 0 < \omega t < \pi/3 \\ [\ 1 \quad 0 \quad 0\ ] & \pi/3 < \omega t < 2\pi/3 \\ [\ 0 \quad 0 \quad -1\ ] & 2\pi/3 < \omega t < \pi \\ [\ 0 \quad 1 \quad 0\ ] & \pi < \omega t < 4\pi/3 \\ [-1 \quad 0 \quad 0\ ] & 4\pi/3 < \omega t < 5\pi/3 \\ [\ 0 \quad 0 \quad 1\ ] & 5\pi/3 < \omega t < 2\pi \end{cases} \tag{5.37}$$

$$\mathbf{f_{s\Delta}}(\omega t) = \begin{cases} [\ 0 \quad -1 \quad 0\ ] & 0 < \omega t < \pi/6 \\ [\ 1 \quad 0 \quad 0\ ] & \pi/6 < \omega t < 3\pi/6 \\ [\ 0 \quad 0 \quad -1\ ] & 3\pi/6 < \omega t < 5\pi/6 \\ [\ 0 \quad 1 \quad 0\ ] & 5\pi/6 < \omega t < 7\pi/6 \\ [-1 \quad 0 \quad 0\ ] & 7\pi/6 < \omega t < 9\pi/6 \\ [\ 0 \quad 0 \quad 1\ ] & 9\pi/6 < \omega t < 11\pi/6 \\ [\ 0 \quad -1 \quad 0\ ] & 11\pi/6 < \omega t < 2\pi \end{cases} \tag{5.38}$$

The dc output currents of the two main converters, i_{Ydc} and $i_{\Delta dc}$ are given by the following two expressions.

$$i_{Ydc}(\omega t) = f_{sY}(\omega t) \cdot I_{YY}(\omega t) \tag{5.39}$$

$$i_{\Delta dc}(\omega t) = f_{s\Delta}(\omega t) \cdot I_{Y\Delta}(\omega t) \tag{5.40}$$

The waveforms of currents i_A, i_B, i_C, i_{Ydc}, $i_{\Delta dc}$ for capacitive operation are shown in Figure 5.9 and Figure 5.10.

5.5.2 Reinjection Circuit Current Waveforms

The reinjection circuit can be formed in different ways, as described in the early chapter 4. For better understanding of the reinjection circuit operation without having to analyze the circuits individually, a simplified circuit is shown in Figure 5.8.

The individual paths from each of the m level nodes (v_0, v_1, $\cdots$, $v_{(m-2)}$, $v_{(m-1)}$) to the output terminal (u_j) of the reinjection converter are represented by ideal switches. Thus the switch component current analysis is replaced by the path current analysis regardless of the topological structure and switch type.

With reference to Figure 5.8, the output current of the reinjection converter, i_j is the algebraic addition of currents i_{Ydc} and $i_{\Delta dc}$, i.e.

$$\begin{aligned} &i_{cu}(\omega t) = i_{\Delta dc}(\omega t) - I_{dc} \qquad i_{cd}(\omega t) = i_{Ydc}(\omega t) - I_{dc} \\ &i_j(\omega t) = i_{cu} - i_{cd} = i_{\Delta dc}(\omega t) - i_{Ydc}(\omega t) \end{aligned} \tag{5.41}$$

Because only one path is in on-state at any instant, and the path states are changed periodically, i_j the output current of the reinjection VSC is periodically taken by the

m paths and distributed in discrete time intervals at six times the main bridge firing frequency. Based on the firing synchronization of the reinjection VSC with the two main bridges, if the converter output voltage is expressed by Equation 5.14, the distributions of the current i_j in the m ideal switch paths for the specific time intervals are as follows:

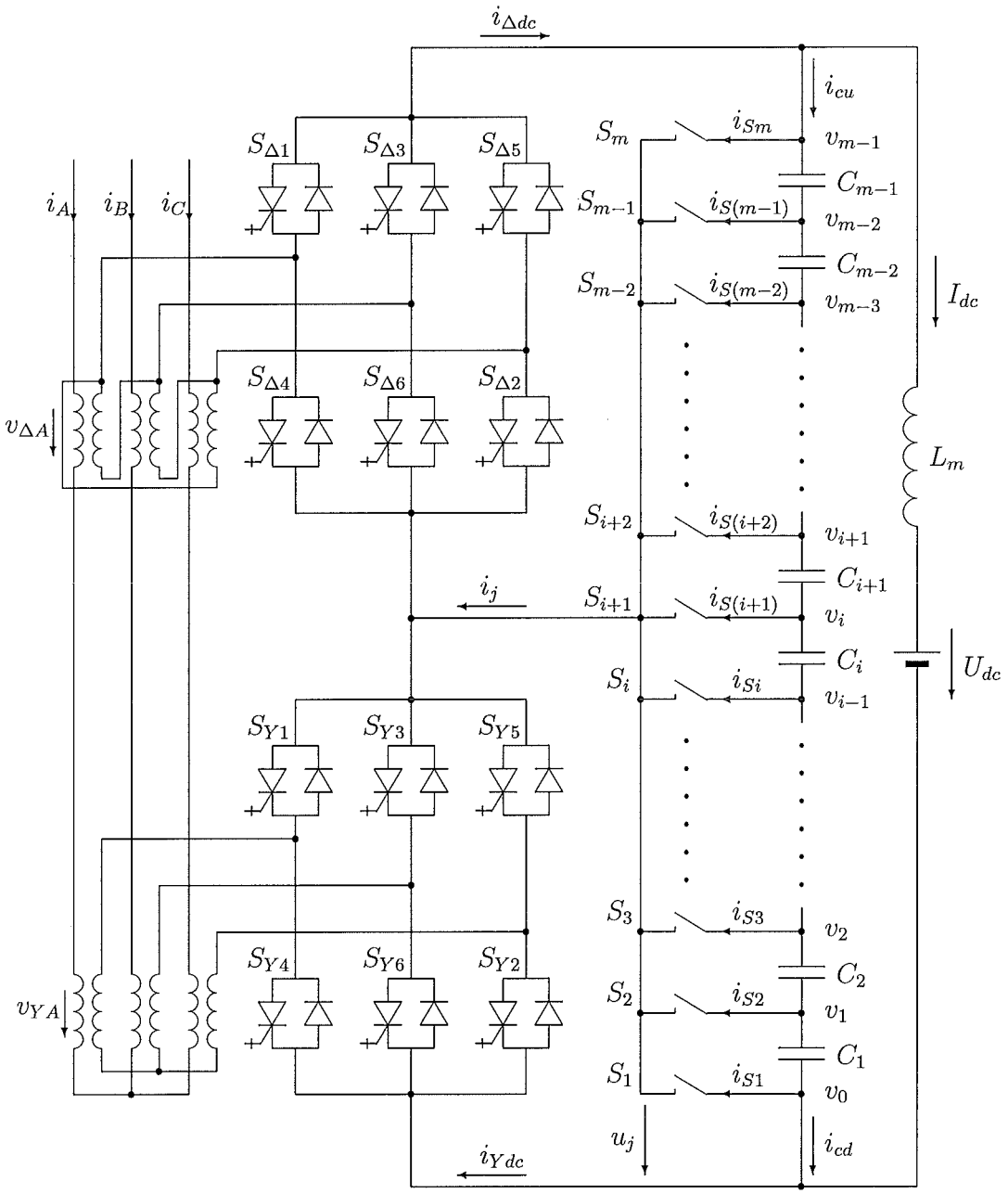


Figure 5.8 The MLVR-VSC Equivalent for System Current Analysis

$for \quad -\alpha < \omega t < \frac{\pi}{6} + \alpha \quad (\alpha = \frac{\pi}{12(m-1)})$

$$
\begin{array}{rcll}
i_{S1}(\omega t) = & i_j(\omega t) & & -\alpha < \omega t < \alpha \\
i_{S2}(\omega t) = & i_j(\omega t) & & \alpha < \omega t < 3\alpha \\
i_{S3}(\omega t) = & i_j(\omega t) & & 3\alpha < \omega t < 5\alpha \\
\vdots \quad & \vdots \quad & \vdots & \vdots \quad \vdots \quad \vdots \\
i_{Si}(\omega t) = & i_j(\omega t) & & (2i-3)\alpha < \omega t < (2i-1)\alpha \\
i_{S(i+1)}(\omega t) = & i_j(\omega t) & & (2i-1)\alpha < \omega t < (2i+1)\alpha \\
i_{S(i+2)}(\omega t) = & i_j(\omega t) & & (2i+1)\alpha < \omega t < (2i+3)\alpha \\
\vdots \quad & \vdots \quad & \vdots & \vdots \quad \vdots \quad \vdots \\
i_{S(m-2)}(\omega t) = & i_j(\omega t) & & \frac{\pi}{6} - 5\alpha < \omega t < \frac{\pi}{6} - 3\alpha \\
i_{S(m-1)}(\omega t) = & i_j(\omega t) & & \frac{\pi}{6} - 3\alpha < \omega t < \frac{\pi}{6} - \alpha \\
i_{Sm}(\omega t) = & i_j(\omega t) & & \frac{\pi}{6} - \alpha < \omega t < \frac{\pi}{6} + \alpha
\end{array}
$$

$for \quad \frac{\pi}{6} - \alpha < \omega t < \frac{\pi}{3} + \alpha$

$$
\begin{array}{rcll}
i_{Sm}(\omega t) = & i_j(\omega t) & & \frac{\pi}{6} - \alpha < \omega t < \frac{\pi}{6} + \alpha \\
i_{S(m-1)}(\omega t) = & i_j(\omega t) & & \frac{\pi}{6} + \alpha < \omega t < \frac{\pi}{6} + 3\alpha \\
i_{S(m-2)}(\omega t) = & i_j(\omega t) & & \frac{\pi}{6} + 3\alpha < \omega t < \frac{\pi}{6} + 5\alpha \\
\vdots \quad & \vdots \quad & \vdots & \vdots \quad \vdots \quad \vdots \\
i_{S(i+2)}(\omega t) = & i_j(\omega t) & & \frac{\pi}{3} - (2i+1)\alpha < \omega t < \frac{\pi}{3} - (2i+3)\alpha \\
i_{S(i+1)}(\omega t) = & i_j(\omega t) & & \frac{\pi}{3} - (2i-1)\alpha < \omega t < \frac{\pi}{3} - (2i+1)\alpha \\
i_{Si}(\omega t) = & i_j(\omega t) & & \frac{\pi}{3} - (2i-3)\alpha < \omega t < \frac{\pi}{3} - (2i-1)\alpha \\
\vdots \quad & \vdots \quad & \vdots & \vdots \quad \vdots \quad \vdots \\
i_{S3}(\omega t) = & i_j(\omega t) & & \frac{\pi}{3} - 7\alpha < \omega t < \frac{\pi}{3} - 5\alpha \\
i_{S2}(\omega t) = & i_j(\omega t) & & \frac{\pi}{3} - 5\alpha < \omega t < \frac{\pi}{3} - 3\alpha \\
i_{S1}(\omega t) = & i_j(\omega t) & & \frac{\pi}{3} - \alpha < \omega t < \frac{\pi}{3} + \alpha
\end{array}
$$

For the steady state operation the full-cycle compact expression of the relations between i_j (the output current of the reinjection circuitry) and the currents of the m ideal switches, is:

$$\mathbf{I_{SJ}} = [i_{S1} \quad i_{S2} \quad \cdots \quad i_{S(m-1)} \quad i_{Sm}]^T = \mathbf{F_{SJ}} \mathbf{I_{JP}} \tag{5.42}$$

where $\mathbf{I_{JP}}$, represents the full-cycle $i_j(\omega t)$ in vector form, and the elements of $\mathbf{I_{JP}}$ are

obtained by dividing the full-cycle $i_j(\omega t)$ into $2(m-1)$ time domain functions i.e.

$$\mathbf{I_{JP}} = [i_{j1}(\omega t) \;\; i_{j2}(\omega t) \;\; \cdots \;\; i_{j(2m-3)}(\omega t) \;\; i_{j(2m-2)}(\omega t)]^T \tag{5.43}$$

where

$$i_{j1}(\omega t) = \begin{cases} i_j(\omega t) & for \quad -\alpha < \omega t < \alpha \\ 0 & for \quad -\alpha > \omega t \;\; and \;\; \omega t > 3\alpha \end{cases}$$

$$i_{j2}(\omega t) = \begin{cases} i_j(\omega t) & for \quad \alpha < \omega t < 3\alpha \\ 0 & for \quad \alpha > \omega t \;\; and \;\; \omega t > 3\alpha \end{cases}$$

$$\vdots \qquad \vdots \qquad \vdots \qquad \vdots$$

$$i_{j(2m-3)}(\omega t) = \begin{cases} i_j(\omega t) & for \quad \frac{\pi}{3} - 5\alpha < \omega t < \frac{\pi}{3} - 3\alpha \\ 0 & for \quad \frac{\pi}{3} - 5\alpha > \omega t \;\; and \;\; \omega t > \frac{\pi}{3} - 3\alpha \end{cases}$$

$$i_{j(2m-2)}(\omega t) = \begin{cases} i_j(\omega t) & for \quad \frac{\pi}{3} - 3\alpha < \omega t < \frac{\pi}{3} - \alpha \\ 0 & for \quad \frac{\pi}{3} - 3\alpha > \omega t \;\; and \;\; \omega t > \frac{\pi}{3} - \alpha \end{cases}$$

$\mathbf{F_{SJ}}$ is the $m \times (2m-2)$ matrix which expresses the on and off states of the m ideal switches over the full-cycle period of the reinjection VSC; the m rows correspond to the m ideal switches and the $2(m-1)$ columns correspond to the $2(m-1)$ time intervals over the $\pi/3$ period. The $\mathbf{F_{SJ}}$ is given by

$$\mathbf{F_{SJ}} = \begin{array}{c} \left[\begin{array}{ccccccccc} 1 & 0 & \cdots & 0 & 0 & 0 & \cdots & 0 & 0 \\ 0 & 1 & \cdots & 0 & 0 & 0 & \cdots & 0 & 1 \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\ 0 & 0 & \cdots & 1 & 0 & 1 & \cdots & 0 & 0 \\ 0 & 0 & \cdots & 0 & 1 & 0 & \cdots & 0 & 0 \end{array}\right] \begin{array}{c} 1 \\ 2 \\ \vdots \\ (m-1) \\ m \end{array} \\ \begin{array}{ccccccccc} 1 & 2 & \cdots & (m-1) & m & (m+1) & \cdots & (2m-3) & (2m-2) \end{array} \end{array} \tag{5.44}$$

In the top and bottom rows of the matrix $\mathbf{F_{SJ}}$ the on-state logic symbol '1' only appears once, whereas in all other rows the symbol '1' appears twice. These reveal that the top and bottom reinjection paths conduct once every one sixth of the fundamental period, and that all of the other reinjection paths conduct twice every one sixth of the fundamental period, i.e. the top and bottom reinjection paths switching frequency is six times the fundamental frequency of the power system, while that of the other paths is twelve times the fundamental frequency.

Based on Equation 5.43, the waveform of the path currents can be determined easily when the current i_j full cycle waveform is obtained. The steady state waveforms of 8 path currents are shown in Figure 5.12.

5.5.3 DC Capacitor Current Waveforms

The currents of the $(m-1)$ capacitors are determined by the state combinations of the m ideal switch paths and currents i_{cu} and i_{cd}. The currents i_{cu} and i_{cd} are determined by the dc current I_{dc} and the two converter output currents i_{Ydc} and $i_{\Delta dc}$. To simplify the analysis, the dc current I_{dc} is assumed to be an ideal dc current of constant value. Thus the currents i_{cu} and i_{cd} are given by

$$i_{cu} = i_{\Delta dc} - I_{dc} \qquad i_{cd} = i_{Ydc} - I_{dc} \tag{5.45}$$

Because there is only one ideal switch path in on-state at any instant, the currents through the capacitors which are above the node connected with the on-state ideal switch path, are the same, i.e. current i_{cu}, while the currents through the capacitors which are below the node connected with the on state ideal switch path, are also the same, i.e. current i_{cd}. It is clear that the capacitor current waveforms are related to the switching sequence. Depending on the firing synchronization relation between the two main bridges and the reinjection multi-level VSC, if the output voltage of the converter system is expressed by Equation 5.8, the currents of the $(m-1)$ capacitors for the specific time intervals are expressed as follows.

$$\mathbf{I_{cap}}(\omega\mathbf{t}) = [i_{c1} \quad i_{c2} \quad \cdots \quad i_{c(m-1)}]^T = \mathbf{F_{cap}}(\omega\mathbf{t})[i_{cu}(\omega t) \quad i_{cd}(\omega t)] \tag{5.46}$$

where $\mathbf{F_{cap}}(\omega\mathbf{t})$ is a $(m-1)\times 2$, time domain matrix. In interval $-\alpha < \omega t < \frac{\pi}{3} + \alpha$, it can be described by $(2m+1)$ discrete constant matrices determined by the state sequence of the m ideal switch paths. These $(2m+1)$ discrete constant matrices are listed below.

$$-\alpha < \omega t < \alpha \quad \alpha < \omega t < 3\alpha \quad \cdots \quad \tfrac{\pi}{6} - 3\alpha < \omega t < \tfrac{\pi}{6} - \alpha \quad \tfrac{\pi}{6} - \alpha < \omega t < \tfrac{\pi}{6} + \alpha$$

$$\begin{bmatrix} 1 & 0 \\ 1 & 0 \\ \vdots & \vdots \\ 1 & 0 \\ 1 & 0 \end{bmatrix} \quad \begin{bmatrix} 0 & 1 \\ 1 & 0 \\ \vdots & \vdots \\ 1 & 0 \\ 1 & 0 \end{bmatrix} \quad \cdots \quad \begin{bmatrix} 0 & 1 \\ 0 & 1 \\ \vdots & \vdots \\ 0 & 1 \\ 1 & 0 \end{bmatrix} \quad \begin{bmatrix} 0 & 1 \\ 0 & 1 \\ \vdots & \vdots \\ 0 & 1 \\ 0 & 1 \end{bmatrix}$$

$$\tfrac{\pi}{6}+\alpha < \omega t < \tfrac{\pi}{6}+3\alpha \quad \cdots \quad \tfrac{\pi}{3}-3\alpha < \omega t < \tfrac{\pi}{3}-\alpha \quad \tfrac{\pi}{3}-\alpha < \omega t < \tfrac{\pi}{3}+\alpha$$

$$\begin{bmatrix} 0 & 1 \\ 0 & 1 \\ \vdots & \vdots \\ 0 & 1 \\ 1 & 0 \end{bmatrix} \quad \cdots \quad \begin{bmatrix} 0 & 1 \\ 1 & 0 \\ \vdots & \vdots \\ 1 & 0 \\ 1 & 0 \end{bmatrix} \quad \begin{bmatrix} 1 & 0 \\ 1 & 0 \\ \vdots & \vdots \\ 1 & 0 \\ 1 & 0 \end{bmatrix} \tag{5.47}$$

Figure 5.9 and 5.10 show the current waveforms of the MLVR-VSC for capacitive operation. The waveforms of the currents i_{c1} to i_{c7} through the dc capacitors in Figure 5.1 for capacitive operation are respectively shown in Figure 5.11.

5.6 COMPONENT RATINGS

The reinjection converter system nominal apparent power rating (ignoring the component caused by the small harmonic current) is

$$S_s = 3S = 3V_{SR}I_{SR} \tag{5.48}$$

where V_{SR} is the fundamental phase RMS voltage, and I_{SR} is the fundamental phase RMS current of the reinjection converter system output. The ratings of all the components in the system are derived based on the condition that the converter system is directly connected to an ideal three phase sinusoidal waveform voltage source with RMS voltage, V_{SR}, operating under perfectly balanced conditions, and the fundamental RMS value of the output phase current I_A, is the converter system rated RMS current I_{SR}. The reinjection converter system dc side voltage U_{dc} is divided into $m-1$ equal levels, and the voltages across the two main bridges consist of m levels (from 0 to U_{dc}) of a staircase shape waveform.

5.6.1 Interface Transformers

On the assumption that the interface transformer primary windings are directly connected to an ideal power system, and since the secondary windings are directly connected to the converter bridges, with the reference of the model in Figure 5.5, the fundamental RMS voltage is

$$V_{Ar} = \sqrt{V_{SR}^2 + (X_s I_{SR})^2 + 2V_{SR}X_s I_{SR}\sin(\theta)} \tag{5.49}$$

where θ is the displacement angle between the source voltage V_{SR} and current I_{SR}, and X_s is the fundamental frequency leakage reactance of the series connected interfacing transformers. It is obvious that when $\theta = 90^o$ (namely pure capacitive operation), the output voltage of the reinjection converter system coupled from the converter side windings has the maximum RMS value, i.e.

$$V_{AR} = V_{SR} + X_s I_{SR} = V_{SR}(1 + \frac{X_s}{V_{SR}/I_{SR}}) = V_{SR}(1 + k_s) \tag{5.50}$$

where k_s is the nominal leakage fundamental reactance of the interface transformer.

Because the primary (the power system side) windings are connected in series, the output voltage of the reinjection converter system is the sum of the two primary winding

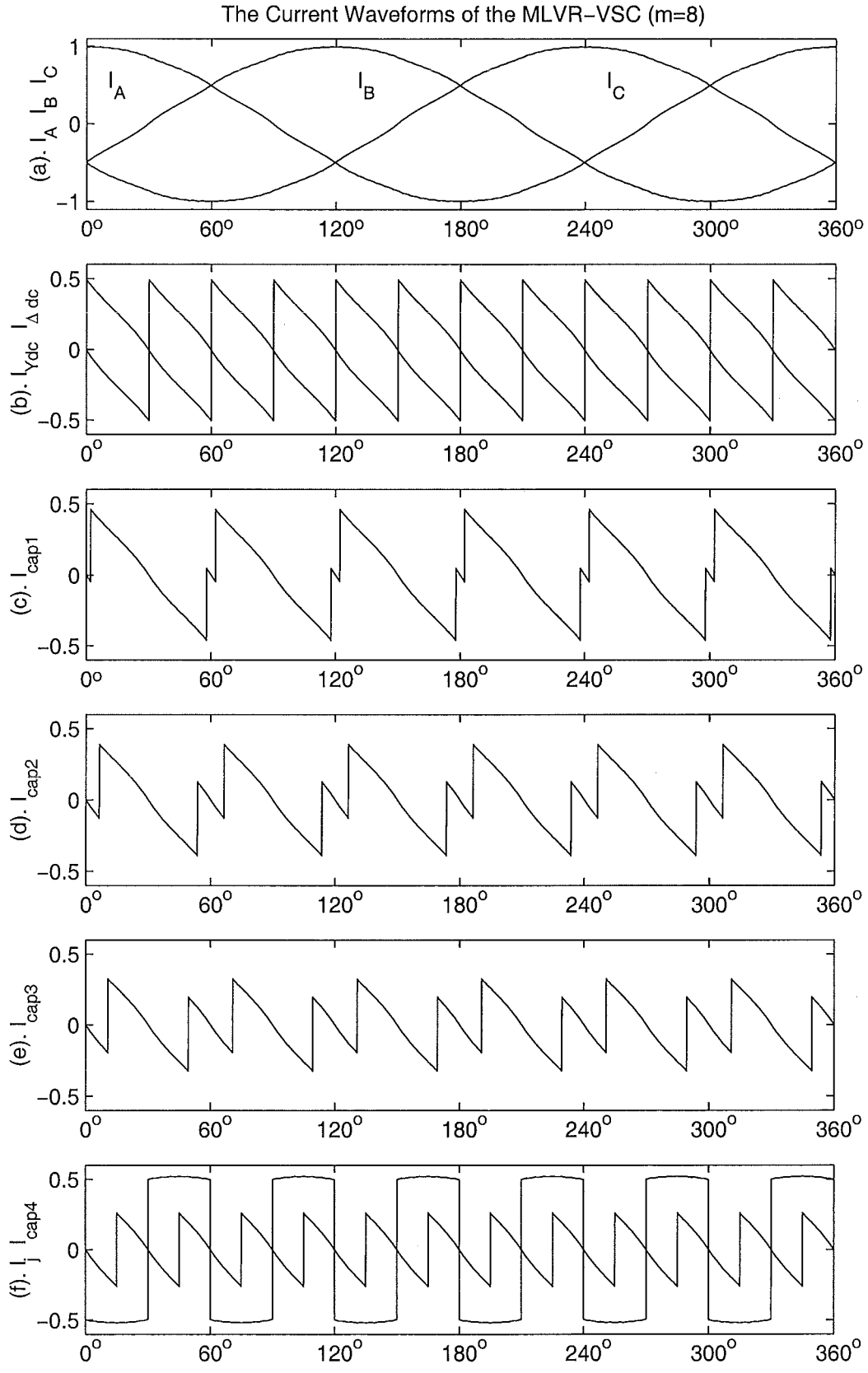


Figure 5.9 The Current Waveforms of the 8-level MLVR-VSC

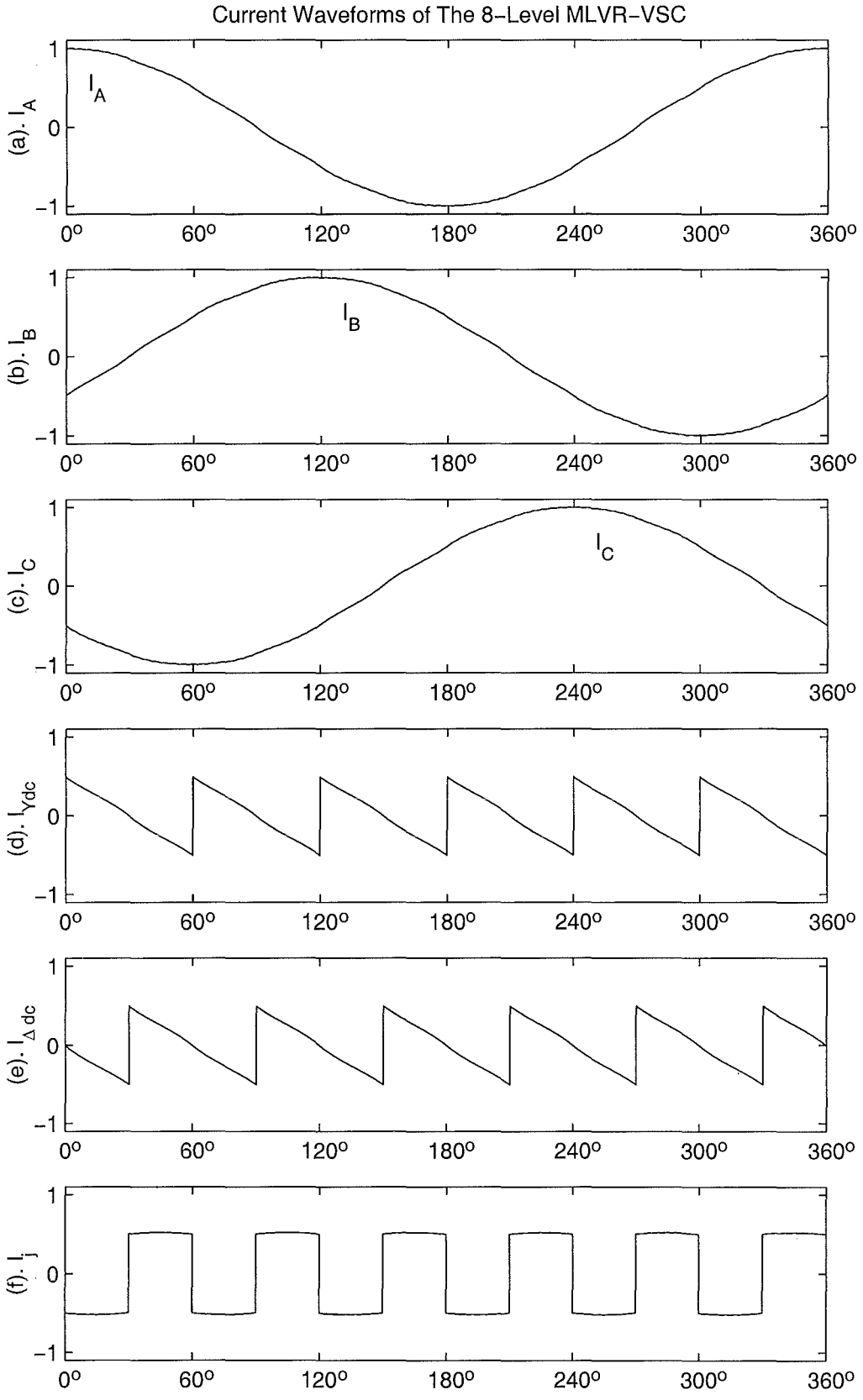


Figure 5.10 The Current Waveforms of the 8-level MLVR-VSC

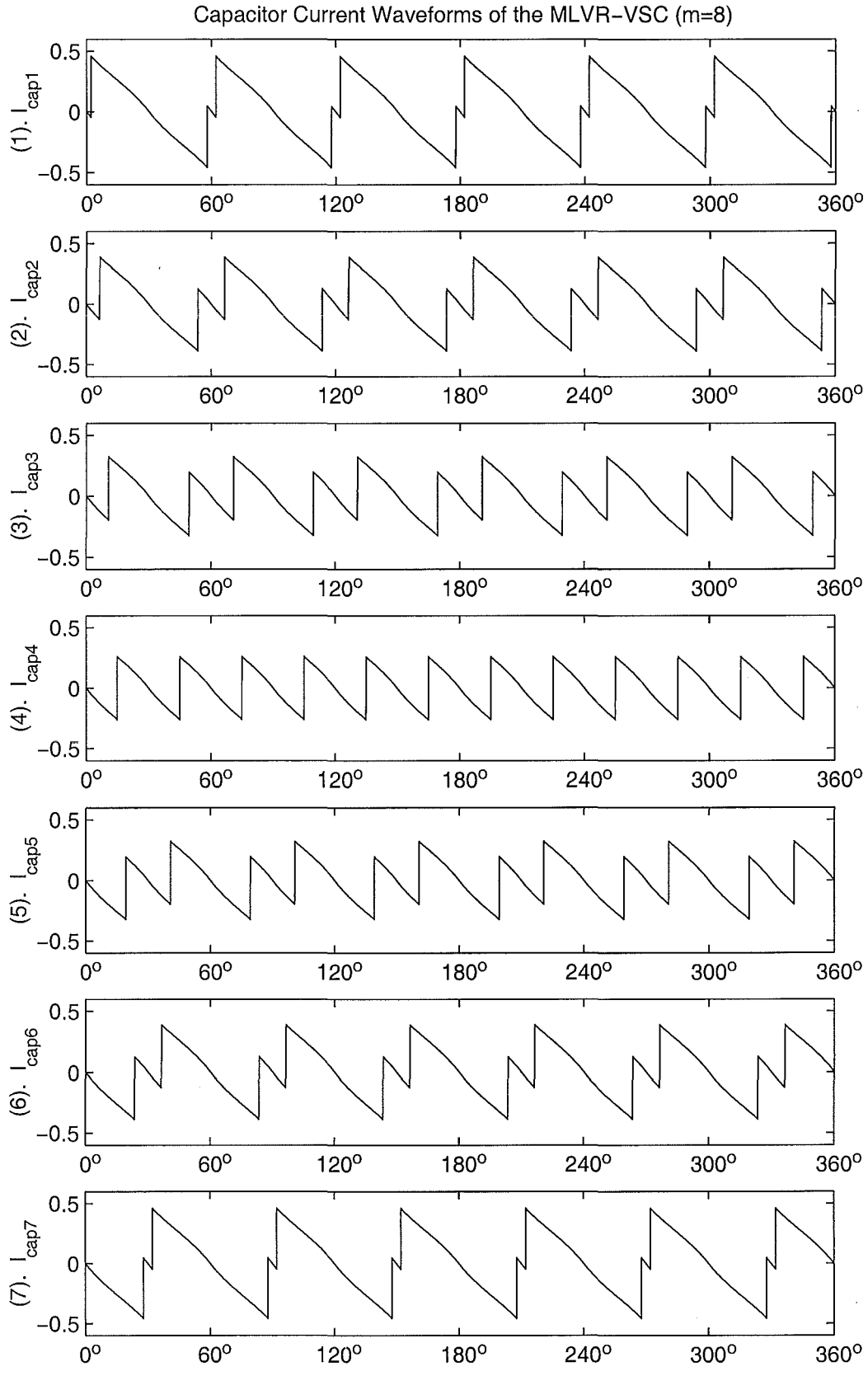


Figure 5.11 The capacitor Current Waveforms of the 8-level MLVR-VSC

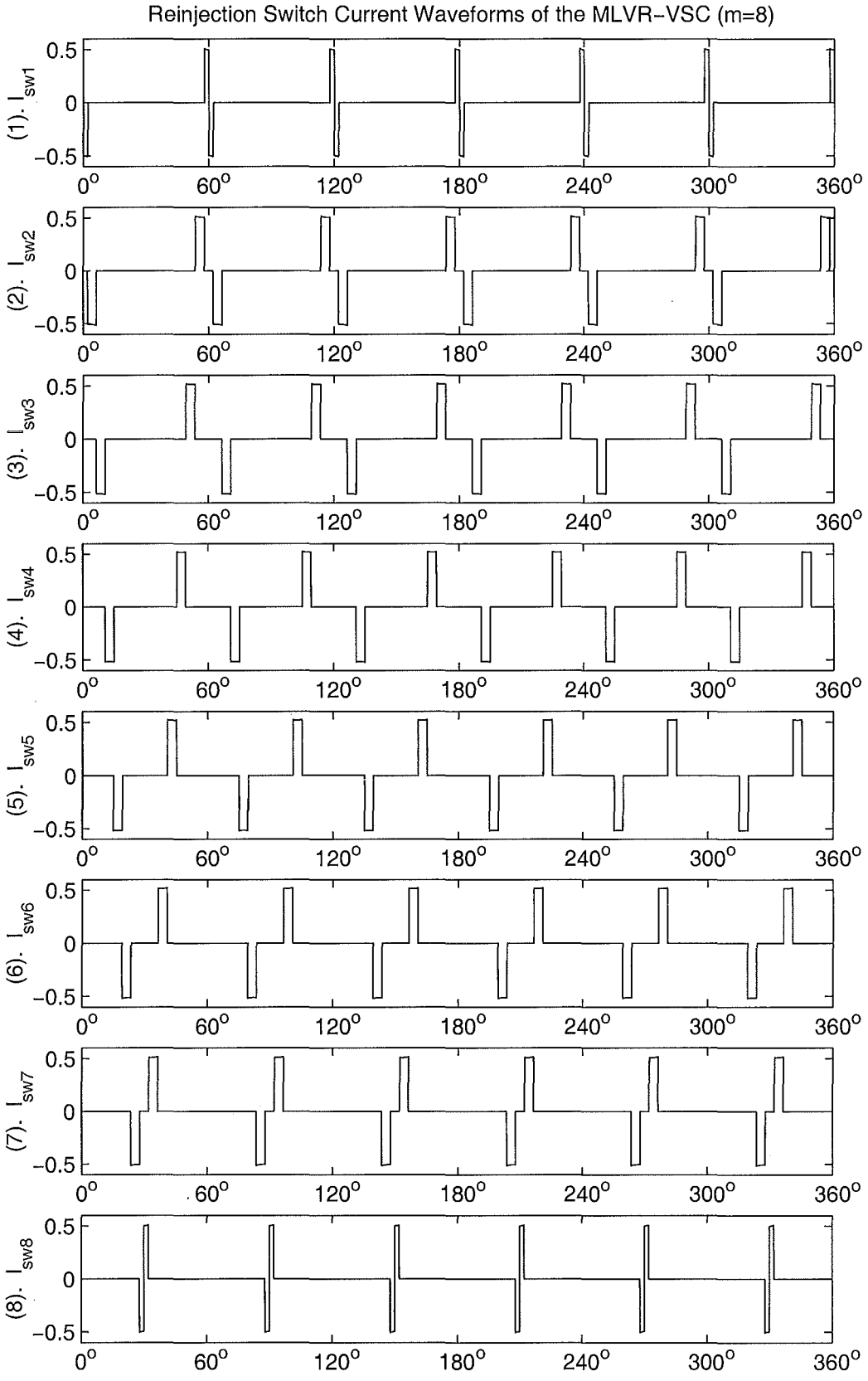


Figure 5.12 The Current Waveforms of the Reinjection Paths

voltages, and the rated converter system current is the winding current of the interface transformers.

As the analysis in the previous section reveals, the converter side winding voltages of the interface transformers are related to the dc capacitor voltages, including harmonics. From Equation 5.10 the dc voltage across all of the capacitors at the rated condition is given by

$$\begin{aligned} U_{dcR} &= \frac{\sqrt{2}\pi(m-1)(1+k_s)V_{SR}}{16k_n \sin(\frac{\pi}{12(m-1)})[\frac{(m-1)}{2} + \sum_{i=1}^{m-2} i\cos(\frac{\pi}{6} - \frac{i\pi}{6(m-1)})]} \\ &= Q_{Vdc}(m)k_n^{-1}(1+k_s)V_{SR} \end{aligned} \tag{5.51}$$

where k_n is the turns ratio (primary to secondary) of the Y/Y connection interface transformer ($k_n/\sqrt{3}$ for Y/Δ connection interface transformer). The symbol $Q_{Vdc}(m)$ is a function of the level number m, and it rises slightly when m increases sharply. Its practical minimum value is 2.164 for $m = 3$, and when m tends to infinity it reaches a maximum value of 2.170.

The rated fundamental RMS voltage of the primary windings is the same for the Y/Y and Y/Δ connection interface transformers. It is

$$U_{pfR} = 0.5V_{AR} = 0.5(1+k_s)V_{SR} \tag{5.52}$$

The peak value for the Y/Y connection interface transformer is

$$\begin{aligned} U_{peakY} &= \frac{\sqrt{2}\pi(m-1)(1+k_s)V_{SR}}{24\sin(\frac{\pi}{12(m-1)})[\frac{(m-1)}{2} + \sum_{i=1}^{m-2} i\cos(\frac{\pi}{6} - \frac{i\pi}{6(m-1)})]} \\ &= \frac{2Q_{Vdc}(m)}{3}(1+k_s)V_{SR} \end{aligned} \tag{5.53}$$

and the peak value for Y/Δ connection transformer

$$\begin{aligned} U_{peak\Delta} &= \frac{\sqrt{2}\pi(m-1)(1+k_s)V_{SR}}{16\sqrt{3}\sin(\frac{\pi}{12(m-1)})[\frac{(m-1)}{2} + \sum_{i=1}^{m-2} i\cos(\frac{\pi}{6} - \frac{i\pi}{6(m-1)})]} \\ &= \frac{Q_{Vdc}(m)}{\sqrt{3}}(1+k_s)V_{SR} \end{aligned} \tag{5.54}$$

Both transformers have a primary phase voltage RMS value of

$$\begin{aligned} U_{pRMS} &= \frac{\sqrt{6}\pi(m-1)(1+k_s)\sqrt{2+\frac{1}{(m-1)^2}}V_{SR}}{144\sin(\frac{\pi}{12(m-1)})[\frac{(m-1)}{2} + \sum_{i=1}^{m-2} i\cos(\frac{\pi}{6} - \frac{i\pi}{6(m-1)})]} \\ &= Q_{RMS}(m)(1+k_s)V_{SR} \end{aligned} \tag{5.55}$$

Although most of the voltage harmonics are absent on the power system side, the

converter transformers have to cope with their presence. This is reflected in the m's function $Q_{RMS}(m)$, its minimum and maximum being $Q_{RMS}(\infty) = 0.590723386$ and $Q_{RMS}(3) = 0.624768987$ respectively.

Under the rated operation condition, the voltages on the converter side windings can be obtained directly by multiplication of the primary voltages by the turn ratio k_n^{-1}.

From Equations 5.31 and 5.33, the primary winding current RMS value for the rated operation condition is

$$I_{\Lambda RMS} = I_{SR}\sqrt{1 + [P(m) - 1](1 + k_s^{-1})^2} \tag{5.56}$$

The corresponding voltage and current ratings on the power system side windings are summarized in Table 5.1. All these expressions are based on the rated system voltage V_{SR} and current I_{SR}. Since each of the two interface transformer nominal MVA ratings is different from $0.5V_{SR}I_{SR}$, a normalized leakage reactance k_s is defined, i.e. $k_s = X_s/(V_{SR}/I_{SR})$. $Q_Y(m)$, $Q_\Delta(m)$ and $Q_{RMS}(m)$ in the table are all m's functions, and $Q_Y(m) = \frac{2}{3}Q_{Vdc}(m)$, $Q_\Delta(m) = \frac{1}{\sqrt{3}}Q_{Vdc}(m)$, $Q_{RMS}(m) = \frac{1}{3\sqrt{3}}\sqrt{2 + \frac{1}{(m-1)^2}}Q_{Vdc}(m)$. Finally the symbol $B(m)$ in the Table 5.1 is equal to $[P(m) - 1](1 + 1/k_s)^2$.

Table 5.1 Interface transformer ratings

		Y/Y connection transformer	Y/Δ connection transformer
phase voltage	peak voltage	$U_{peakY} = Q_Y(m)(1 + k_s)V_{SR}$	$U_{peak\Delta} = Q_\Delta(m)(1 + k_s)V_{SR}$
	RMS value	$U_{RMS} = Q_{RMS}(m)(1 + k_s)V_{SR}$	$U_{RMS} = Q_{RMS}(m)(1 + k_s)V_{SR}$
	fundamental	$U_{fRMS} = 0.5(1 + k_s)V_{SR}$	$U_{fRMS} = 0.5(1 + k_s)V_{SR}$
phase current	RMS value	$I_{ARMS} = I_{SR}\sqrt{1 + B(m)}$	$I_{ARMS} = I_{SR}\sqrt{1 + B(m)}$
	fundamental	$I_{AfRMS} = I_{SR}$	$I_{AfRMS} = I_{SR}$

5.6.2 Main Switches

The switch arms in the two main bridges have the same voltage ratings. The maximum voltage across each switch arm is

$$\begin{aligned} U_{GDm} &= \frac{\sqrt{2}\pi(m-1)k_n^{-1}(1 + k_s)V_{SR}}{16\sin(\frac{\pi}{12(m-1)})[\frac{(m-1)}{2} + \sum_{i=1}^{m-2} i\cos(\frac{\pi}{6} - \frac{i\pi}{6(m-1)})]} \\ &= Q_{dc}(m)k_n^{-1}(1 + k_s)V_{SR} \end{aligned} \tag{5.57}$$

The current waveforms of the main switches depend on the converter system output current waveform and the firing pattern. From Equation 5.31-5.33, the total harmonic

distortion of the converter system output current at the rated condition is

$$THD_{IR} = \frac{\sqrt{P(m)-1}}{k} = \sqrt{P(m)-1} \cdot \frac{V_{A1rms}}{V_{SR}} \cdot \frac{1}{k_s} \tag{5.58}$$

and the possible maximum value of the voltage, V_{A1rms}, is $(1+k_s)V_{SR}$, and the practical maximum of $P(m)$ is $P(3) = 1 + 5.096940954 \times 10^{-6}$. Thus the maximum value of the total harmonic distortion of the converter system output current at the rated condition is

$$THD_{IRmax} = 2.258 \times 10^{-3} \cdot \frac{1+k_s}{k_s} \tag{5.59}$$

By choosing a sufficiently large leakage reactance, the harmonic components of the converter system output current can be kept to a very low level, e.g. $k_s \geq 0.1$, $THD_{IRmax} \leq 2.48\%$, and $I_{ARMS} \leq 1.00031 I_{SR}$. That means that the switch current rating can be derived using only the fundamental component without introducing significant error.

Under nominal rated current operation, the RMS currents through the main switches and freewheel diodes only depend on the triggering pattern. To derive the current ratings of the switching devices in the main bridges, two possible operating states are considered, i.e. current leading voltage and current lagging voltage.

For the first operating state, if the converter system output current of phase A is expressed as $I_A(\omega t) = \sqrt{2} I_{SR} \sin(\omega t)$, and the main switch S_{Y1} is fired on in the period between $\omega t = \theta$ and $\omega t = \theta + \pi$ $(0 < \theta < \pi)$ (while the main switch S_{Y4} is off during this period), the current of G_{y1} can be expressed as

$$I_{Gy1}(\omega t) = \begin{cases} 0 & 0 < \omega t < \pi \\ \sqrt{2} k_n I_{sR} \sin(\omega t - \pi) & \pi < \omega t < \pi + \theta \\ 0 & \pi + \theta < \omega t < 2\pi \end{cases} \tag{5.60}$$

and the current of Diode D_{y1}

$$I_{Dy1}(\omega t) = \begin{cases} 0 & \omega t < \theta \\ \sqrt{2} k_n I_{sR} \sin(\omega t) & \theta < \omega t < \pi \\ 0 & \pi < \omega t < 2\pi \end{cases} \tag{5.61}$$

The RMS values of the currents $I_{Gy1}(\omega t)$ and $I_{Dy1}(\omega t)$ are respectively

$$I_{Gy1RMS} = I_{SR} k_n \sqrt{\frac{1}{\pi} \int_{\pi}^{\pi+\theta} \sin^2(\omega t - \pi) d\omega t} = I_{SR} k_n \sqrt{\frac{1}{2\pi} \left[\theta - 0.5 \sin(2\theta)\right]} \tag{5.62}$$

and

$$I_{Dy1RMS} = I_{SR}k_n\sqrt{\frac{1}{\pi}\int_{\theta}^{\pi}\sin^2(\omega t)d\omega t} = I_{SR}k_n\sqrt{\frac{1}{2} - \frac{1}{2\pi}\Big[\theta - 0.5\sin(2\theta)\Big]} \tag{5.63}$$

For the second operating state (i.e. the current lagging the voltage), if the converter system output current of phase A is expressed as $I_A(\omega t) = \sqrt{2}I_{SR}\sin(\omega t)$, and the main switch S_{Y1} is fired on in the period between $\omega t = \theta$ and $\omega t = \theta + \pi$ $(-\pi < \theta < 0)$ (while the main switch S_{Y4} is off during this period), the current of S_{Y1} can be expressed as

$$I_{Sy1}(\omega t) = \begin{cases} -\sqrt{2}k_n I_{sR}\sin(\omega t) & \theta < \omega t < 0 \\ 0 & 0 < \omega t < 2\pi + \theta \end{cases} \tag{5.64}$$

and the current of Diode D_{y1}

$$I_{Dy1}(\omega t) = \begin{cases} 0 & \omega t < 0 \\ \sqrt{2}k_n I_{sR}\sin(\omega t) & 0 < \omega t < \pi + \theta \\ 0 & \theta + \pi < \omega t < \theta + 2\pi \end{cases} \tag{5.65}$$

The RMS values of the currents $I_{Sy1}(\omega t)$ and $I_{Dy1}(\omega t)$ are respectively

$$I_{Sy1RMS} = I_{SR}k_n\sqrt{\frac{1}{\pi}\int_{\theta}^{0}\sin^2(\omega t)d\omega t} = I_{SR}k_n\sqrt{\frac{1}{2\pi}\Big[-\theta + 0.5\sin(2\theta)\Big]} \tag{5.66}$$

and

$$I_{Dy1RMS} = I_{SR}k_n\sqrt{\frac{1}{\pi}\int_{0}^{\theta+\pi}\sin^2(\omega t)d\omega t} = I_{SR}k_n\sqrt{\frac{1}{2} + \frac{1}{2\pi}\Big[\theta - 0.5\sin(2\theta)\Big]} \tag{5.67}$$

By the combination of the expressions of the two states, the current RMS ratings of the main switch and Diode are given by:

$$I_{Sy1RMS} = I_{SR}k_n\sqrt{\frac{1}{2\pi}|\theta - 0.5\sin(2\theta)|} \tag{5.68}$$

$$I_{Dy1RMS} = I_{SR}k_n\sqrt{\frac{1}{2} - \frac{1}{2\pi}|\theta - 0.5\sin(2\theta)|} \tag{5.69}$$

The maximum values of the GTO's and Diode's current RMS ratings (derived from Equations 5.68 and 5.69) are

$$I_{Sy1RMSmax} = I_{SR}k_n\sqrt{0.5} \quad for\ |\theta| \to \pm\pi \tag{5.70}$$

$$I_{Dy1RMSmax} = I_{SR}k_n\sqrt{0.5} \quad for\ |\theta| \to 0 \tag{5.71}$$

5.6.3 Reinjection Switches

As the reinjection switches are clamped to the series connected capacitors which equally share the dc bus voltage U_{dc}, if the voltage impulse caused by the stray inductance effect during the switching process is ignored, the voltages across the reinjection switches for the m-level reinjection VSC are all the level voltage $V_L = U_{dc}/(m-1)$. Taking into account the relation between the dc voltage and the rated source voltage, the reinjection switch maximum voltage is

$$\begin{aligned} U_{jGDm} &= \frac{\sqrt{2}\pi k_n^{-1}(1+k_s)V_{SR}}{16\sin(\frac{\pi}{12(m-1)})[\frac{(m-1)}{2}+\sum_{i=1}^{m-2} i\cos(\frac{\pi}{6}-\frac{i\pi}{6(m-1)})]} \\ &= \frac{Q_{dc}(m)}{(m-1)}k_n^{-1}(1+k_s)V_{SR} \end{aligned} \tag{5.72}$$

The currents of the reinjection switches are related to the reinjection current and the topological structure of the reinjection circuit. As described in chapter 4, there are different topological structures. Using the ideal switch paths shown in Figure 5.8 as the basic elements of the reinjection circuit, from which all the reinjection switch current ratings can be obtained, the following derivations are used to obtain the ideal path current ratings. For example, the current RMS rating of a switch which is commonly used by the ideal paths: i^{th}, j^{th}, $k^{th}, \cdots$, is given by the square root of the sum of the current squares of these paths(i^{th}, j^{th}, $k^{th}, \cdots$).

Under the assumption of the three-phase ac output currents being symmetrical, and the interface transformer turns ratios having the theoretical values, the reinjection current is a periodical function at six times the source fundamental frequency. Thus with the time reference fixed by Equation 5.14 and the phase displacement θ, between the converter output current and voltage, the reinjection current i_j under the rated condition can be written in the following simple form:

$$i_j(\omega t) = \begin{cases} 2\sqrt{2}k_n I_{SR}\sin(\frac{\pi}{12})\cos(\omega t+\theta+\frac{5\pi}{12}) & 0<\omega t<\frac{\pi}{6} \\ -2\sqrt{2}k_n I_{SR}\sin(\frac{\pi}{12})\cos(\omega t+\theta+\frac{\pi}{4}) & \frac{\pi}{6}<\omega t<\frac{\pi}{3} \end{cases} \tag{5.73}$$

The i^{th} $(for\ i = 2, 3, \cdots, m-1)$ ideal switch path current, i_{si} in the interval $0 \leftrightarrow \frac{\pi}{3}$ is expressed by

$$i_{si}(\omega t) = \begin{cases} 0 & 0<\omega t<\gamma_{i-1} \\ 2\sqrt{2}k_n I_{SR}\sin(\frac{\pi}{12})\cos(\omega t+\theta+\frac{5\pi}{12}) & \gamma_{i-1}<\omega t<\gamma_i \\ 0 & \gamma_i<\omega t<\lambda_{i-1} \\ -2\sqrt{2}k_n I_{SR}\sin(\frac{\pi}{12})\cos(\omega t+\theta+\frac{\pi}{4}) & \lambda_{i-1}<\omega t<\lambda_i \\ 0 & \lambda_i<\omega t<\frac{\pi}{3} \end{cases} \tag{5.74}$$

where $\gamma_{i-1}(=\beta_{i-1}+\delta_{i-1})$, $\gamma_i(=\beta_i+\delta_i)$ and $\lambda_{i-1}(=\frac{\pi}{3}-\beta_i+\delta_i)$, $\lambda_i(=\frac{\pi}{3}-\beta_{i-1}+\delta_{i-1})$

are the on-state starting and stopping angles of the i^{th} ideal switch path in the intervals $(0 \leftrightarrow \frac{\pi}{6})$ and $(\frac{\pi}{6} \leftrightarrow \frac{\pi}{3})$ respectively.

The RMS value of the reinjection current i_j is

$$I_{jRMS} = 2\sqrt{2}k_n I_{SR}\sin(\tfrac{\pi}{12})\sqrt{\tfrac{3}{\pi}[\int_0^{\frac{\pi}{6}}\cos^2(\omega t+\theta+\tfrac{5\pi}{12})d\omega t+\int_{\frac{\pi}{6}}^{\frac{\pi}{3}}\cos^2(\omega t+\theta+\tfrac{\pi}{4})d\omega t]}$$
$$= 2k_n I_{SR}\sin(\tfrac{\pi}{12})\sqrt{1-\tfrac{3}{\pi}\cos(2\theta)} \quad (5.75)$$

The RMS current of the i^{th} $(i = 2, 3, \cdots, m-1)$ reinjection ideal switch path is

$$I_{siRMS} = 2\sqrt{2}k_n I_{SR}\sin(\frac{\pi}{12})\sqrt{\frac{3}{\pi}[\int_{\gamma_{i-1}}^{\gamma_i}\cos^2(\omega t+\theta+\frac{5\pi}{12})d\omega t+\int_{\lambda_{i-1}}^{\lambda_i}\cos^2(\omega t+\theta+\frac{\pi}{4})d\omega t]}$$
$$= 2k_n I_{SR}\sin(\frac{\pi}{12})\sqrt{\frac{3}{\pi}[(\gamma_i-\gamma_{i-1})+(\lambda_i-\lambda_{i-1})+A_0(i)+B_0(i)]}$$
$$= 2k_n I_{SR}\sin(\frac{\pi}{12})\sqrt{\frac{3}{\pi}[\frac{\pi}{3(m-1)}+A_i-B_i]} \quad (5.76)$$

$$A_0(i) = 0.5[\sin(2\gamma_i+2\theta+\frac{5\pi}{6})-\sin(2\gamma_{i-1}+2\theta+\frac{5\pi}{6})]$$
$$B_0(i) = 0.5[\sin(2\lambda_i+2\theta+\frac{\pi}{2})-\sin(2\lambda_{i-1}+2\theta+\frac{\pi}{2})]$$

$$A_i = \cos(2\theta+2\delta_i)\sin(\frac{\pi}{6}-2\beta_i) = \Big[\frac{2\cos^2(\theta)\cos^2(\frac{\pi}{12})}{\cos^2(\frac{\pi}{12}-\frac{(2i-1)\pi}{12(m-1)})}-1\Big]\sin(\frac{\pi}{6}-\frac{(2i-1)\pi}{6(m-1)}) \quad (5.77)$$

$$B_i = \cos(2\theta+2\delta_{i-1})\sin(\frac{\pi}{6}-2\beta_{i-1}) = \Big[\frac{2\cos^2(\theta)\cos^2(\frac{\pi}{12})}{\cos^2(\frac{\pi}{12}-\frac{(2i-3)\pi}{12(m-1)})}-1\Big]\sin(\frac{\pi}{6}-\frac{(2i-3)\pi}{6(m-1)}) \quad (5.78)$$

In the above equations δ_i and δ_{i-1} are the adjustments for the capacitor voltage balance (this issue will be discussed in next chapter), as these are small in value and in difference, the RMS current of the i^{th} $(i = 2, 3, \cdots, m-1)$ reinjection ideal switch path can be approximately expressed as

$$I_{siRMS} \approx 2k_n I_{SR}\sin(\tfrac{\pi}{12})\sqrt{\tfrac{3}{\pi}\{\tfrac{\pi}{3(m-1)}-2\sin(\tfrac{\pi}{6(m-1)})\cos(\tfrac{(m-2i+1)\pi}{6(m-1)})\cos(2\theta+2\delta_i)\}} \quad (5.79)$$
$$\approx 2k_n I_{SR}\sin(\tfrac{\pi}{12})\sqrt{\tfrac{3}{\pi}\{\tfrac{\pi}{3(m-1)}-2\sin(\tfrac{\pi}{6(m-1)})\cos(\tfrac{(m-2i+1)\pi}{6(m-1)})\cos(2\theta)\}} \quad (5.80)$$

The RMS currents of the first and m^{th} ideal switch paths are the same and are given by

$$I_{s1RMS} = I_{smRMS}$$
$$= 2\sqrt{2}k_n I_{SR}\sin(\tfrac{\pi}{12})\sqrt{\tfrac{3}{\pi}[\int_0^{\gamma_1}\cos^2(\omega t+\theta+\tfrac{5\pi}{12})d\omega t+\int_{\lambda_1}^{\frac{\pi}{3}}\cos^2(\omega t+\theta+\tfrac{\pi}{4})d\omega t]}$$
$$= 2k_n I_{SR}\sin(\tfrac{\pi}{12})\sqrt{\tfrac{3}{\pi}[\tfrac{\pi}{6(m-1)}+\cos(2\theta+2\delta_1)\sin(\tfrac{\pi}{6}-2\beta_1)-0.5\cos(2\theta)]} \quad (5.81)$$
$$\approx 2k_n I_{SR}\sin(\tfrac{\pi}{12})\sqrt{\tfrac{3}{\pi}[\tfrac{\pi}{6(m-1)}-2\sin(\tfrac{\pi}{12(m-1)})\cos\tfrac{(2m-3)\pi}{12(m-1)}\cos(2\theta)\}} \quad (5.82)$$

From Equation 5.75 it is clear that the RMS value of the reinjection current i_j varies with the power factor. Its maximum value is $0.724k_nI_{SR}$ at $\theta = \pm 90^o$, and its minimum value is $0.215k_nI_{SR}$ at $\theta = \pm 15^o$ for the stable operation of the reinjection converter system. Because the reinjection current is distributed between the m paths, the individual reinjection current ratings are relatively very low.

5.6.4 D.C. Side Capacitance

Under the rated operating condition the dc average voltage across the $m-1$ capacitors connected in series is given by

$$\begin{aligned} U_{dcR} &= \frac{\sqrt{2}\pi(m-1)(1+k_s)V_{SR}}{16k_n \sin(\frac{\pi}{12(m-1)})[\frac{(m-1)}{2} + \sum_{i=1}^{m-2} i\cos(\frac{\pi}{6} - \frac{i\pi}{6(m-1)})]} \\ &= Q_{Vdc}(m)k_n^{-1}(1+k_s)V_{SR} \end{aligned} \tag{5.83}$$

If the voltages across all the capacitors are kept balanced, the rated average voltages of each capacitor is one $(m-1)^{th}$ of the rated dc average voltage. As the theoretical analysis of the MLVR-VSC is based on constant dc level voltages, the capacitances of the dc capacitors must be sufficiently large to remove the capacitor voltages ripple. In practice the designed value of that capacitance is only high enough to ensure that the capacitor voltage ripple is within a specified margin.

The voltage ripple in the capacitors is caused by the currents flowing through them. In the multi-level reinjection converter system with capacitor voltage balance control, the current waveforms of the dc side capacitors are different, but their dc components must be the same in order to keep the capacitor voltage balance. However to ensure capacitor average voltage balance under the condition of equal dc current components, the capacitances of the individual dc side capacitors must be of the same value; therefore the capacitor voltage fluctuations are not the same.

To simplify the analysis, the reinjection converter system ac output currents are assumed symmetrical, and the interface transformer turns ratios are the theoretical values. To determine the voltage fluctuation of the dc side capacitors for the most critical conditions, a further assumption is made that the capacitor current ac content is solely determined by the ac components of the two main bridge dc output currents i_{Ydc} and $i_{\Delta dc}$, i.e. the ac components of the currents i_{Ydc} and $i_{\Delta dc}$ are all flowing through the dc capacitors. Under these assumptions the currents of the dc side $m-1$ capacitors are periodical functions at six times the source fundamental frequency, and every capacitor current can be described by two parts of sinusoidal waveforms, one is the part of the Y/Y bridge output current i_{Ydc}, and the other is the part of the Y/Δ bridge output current $i_{\Delta dc}$.

Thus under the rated condition, with the time reference fixed by Equation 5.14 and for

a power angle θ, the ac component of the i^{th} capacitor current is given by

$$i_{Caci} = \begin{cases} k_n\sqrt{2}I_{SR}\sin(\omega t+\theta+90^o)-I_{dc} & -\beta_i+\delta_i<\omega t<\beta_i+\delta_i \\ k_n\sqrt{2}I_{SR}\sin(\omega t+\theta+60^o)-I_{dc} & \beta_i+\delta_i<\omega t<\frac{\pi}{3}-\beta_i+\delta_i \end{cases} \tag{5.84}$$

where $\beta_i = \frac{(2i-1)\pi}{12(m-1)}$ is the point at which the i^{th} ideal switch is fired on under $\theta = \pm 90^o$ condition, δ_i is the adjustment for capacitor voltage balance (will be described in next chapter) and $I_{dc} = \frac{3}{\pi}\sqrt{2}k_nI_{SR}\cos\theta$ is the dc component of the two bridge dc side output currents.

Because the capacitor voltage ripple is caused by the ac components of the capacitor currents, the ac components of the i^{th} capacitor voltages are given by

$$\begin{aligned} V_{Caci}(\omega t) &= \begin{cases} \frac{k_n\sqrt{2}I_{SR}}{\omega C}\int_{-\beta_i+\delta_i}^{\omega t}[\cos(\omega t+\theta)-\frac{3}{\pi}\cos\theta]d\omega t & -\beta_i+\delta_i<\omega t<\beta_i+\delta_i \\ \frac{k_n\sqrt{2}I_{SR}}{\omega C}\{\int_{\beta_i+\delta_i}^{\omega t}[\sin(\omega t+\theta+60^o)-\frac{3}{\pi}\cos\theta]d\omega t & \\ \quad +2\cos(\theta+\delta_i)\sin\beta_i-\frac{6\beta_i}{\pi}\cos\theta\} & \beta_i+\delta_i<\omega t<\frac{\pi}{3}-\beta_i+\delta_i \end{cases} \\ &= \begin{cases} \frac{k_n\sqrt{2}I_{SR}}{\omega C}[\sin(\omega t+\theta)-\sin(\theta+\delta_i-\beta_i) & \\ \quad -\frac{3}{\pi}\cos\theta(\omega t+\beta_i-\delta_i)] & -\beta_i+\delta_i<\omega t<\beta_i+\delta_i \\ \frac{k_n\sqrt{2}I_{SR}}{\omega C}[\sin(\omega t+\theta-30^o)-\sin(\theta+\delta_i+\beta_i-30^o) & \\ \quad +2\cos(\theta+\delta_i)\sin\beta_i-\frac{3}{\pi}\cos\theta(\omega t+\beta_i-\delta_i)] & \beta_i+\delta_i<\omega t<\frac{\pi}{3}-\beta_i+\delta_i \end{cases} \end{aligned} \tag{5.85}$$

The possible peaks or troughs appear at $\omega t_1 = \cos^{-1}[\frac{3}{\pi}\cos\theta]-\theta$ $(-\beta_i+\delta_i<\omega t_1<\beta_i+\delta_i)$, and $\omega t_2 = \cos^{-1}[\frac{3}{\pi}\cos\theta]-\theta+30^o$ $(\beta_i+\delta_i<\omega t_2<\frac{\pi}{3}-\beta_i+\delta_i)$. The corresponding peak or trough values are

$$\left.\begin{aligned} V_{Cim1} &= \frac{k_n\sqrt{2}I_{SR}}{\omega C}\{\sqrt{1-(\frac{3}{\pi}\cos\theta)^2}-\sin(\theta+\delta_i-\beta_i) \\ &\quad -\frac{3}{\pi}\cos\theta[\cos^{-1}(\frac{3}{\pi}\cos\theta)-\theta+\beta_i-\delta_i]\} \quad -\beta_i+\delta_i<\omega t_1<\beta_i+\delta_i \\ V_{Cim2} &= \frac{k_n\sqrt{2}I_{SR}}{\omega C}\{\sqrt{1-(\frac{3}{\pi}\cos\theta)^2}-\sin(\theta+\delta_i+\beta_i-30^o)+2\cos(\theta+\delta_i)\sin\beta_i \\ &\quad -\frac{3}{\pi}\cos\theta[\cos^{-1}(\frac{3}{\pi}\cos\theta)-\theta+30^o+\beta_i-\delta_i]\} \quad \beta_i+\delta_i<\omega t_2<\frac{\pi}{3}-\beta_i+\delta_i \end{aligned}\right\} \tag{5.86}$$

By substituting $\delta_i = [\cos^{-1}(\frac{\cos\frac{\pi}{12}\cos\theta}{\cos(\frac{\pi}{12}-\beta_i)})-\theta]$ into Equation 5.86, V_{Cim1} and V_{Cim2} become functions of θ and β_i. Thus for a specified capacitor (i.e. β_i is fixed), V_{Cim1} and V_{Cim2} are solely determined by θ.

The greater one among the absolute values $|V_{Cim1}|$ and $|V_{Cim2}|$ is V_{jppi}, the peak to peak value of the i^{th} capacitor voltage ac component under the operating condition of a phase displacement θ between the reinjection converter system output current and voltage. And when θ is equal to $\pm 90^o$, V_{jppi} reaches its maximum value V_{Mjppi}

$$V_{Mjppi} = \begin{cases} \frac{k_n\sqrt{2}I_{SR}}{\omega C}[1-\cos\beta_i] & i>(m-1)/2 \\ \frac{k_n\sqrt{2}I_{SR}}{\omega C}[1-\cos(30^o-\beta_i)] & i<(m-1)/2 \end{cases} \tag{5.87}$$

It is obvious that the top and bottom capacitor voltage fluctuations are the same and higher than the middle ones. For the m level system the top and bottom capacitor voltage fluctuation (peak to peak value) is

$$V_{Mjpp1} = \frac{k_n\sqrt{2}I_{SR}}{\omega C}[1 - \cos(30^o - \frac{\pi}{12(m-1)})] \tag{5.88}$$

5.7 CONCLUSIONS

Based on the analysis carried out in this chapter, the following features of the MLVR-VSC can be summarized:

1. The voltages across the main bridges are periodically varying, linearly increasing and decreasing waveforms; these waveforms can be generated by a controllable voltage divider, which is powered by a dc voltage source.

2. Based on the reinjection concept of harmonic cancellation, the ac output voltage waveform is of high quality. The ac output voltage waveform of an m-level MLVR-VSC is equivalent to that of a $12(m-1)$-pulse conversion system.

3. A step by step periodically varying voltage with zero voltage levels is supplied to the main bridges and synchronized with the main bridge firings; the commutations of the main bridge switches always take place in the interval of zero voltage. This zero voltage switching condition provided by force-clamping the main bridges removes the need for a dead interval for the two valves in the same phase pole to commutate, as there is no risk of short-circuiting the dc source. Thus the reliability of the MLVR-VSC system is enhanced.

4. The zero switching condition enables the direct series connected power switches in the main bridge to be controlled synchronously without dynamic equal voltage sharing problems. That means that the series connected switches in the main bridge are of the same power rating and the two main bridges operate as a conventional six-pulse converter. The simple structure and control requirements of the main bridges makes the converter system compact and cost effective.

5. The interval length controllable ZVS condition provided by the force-clamping of the main bridges not only eliminates the switching losses, but also simplifies the snubber requirements. A snubber-less or very simple snubber structure can be used in the main bridge design, because the capacitive energy (due to the parasitic capacitance of the power switches) discharges before the switch to be turned on, and the stray inductor current is by-passed by the force-clamping during the turning off process.

6. The reinjection circuit is a single phase multi-level converter pole that functions like a controllable voltage divider. It is not involved in the main power conversion, only the ac component of the convert system dc output current will pass through it. This means that when the converter system operates on the high power factor condition, the reinjection circuitry power rating and the power losses would be very low.

7. Because the voltages across the converter bridges are controlled to rise and fall step by step, very low dV/dt is produced across the main bridge switches and at the converter system ac output terminals. This reduces the electromagnetic interference (EMI) and ensures that the power switches in the main bridge operate properly and without the need of filters to prevent the insulation damage at the interface transformers.

The main shortcoming of the present MLVR-VSC is lack of individual phase voltage control to ensure the three phase current balance during ac source voltage unbalance. This is a matter for further work.

Chapter 6

MLVR-VSC CAPACITOR VOLTAGE BALANCING

6.1 INTRODUCTION

In previous chapters the voltages across the dc side capacitors have been assumed to be equal, (i.e. kept in perfect balance). This is an essential condition for the multi-level reinjection converter system to operate properly. It is thus important to verify under what operating conditions the voltages across the dc side capacitors can be kept in stable balance. With this purpose the following analysis uses power angle θ (the phase angle displacement between the converter system output current and voltage fundamental components) as the converter operation index.

6.2 CAPACITOR VOLTAGES OF EQUAL ON-STATE CONTROL

The converter system output voltage and current (given by Equations 5.14 and 5.20) are now written in the following slightly modified forms.

$$\mathbf{V_o}(\omega\mathbf{t}) = \begin{bmatrix} v_A(\omega t) \\ v_B(\omega t) \\ v_C(\omega t) \end{bmatrix} = \begin{bmatrix} \sum_{n=1}^{\infty} V_{An} \sin(n\omega t) \\ \sum_{n=1}^{\infty} V_{Bn} \sin(n\omega t - 120^o) \\ \sum_{n=1}^{\infty} V_{Cn} \sin(n\omega t + 120^o) \end{bmatrix} \tag{6.1}$$

where $V_{An} = V_{Bn} = V_{Cn}$, because the MLVR-VSC always outputs symmetrical three-phase ac voltages based on the symmetrical firing control and the same dc voltage.

$$\mathbf{I_o}(\omega\mathbf{t}) = \begin{bmatrix} i_A(\omega t) \\ i_B(\omega t) \\ i_C(\omega t) \end{bmatrix} = \begin{bmatrix} \sum_{n=1}^{\infty} I_{An} \sin(n\omega t + \theta_{An}) \\ \sum_{n=1}^{\infty} I_{Bn} \sin(n\omega t - 120^o + \theta_{Bn}) \\ \sum_{n=1}^{\infty} I_{Cn} \sin(n\omega t + 120^o + \theta_{Cn}) \end{bmatrix} \tag{6.2}$$

Their main difference is that the source voltage has been removed from the above expressions, its influence being represented by the output current fundamental and harmonic component amplitudes, I_{An}, I_{Bn}, I_{Cn} $(n = 1, 2, \cdots)$ and phase displacement angles θ_{An}, θ_{Bn}, θ_{Cn} $(n = 1, 2, \cdots)$; the modification has been made to take into account possible asymmetry and distortion in the voltage source.

Based on the expressions derived in section 5.5.2, i_{cu} and i_{cd}, the currents through the capacitors, can be determined by the following procedure.

To take into account possible turns ratio differences from the nominal, the interface transformer secondary line currents are expressed by

$$\begin{bmatrix} i_{Ya}(\omega t) \\ i_{Yb}(\omega t) \\ i_{Yc}(\omega t) \end{bmatrix} = k_{Yn} \begin{bmatrix} i_A(\omega t) \\ i_B(\omega t) \\ i_C(\omega t) \end{bmatrix} \tag{6.3}$$

$$\begin{bmatrix} i_{\Delta a}(\omega t) \\ i_{\Delta b}(\omega t) \\ i_{\Delta c}(\omega t) \end{bmatrix} = k_{\Delta n} \begin{bmatrix} i_A(\omega t + 30^o) \\ i_B(\omega t + 30^o) \\ i_C(\omega t + 30^o) \end{bmatrix} \tag{6.4}$$

where k_{Yn} and $k_{\Delta n}$ are turns ratios of the two interface transformers, (the Y/Y connection transformer turns ratio is $k_{Yn} : 1$; the Y/Δ connection transformer turns ratio is $k_{\Delta n} : \sqrt{3}$).

The dc output currents of the two main bridges (given by Equations 5.37–5.40) are

$$i_{Ydc}(\omega t) = \mathbf{f_{sY}}(\omega \mathbf{t}) \begin{bmatrix} i_{Ya}(\omega t) \\ i_{Yb}(\omega t) \\ i_{Yc}(\omega t) \end{bmatrix} \tag{6.5}$$

$$i_{\Delta dc}(\omega t) = \mathbf{f_{s\Delta}}(\omega \mathbf{t}) \begin{bmatrix} i_{\Delta a}(\omega t) \\ i_{\Delta b}(\omega t) \\ i_{\Delta c}(\omega t) \end{bmatrix} \tag{6.6}$$

They relate to the converter system output current $\mathbf{I_o}(\omega \mathbf{t})$, as follows

$$i_{Ydc}(\omega t) = k_{Yn} \begin{cases} -i_B(\omega t) & 0 < \omega t < \frac{\pi}{3} \\ i_A(\omega t) & \frac{\pi}{3} < \omega t < \frac{2\pi}{3} \\ -i_C(\omega t) & \frac{2\pi}{3} < \omega t < \pi \\ i_B(\omega t) & \pi < \omega t < \frac{4\pi}{3} \\ -i_A(\omega t) & \frac{4\pi}{3} < \omega t < \frac{5\pi}{3} \\ i_C(\omega t) & \frac{5\pi}{3} < \omega t < 2\pi \end{cases} \tag{6.7}$$

$$i_{\Delta dc}(\omega t) = k_{\Delta n} \begin{cases} -i_B(\omega t + 30^o) & -\frac{\pi}{6} < \omega t < \frac{\pi}{6} \\ i_A(\omega t + 30^o) & \frac{\pi}{6} < \omega t < \frac{\pi}{2} \\ -i_C(\omega t + 30^o) & \frac{\pi}{2} < \omega t < \frac{5\pi}{6} \\ i_B(\omega t + 30^o) & \frac{5\pi}{6} < \omega t < \frac{7\pi}{6} \\ -i_A(\omega t + 30^o) & \frac{7\pi}{6} < \omega t < \frac{3\pi}{2} \\ i_C(\omega t + 30^o) & \frac{3\pi}{2} < \omega t < \frac{11\pi}{6} \\ -i_B(\omega t + 30^o) & \frac{11\pi}{6} < \omega t < \frac{13\pi}{6} \end{cases} \tag{6.8}$$

The currents i_{cu} and i_{cd} through the dc capacitors are given by

$$i_{cu}(\omega t) = i_{Ydc}(\omega t) - I_{dcL} \quad i_{cd}(\omega t) = i_{\Delta dc}(\omega t) - I_{dcL} \tag{6.9}$$

where I_{dcL} is the load current of the converter system.

Based on equation 6.9, the reinjection current i_j is expressed by

$$\begin{aligned} i_j(\omega t) &= i_{cu}(\omega t) - i_{cd}(\omega t) \\ &= i_{\Delta dc}(\omega t) - i_{Ydc}(\omega t) \end{aligned}$$

$$= \begin{cases} -k_{\Delta n} i_B(\omega t + 30^o) + k_{Yn} i_B(\omega t) & 0 < \omega t < \frac{\pi}{6} \\ k_{\Delta n} i_A(\omega t + 30^o) + k_{Yn} i_B(\omega t) & \frac{\pi}{6} < \omega t < \frac{\pi}{3} \\ k_{\Delta n} i_A(\omega t + 30^o) - k_{Yn} i_A(\omega t) & \frac{\pi}{3} < \omega t < \frac{\pi}{2} \\ -k_{\Delta n} i_C(\omega t + 30^o) - k_{Yn} i_A(\omega t) & \frac{\pi}{2} < \omega t < \frac{2\pi}{3} \\ -k_{\Delta n} i_C(\omega t + 30^o) + k_{Yn} i_C(\omega t) & \frac{2\pi}{3} < \omega t < \frac{5\pi}{6} \\ k_{\Delta n} i_B(\omega t + 30^o) + k_{Yn} i_C(\omega t) & \frac{5\pi}{6} < \omega t < \pi \\ k_{\Delta n} i_B(\omega t + 30^o) - k_{Yn} i_B(\omega t) & \pi < \omega t < \frac{7\pi}{6} \\ -k_{\Delta n} i_A(\omega t + 30^o) - k_{Yn} i_B(\omega t) & \frac{7\pi}{6} < \omega t < \frac{4\pi}{3} \\ -k_{\Delta n} i_A(\omega t + 30^o) + k_{Yn} i_A(\omega t) & \frac{4\pi}{3} < \omega t < \frac{3\pi}{2} \\ k_{\Delta n} i_C(\omega t + 30^o) + k_{Yn} i_A(\omega t) & \frac{3\pi}{2} < \omega t < \frac{5\pi}{3} \\ k_{\Delta n} i_C(\omega t + 30^o) - k_{Yn} i_C(\omega t) & \frac{5\pi}{3} < \omega t < \frac{11\pi}{6} \\ -k_{\Delta n} i_B(\omega t + 30^o) - k_{Yn} i_C(\omega t) & \frac{11\pi}{6} < \omega t < 2\pi \end{cases} \tag{6.10}$$

The vector of capacitor currents is $\mathbf{I_{cap}}(\omega \mathbf{t}) = [i_{c1} \;\; i_{c2} \;\; \cdots \;\; i_{c(m-1)}]^T$, and the currents through the $m-1$ capacitors are listed below:

$$i_{c1} = \begin{cases} -k_{\Delta n} i_B(\omega t + 30^o) - I_{dc} & -\alpha < \omega t < \alpha \\ -k_{Yn} i_B(\omega t) - I_{dc} & \alpha < \omega t < \frac{\pi}{3} - \alpha \\ k_{\Delta n} i_A(\omega t + 30^o) - I_{dc} & \frac{\pi}{3} - \alpha < \omega t < \frac{\pi}{3} + \alpha \\ k_{Yn} i_A(\omega t) - I_{dc} & \frac{\pi}{3} + \alpha < \omega t < \frac{2\pi}{3} - \alpha \\ -k_{\Delta n} i_C(\omega t + 30^o) - I_{dc} & \frac{2\pi}{3} - \alpha < \omega t < \frac{2\pi}{3} + \alpha \\ -k_{Yn} i_C(\omega t) - I_{dc} & \frac{2\pi}{3} + \alpha < \omega t < \pi - \alpha \\ k_{\Delta n} i_B(\omega t + 30^o) - I_{dc} & \pi - \alpha < \omega t < \pi + \alpha \\ k_{Yn} i_B(\omega t) - I_{dc} & \pi + \alpha < \omega t < \frac{4\pi}{3} - \alpha \\ -k_{\Delta n} i_A(\omega t + 30^o) - I_{dc} & \frac{4\pi}{3} - \alpha < \omega t < \frac{4\pi}{3} + \alpha \\ -k_{Yn} i_A(\omega t) - I_{dc} & \frac{4\pi}{3} + \alpha < \omega t < \frac{5\pi}{3} - \alpha \\ k_{\Delta n} i_C(\omega t + 30^o) - I_{dc} & \frac{5\pi}{3} - \alpha < \omega t < \frac{5\pi}{3} + \alpha \\ k_{Yn} i_C(\omega t) - I_{dc} & \frac{5\pi}{3} + \alpha < \omega t < 2\pi - \alpha \end{cases} \tag{6.11}$$

$$i_{c2} = \begin{cases} -k_{\Delta n} i_B(\omega t + 30^o) - I_{dc} & -3\alpha < \omega t < 3\alpha \\ -k_{Yn} i_B(\omega t) - I_{dc} & 3\alpha < \omega t < \frac{\pi}{3} - 3\alpha \\ k_{\Delta n} i_A(\omega t + 30^o) - I_{dc} & \frac{\pi}{3} - 3\alpha < \omega t < \frac{\pi}{3} + 3\alpha \\ k_{Yn} i_A(\omega t) - I_{dc} & \frac{\pi}{3} + 3\alpha < \omega t < \frac{2\pi}{3} - 3\alpha \\ -k_{\Delta n} i_C(\omega t + 30^o) - I_{dc} & \frac{2\pi}{3} - 3\alpha < \omega t < \frac{2\pi}{3} + 3\alpha \\ -k_{Yn} i_C(\omega t) - I_{dc} & \frac{2\pi}{3} + 3\alpha < \omega t < \pi - 3\alpha \\ k_{\Delta n} i_B(\omega t + 30^o) - I_{dc} & \pi - 3\alpha < \omega t < \pi + 3\alpha \\ k_{Yn} i_B(\omega t) - I_{dc} & \pi + 3\alpha < \omega t < \frac{4\pi}{3} - 3\alpha \\ -k_{\Delta n} i_A(\omega t + 30^o) - I_{dc} & \frac{4\pi}{3} - 3\alpha < \omega t < \frac{4\pi}{3} + 3\alpha \\ -k_{Yn} i_A(\omega t) - I_{dc} & \frac{4\pi}{3} + 3\alpha < \omega t < \frac{5\pi}{3} - 3\alpha \\ k_{\Delta n} i_C(\omega t + 30^o) - I_{dc} & \frac{5\pi}{3} - 3\alpha < \omega t < \frac{5\pi}{3} + 3\alpha \\ k_{Yn} i_C(\omega t) - I_{dc} & \frac{5\pi}{3} + 3\alpha < \omega t < 2\pi - 3\alpha \end{cases} \tag{6.12}$$

$$\vdots \qquad \vdots \qquad \vdots$$

$$i_{ci} = \begin{cases} -k_{\Delta n} i_B(\omega t + 30^o) - I_{dc} & -(2i-1)\alpha < \omega t < (2i-1)\alpha \\ -k_{Yn} i_B(\omega t) - I_{dc} & (2i-1)\alpha < \omega t < \frac{\pi}{3} - (2i-1)\alpha \\ k_{\Delta n} i_A(\omega t + 30^o) - I_{dc} & \frac{\pi}{3} - (2i-1)\alpha < \omega t < \frac{\pi}{3} + (2i-1)\alpha \\ k_{Yn} i_A(\omega t) - I_{dc} & \frac{\pi}{3} + (2i-1)\alpha < \omega t < \frac{2\pi}{3} - (2i-1)\alpha \\ -k_{\Delta n} i_C(\omega t + 30^o) - I_{dc} & \frac{2\pi}{3} - (2i-1)\alpha < \omega t < \frac{2\pi}{3} + (2i-1)\alpha \\ -k_{Yn} i_C(\omega t) - I_{dc} & \frac{2\pi}{3} + (2i-1)\alpha < \omega t < \pi - (2i-1)\alpha \\ k_{\Delta n} i_B(\omega t + 30^o) - I_{dc} & \pi - (2i-1)\alpha < \omega t < \pi + (2i-1)\alpha \\ k_{Yn} i_B(\omega t) - I_{dc} & \pi + (2i-1)\alpha < \omega t < \frac{4\pi}{3} - (2i-1)\alpha \\ -k_{\Delta n} i_A(\omega t + 30^o) - I_{dc} & \frac{4\pi}{3} - (2i-1)\alpha < \omega t < \frac{4\pi}{3} + (2i-1)\alpha \\ -k_{Yn} i_A(\omega t) - I_{dc} & \frac{4\pi}{3} + (2i-1)\alpha < \omega t < \frac{5\pi}{3} - (2i-1)\alpha \\ k_{\Delta n} i_C(\omega t + 30^o) - I_{dc} & \frac{5\pi}{3} - (2i-1)\alpha < \omega t < \frac{5\pi}{3} + (2i-1)\alpha \\ k_{Yn} i_C(\omega t) - I_{dc} & \frac{5\pi}{3} + (2i-1)\alpha < \omega t < 2\pi - (2i-1)\alpha \end{cases} \tag{6.13}$$

$$\vdots \qquad \vdots \qquad \vdots$$

$$i_{c(m-1)} = \begin{cases} -k_{\Delta n} i_B(\omega t + 30^o) - I_{dc} & -\frac{\pi}{6} + \alpha < \omega t < \frac{\pi}{6} - \alpha \\ -k_{Yn} i_B(\omega t) - I_{dc} & \frac{\pi}{6} - \alpha < \omega t < \frac{\pi}{6} + \alpha \\ k_{\Delta n} i_A(\omega t + 30^o) - I_{dc} & \frac{\pi}{6} + \alpha < \omega t < \frac{\pi}{2} - \alpha \\ k_{Yn} i_A(\omega t) - I_{dc} & \frac{\pi}{2} - \alpha < \omega t < \frac{\pi}{2} + \alpha \\ -k_{\Delta n} i_C(\omega t + 30^o) - I_{dc} & \frac{\pi}{2} + \alpha < \omega t < \frac{5\pi}{6} - \alpha \\ -k_{Yn} i_C(\omega t) - I_{dc} & \frac{5\pi}{6} - \alpha < \omega t < \frac{5\pi}{6} + \alpha \\ k_{\Delta n} i_B(\omega t + 30^o) - I_{dc} & \frac{5\pi}{6} + \alpha < \omega t < \frac{7\pi}{6} - \alpha \\ k_{Yn} i_B(\omega t) - I_{dc} & \frac{7\pi}{6} - \alpha < \omega t < \frac{7\pi}{6} + \alpha \\ -k_{\Delta n} i_A(\omega t + 30^o) - I_{dc} & \frac{7\pi}{6} + 3\alpha < \omega t < \frac{3\pi}{2} - \alpha \\ -k_{Yn} i_A(\omega t) - I_{dc} & \frac{3\pi}{2} - \alpha < \omega t < \frac{3\pi}{2} + \alpha \\ k_{\Delta n} i_C(\omega t + 30^o) - I_{dc} & \frac{3\pi}{2} + \alpha < \omega t < \frac{11\pi}{6} - \alpha \\ k_{Yn} i_C(\omega t) - I_{dc} & \frac{11\pi}{6} - \alpha < \omega t < \frac{11\pi}{6} + \alpha \end{cases} \tag{6.14}$$

where $\alpha = \frac{\pi}{12(m-1)}$ for Equations 6.11-6.14.

The above equations show that the (m-1) capacitor currents are periodical time functions. Every $\frac{\pi}{3}$ interval consists of two continuous current curves corresponding to the

two main bridge output currents, and there are six of these two curve groups in a full fundamental period for every capacitor current waveform.

The voltages across the dc capacitors are determined by integrating the currents flowing through them. The integrations of the $m-1$ capacitor currents on the source fundamental period are proportional to the voltage increments of the $m-1$ capacitors after every cycle. Because the i^{th} capacitor current i_{ci} represents the current of every capacitor, the integration of the current as expressed in Equation 6.13 will give the expression of the voltage increment for all the $m-1$ capacitors. Thus the capacitor voltage balance condition is achieved when the integration of this current is the same for all $i = 1,\ 2, \cdots\ (m-1)$.

The i^{th} capacitor voltage increment for every period of the source fundamental is given by

$$
\begin{aligned}
\Delta V_{Ci} &= \frac{1}{\omega C_i}\int_{-(2i-1)\alpha}^{2\pi-(2i-1)\alpha} i_{ci}\,d(\omega t) \\
&= \frac{1}{\omega C_i}\Big\{ -2\pi I_{dc} - 2k_{\Delta n}\sum_{n=1}^{\infty}\frac{I_{Bn}[1-(-1)^n]}{n}\sin\Big[\frac{(n-4)\pi}{6}+\theta_{Bn}\Big]\sin(n\beta_i) \\
&\quad -2k_{Yn}\sum_{n=1}^{\infty}\frac{I_{Bn}[1-(-1)^n]}{n}\sin\Big[\frac{(n-4)\pi}{6}+\theta_{Bn}\Big]\sin(\frac{n\pi}{6}-n\beta_i) \\
&\quad +2k_{\Delta n}\sum_{n=1}^{\infty}\frac{I_{An}[1-(-1)^n]}{n}\sin\Big[\frac{n\pi}{2}+\theta_{An}\Big]\sin(n\beta_i) \\
&\quad +2k_{Yn}\sum_{n=1}^{\infty}\frac{I_{An}[1-(-1)^n]}{n}\sin\Big[\frac{n\pi}{2}+\theta_{An}\Big]\sin(\frac{n\pi}{6}-n\beta_i) \\
&\quad -2k_{\Delta n}\sum_{n=1}^{\infty}\frac{I_{Cn}[1-(-1)^n]}{n}\sin\Big[\frac{(5n+4)\pi}{6}+\theta_{Cn}\Big]\sin(n\beta_i) \\
&\quad -2k_{Yn}\sum_{n=1}^{\infty}\frac{I_{Cn}[1-(-1)^n]}{n}\sin\Big[\frac{(5n+4)\pi}{6}+\theta_{Cn}\Big]\sin(\frac{n\pi}{6}-n\beta_i)\Big\}
\end{aligned}
\tag{6.15}
$$

where $\alpha = \frac{\pi}{12(m-1)}$, and $\beta_i = (2i-1)\alpha$.

It is obvious from Expression 6.15 that under the firing arrangement of equal on-state interval for every reinjection switch in the firing sequence, the voltage increments of the $(m-1)$ capacitors depend on their positions in the dc voltage divider, i.e. capacitor voltage balance is not achieved. Thus further investigation of the firing arrangement for the reinjection switches has to be carried out to achieve capacitor voltage balance.

6.3 ON-STATE ADJUSTMENTS FOR CAPACITOR VOLTAGE BALANCING

Capacitor voltage balance can be achieved by ensuring that all the capacitor current period integrations are equal for every period. Because the capacitor current periodic

integration is proportional to its dc current component, the capacitor voltage balance assessment is based on the dc component analysis of the converter system reinjection circuit.

With reference to Figure 5.8, $I_{\Delta dc}$, I_{Ydc}, I_{cu}, I_{cd}, and I_{S1} to I_{Sm} are used to represent the dc components of currents $i_{\Delta dc}$, i_{Ydc}, i_{cu}, i_{cd}, and i_{S1} to i_{Sm} respectively. For the steady state operation, the dc component currents through the (m-1) capacitors, I_{c1} to $I_{c(m-1)}$, are given by the following expressions based on the reinjection circuit topological structure:

$$\begin{array}{lcl} I_{c(m-1)} & = & I_{cu} - I_{Sm} \\ I_{c(m-2)} & = & I_{c(m-1)} - I_{S(m-1)} \\ I_{c(m-3)} & = & I_{c(m-2)} - I_{S(m-2)} \\ \vdots & & \vdots \\ I_{ci} & = & I_{c(i+1)} - I_{S(i+1)} \\ \vdots & & \vdots \\ I_{c2} & = & I_{c3} - I_{S3} \\ I_{c1} & = & I_{c2} - I_{S2} = I_{cd} + I_{S1} \end{array} \tag{6.16}$$

These expressions can be rewritten in the form below.

$$\left\{ \begin{array}{lcl} I_{c(m-2)} & = & I_{c(m-1)} - I_{S(m-1)} \\ I_{c(m-3)} & = & I_{c(m-1)} - \sum_{j=m-2}^{(m-1)} I_{Sj} \\ \vdots & & \vdots \\ I_{ci} & = & I_{c(m-1)} - \sum_{j=i+1}^{(m-1)} I_{Sj} \\ \vdots & & \vdots \\ I_{c2} & = & I_{c(m-1)} - \sum_{j=3}^{(m-1)} I_{Sj} \\ I_{c1} & = & I_{c(m-1)} - \sum_{j=2}^{(m-1)} I_{Sj} \end{array} \right. \tag{6.17}$$

and

$$\left\{ \begin{array}{lcl} I_{c1} & = & I_{cd} + I_{S1} \\ I_{c(m-1)} & = & I_{cu} - I_{Sm} \end{array} \right. \tag{6.18}$$

Equations 6.17 and 6.18 indicate that the capacitor voltage balance can be achieved by ensuring the dc components of the (m-2) inner reinjection switch currents, i.e. I_{Sj} ($j = 2, 3, \cdots, (m-1)$) are zero. The dc components of the reinjection switch currents, I_{S1} and I_{Sm} do not affect capacitor voltage balance, but influence the operating behaviour of the converter system. In an ideal 12-pulse case $I_{cd} = I_{cu}$ and thus, from equations 6.18, $I_{S1} = -I_{Sm}$, i.e. switch paths S_1 and S_m act as by pass switches for their dc components.

Capacitor voltage balance can also be assessed with reference to the charge taken away

from the capacitors. Thus the dc components of the $(m-2)$ inner ideal switch currents are proportional to the charges taken away from the $m-2$ inner level nodes every period. If these charges are all zero, the capacitor voltages are kept in balanced conditions.

From equation 6.17 the dc component current differences between the first capacitor (taken as the reference) and other capacitors are given by

$$I_{ci} - I_{c1} = \sum_{j=2}^{i} I_{Sj} \qquad for \quad i = 2, 3, \cdots, (m-1) \tag{6.19}$$

These differences determine the capacitor voltage increment or decrement after every period; thus when imbalance occurs, adjustments can be made to the dc capacitor voltages by regulating the dc components of the (m-2) inner reinjection switch currents. The remaining question is how to make such adjustments.

The m ideal reinjection switches in figure 5.8 are fired on and off periodically and in synchronism with the main bridge switches in the sequence

$$S_m, S_{m-1}, \cdots, S_i, \cdots, S_2, S_1, S_2, \cdots, S_i, \cdots, S_{m-2}, S_{m-1}.$$

Every six terms of this sequence corresponds to a full fundamental cycle. Every switch in each sequence conducts the reinjection current i_j twice, except for S_m and S_1 that conduct only once.

To simplify the explanation the following discussion is made under the condition that the converter system output ac current is symmetrical and perfectly sinusoidal, while θ, the current phase displacement with repect to the converter output ac voltage, and the interface transformer turns ratios (i.e. $k_{Yn} = k_{\Delta n} = k_n$) are kept at nominal values. The results obtained under these ideal conditions will be extended to general conditions later.

Under the ideal conditions, and with the time reference set by equation 6.1, the reinjection current i_j, a periodic waveform at six times the fundamental frequency, is given by

$$i_j(\omega t) = \begin{cases} 2k_n I_A \sin\frac{\pi}{12}\sin(\omega t + \theta + \frac{\pi}{12}) & -\pi/6 < \omega t < 0 \\ -2k_n I_A \sin\frac{\pi}{12}\sin(\omega t + \theta - \frac{\pi}{12}) & 0 < \omega t < \pi/6 \end{cases} \tag{6.20}$$

where $k_n I_A$ is the peak value of the converter ac output line current.

It is obvious that $i_j(-\omega t) = -i_j(\omega t)$ is not satisfied in the interval $-\pi/6 < \omega t < \pi/6$ except when $\theta = \pm 90^o$, i.e. the reinjection current i_j, described by equation 6.20, is not an odd symmetrical function for $\theta \neq \pm 90^o$.

Under the equal synchronous firing control criterion, the reinjection switch S_i $(i = 2, 3, \cdots, (m-1))$ is in ON-state for the intervals $-\beta_i < \omega t < -\beta_{i-1}$ and $\beta_{i-1} < \omega t < \beta_i$ $(\beta_i = \frac{(2i-1)\pi}{12(m-1)})$ to conduct $i_j(\omega t)$. Due to the asymmetrical characteristics of $i_j(\omega t)$, the dc component of the current through S_i $(i = 2, 3, \cdots, (m-1))$ varies with θ.

The dc components of the reinjection switch path currents under equal on-state interval firing control are clearly visible in Figure 6.1, for the case when $\theta = 30^o$. The waveforms shown in this figure are:

a. V_{YY}/U_{dc}, the voltage across the Y/Y connection bridge

b. $V_{Y\Delta}/U_{dc}$, the voltage across the Y/Δ connection bridge

c. $i_j(\omega t)$, the reinjection current

d. i_{S1}, the path current through the ideal switch S_1

e. i_{S2}, the path current through the ideal switch S_2

f. i_{S3}, the path current through the ideal switch S_3

g. i_{S4}, the path current through the ideal switch S_4

h. i_{S5}, the path current through the ideal switch S_5

i. i_{S6}, the path current through the ideal switch S_6

j. i_{S7}, the path current through the ideal switch S_7

k. i_{S8}, the path current through the ideal switch S_8

The characteristics, $i_j(\omega t - \pi/6) = -i_j(\omega t)$, of the reinjection current $i_j(\omega t)$, enable slight variations of the ON state intervals in the regions $-\pi/6 < \omega t < 0$ and $0 < \omega t < \pi/6$ to regulate the dc components of the capacitor currents. The ON state sequence of the reinjection paths must remain in the sequence

$$S_m, S_{m-1}, \cdots, S_i, \cdots, S_2, S_1, S_2, \cdots, S_i, \cdots, S_{m-2}, S_{m-1}$$

to suppress the harmonics, but the equal ON state interval must be modified to ensure that the dc component of the individual reinjection path current is zero.

To achieve this, the first and second ON state intervals of the reinjection switch S_i $(i = 2, 3, \cdots, (m-1))$ in every sequence are adjusted from $[-\beta_i < \omega t < -\beta_{i-1}]$ to $[-\beta_i + \delta_i < \omega t < -\beta_{i-1} + \delta_{i-1}]$ for the first, and from $[\beta_{i-1} < \omega t < \beta_i]$ to $[\beta_{i-1} + \delta_{i-1} < \omega t < \beta_i + \delta_i]$ for the second. Thus the dc component of the current through S_i $(i = 2, 3, \cdots, (m-1))$ is given by

$$\begin{bmatrix} I_{S1} \\ I_{S2} \\ I_{S3} \\ \vdots \\ I_{Si} \\ \vdots \\ I_{S(m-1)} \end{bmatrix} = \frac{3}{\pi} \begin{bmatrix} \int_{-\beta_1+\delta_1}^{\beta_1+\delta_1} i_j(\omega t)d\omega t \\ \int_{-\beta_2+\delta_2}^{\beta_2+\delta_2} i_j(\omega t)d\omega t - \int_{-\beta_1+\delta_1}^{\beta_1+\delta_1} i_j(\omega t)d\omega t \\ \int_{-\beta_3+\delta_3}^{\beta_3+\delta_3} i_j(\omega t)d\omega t - \int_{-\beta_2+\delta_2}^{\beta_2+\delta_2} i_j(\omega t)d\omega t \\ \vdots \qquad\qquad \vdots \\ \int_{-\beta_i+\delta_i}^{\beta_i+\delta_i} i_j(\omega t)d\omega t - \int_{-\beta_{i-1}+\delta_{i-1}}^{\beta_{i-1}+\delta_{i-1}} i_j(\omega t)d\omega t \\ \vdots \qquad\qquad \vdots \\ \int_{-\beta_{m-1}+\delta_{m-1}}^{\beta_{m-1}+\delta_{m-1}} i_j(\omega t)d\omega t - \int_{-\beta_{m-2}+\delta_{m-2}}^{\beta_{m-2}+\delta_{m-2}} i_j(\omega t)d\omega t \end{bmatrix} \tag{6.21}$$

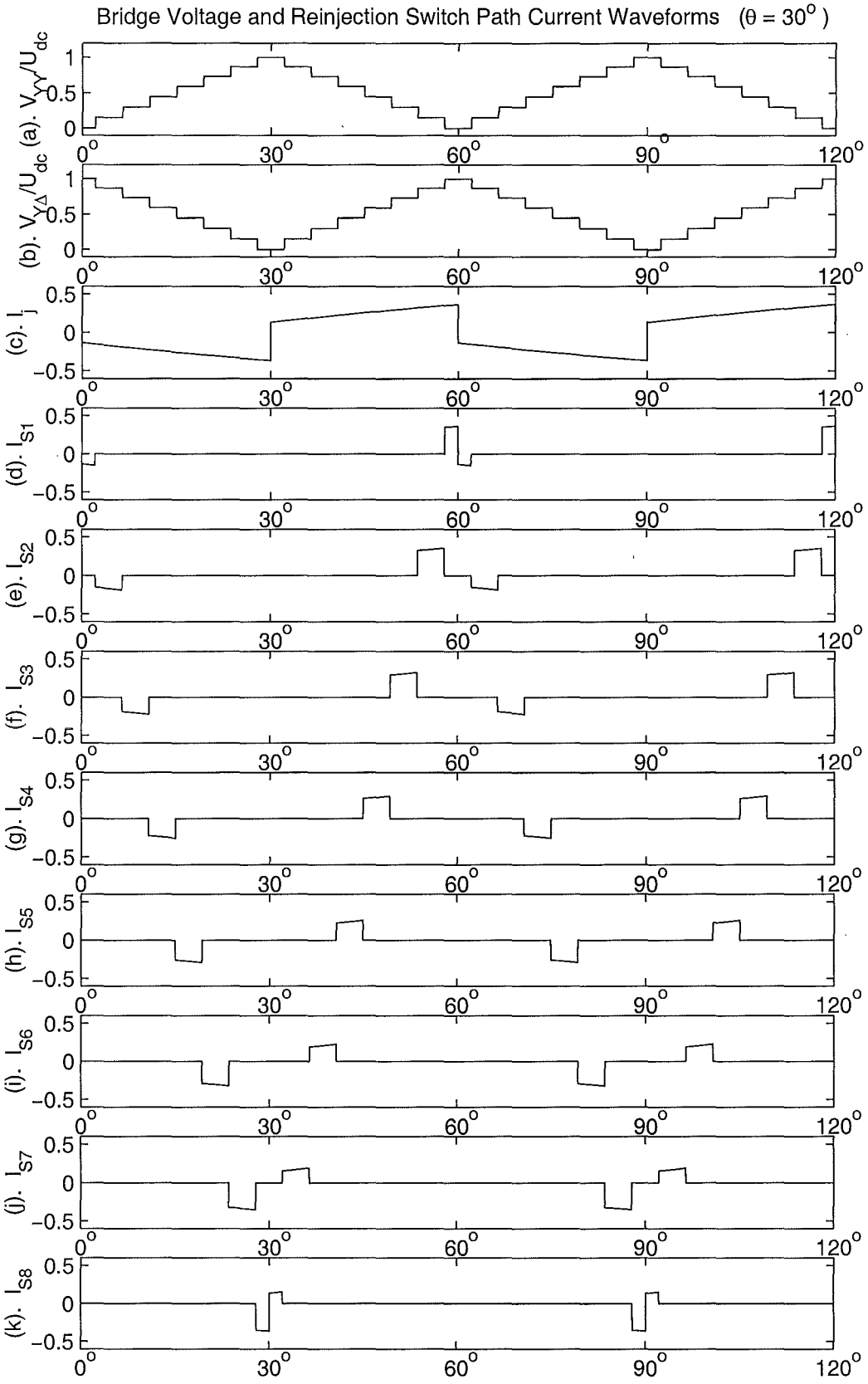


Figure 6.1 The Reinjection Waveforms under equal on-state interval firing

which can be rewritten in the form

$$\begin{bmatrix} I_{S1} \\ I_{S2} \\ I_{S3} \\ \vdots \\ I_{Si} \\ \vdots \\ I_{S(m-1)} \end{bmatrix} = \begin{bmatrix} \frac{3}{\pi}\int_{-\beta_1+\delta_1}^{\beta_1+\delta_1} i_j(\omega t)d\omega t \\ \frac{3}{\pi}\int_{-\beta_2+\delta_2}^{\beta_2+\delta_2} i_j(\omega t)d\omega t - I_{S1} \\ \frac{3}{\pi}\int_{-\beta_3+\delta_3}^{\beta_3+\delta_2} i_j(\omega t)d\omega t - I_{S2} - I_{S1} \\ \vdots \\ \frac{3}{\pi}\int_{-\beta_i+\delta_i}^{\beta_i+\delta_i} i_j(\omega t)d\omega t - I_{S(i-1)} - \cdots - I_{S2} - I_{S1} \\ \vdots \\ \frac{3}{\pi}\int_{-\beta_{m-1}+\delta_{m-1}}^{\beta_{m-1}+\delta_{m-1}} i_j(\omega t)d\omega t - I_{S(m-2)} - \cdots - I_{S2} - I_{S1} \end{bmatrix} \tag{6.22}$$

Using Equation 6.22, and a recurring procedure starting from I_{S1}, determines all of the (m-2) path currents, I_{S2} to $I_{S(m-1)}$.

The integrations (for $i = 1, 2, \cdots, (m-1)$) in equation 6.22 are given by

$$\begin{aligned} \frac{3}{\pi}\int_{-\beta_i+\delta_i}^{\beta_i+\delta_i} i_j(\omega t)d\omega t &= \frac{3}{\pi}\int_{-\beta_i+\delta_i}^{0} i_j(\omega t)d\omega t + \frac{3}{\pi}\int_{0}^{\beta_i+\delta_i} i_j(\omega t)d\omega t \\ &= \frac{12}{\pi}k_n I_A \sin\frac{\pi}{12}[\cos(\theta+\delta_i)\cos(\frac{\pi}{12}-\beta_i) - \cos\theta\cos\frac{\pi}{12}] \end{aligned} \tag{6.23}$$

As indicated earlier, the first and last path currents, I_{S1} and I_{Sm} do not influence the capacitor voltage balance, thus the δ_1 adjustment for regulating I_{S1} can be set freely, and all the other adjustments, δ_2 to $\delta_{(m-1)}$ are used to regulate the capacitor voltages, V_{c2} to $V_{c(m-1)}$, (V_{c1} is treated as the reference).

Equations 6.22 show that $\sum_{j=2}^{i} I_{Sj} = \frac{3}{\pi}\int_{-\beta_i+\delta_i}^{\beta_i+\delta_i} i_j(\omega t)d\omega t - I_{S1}$, and using Equation 6.19 the dc component difference between the i_{th} capacitor current, I_{ci}, and the reference capacitor current, I_{c1}, is given by

$$\begin{aligned} I_{ci} - I_{c1} = \sum_{j=2}^{i} I_{Sj} &= \frac{3}{\pi}\int_{-\beta_i+\delta_i}^{\beta_i+\delta_i} i_j(\omega t)d\omega t - I_{S1} \qquad \text{for } i = 2, 3, \cdots, (m-1) \\ &= \frac{12}{\pi}k_n I_A \sin\frac{\pi}{12}[\cos(\theta+\delta_i)\cos(\frac{\pi}{12}-\beta_i) - \cos(\theta+\delta_1)\cos(\frac{\pi}{12}-\beta_1)] \end{aligned} \tag{6.24}$$

Since the capacitor dc current differences are proportional to the voltage increment differences (after every $\frac{\pi}{3}$ period), equation 6.24 shows that this increment difference can be regulated by the adjustment, δ_i, if δ_1 is fixed. Equation 6.24 also reveals that the converter system power angle θ, has a strong influence on the capacitor voltage balance. If there is no adjustment, i.e. $\delta_1 = \delta_i = 0$, the capacitor current dc component differences can not be zero except for $\theta = \pm 90^o$; this means that without capacitor voltage balance adjustment, as a result of the cumulative effect, the capacitor voltage will drift away from the balanced condition.

Because $\cos(\frac{\pi}{12}-\beta_i) > \cos(\frac{\pi}{12}-\beta_1)$ for $i = 2, 3, \cdots, (m-2)$, the sign of $I_{ci} - I_{c1}$ is determined by $\cos\theta$. Thus for $-90^o < \theta < 90^o$, i.e. the source transfers power to

the converter system, the inner capacitor voltages increase faster or decrease slower than the outer ones; while for $-90^o > \theta > -180^o$ *and* $90^o < \theta < 180^o$, i.e. the source receives power from the converter system, the outer capacitor voltages increase faster or decrease slower than the inner ones. Thus if there is no capacitor voltage balance control, θ governs which capacitor is over rated first, since $\cos(\frac{\pi}{12} - \beta_{(\frac{m}{2})}) > \cos(\frac{\pi}{12} - \beta_{(\frac{m}{2}\pm1)}) > \cos(\frac{\pi}{12} - \beta_{(\frac{m}{2}\pm2)}) > \cdots > \cos(\frac{\pi}{12} - \beta_{(m-2)}) = \cos(\frac{\pi}{12} - \beta_2)$ for m being even, or $\cos(\frac{\pi}{12} - \beta_{(\frac{m-1}{2})}) > \cos(\frac{\pi}{12} - \beta_{(\frac{m-1}{2}\pm1)}) > \cos(\frac{\pi}{12} - \beta_{(\frac{m-1}{2}\pm2)}) > \cdots > \cos(\frac{\pi}{12} - \beta_{(m-2)}) = \cos(\frac{\pi}{12} - \beta_2)$ for m being odd.

Figures 6.4 and 6.5 illustrate the on-state interval adjustments of the reinjection switch paths of the 8-level MLVR-VSC example to cancel the dc components of the reinjection switch path currents for $\theta = 30^o$ and $\theta = -150^o$ respectively. The waveforms in these figures are in the same order as those in Figure 6.1. In Figures 6.4 and 6.5, currents I_{S2} to I_{S7} are regulated to ensure capacitor voltage balance; while I_{S1} and I_{S8} contain dc current components due to lack of adjustment.

6.4 GENERAL CONDITIONS FOR CAPACITOR VOLTAGE BALANCING

To extend the above analysis carried out under ideal conditions, to practical operating conditions, it is convenient to define $-\lambda_i = -\beta_i + \delta_i$ as the first ON interval start instant, and $\gamma_i = \beta_i + \delta_i$ as the second ON interval end instant of the i^{th} switch $(i = 2, 3, \cdots, (m-1))$ in every sequence, with the sequence center used as the reference.

In every sequence the integration of the reinjection current i_j from the first ON state start instant of the i^{th} switch to its second ON state end instant, is the sum of the current integrations of the ideal switch paths $S_1, S_2, \cdots, S_i$. In the presence of asymmetry and distortion, i_j may not be a periodical function of six times the fundamental frequency. Thus the dc components of the reinjection switch current have to be calculated on the full fundamental period. The dc components of the $(m-2)$ ideal switch path currents, I_{S2} to $I_{S(m-1)}$ must be zero to ensure capacitor voltage balance. Thus, $I_{ci} - I_{c1}$, the average current differences derived from the integration of the reinjection current i_j from the first on-state start instant of the i^{th} switch to its second on-state end instant for the six sequences are given by

$$\begin{aligned} I_{ci} - I_{c1} = & \frac{1}{2\pi}\int_{-\lambda_i}^{\gamma_i} i_j(\omega t)d(\omega t) + \frac{1}{2\pi}\int_{\frac{\pi}{3}-\lambda_i}^{\frac{\pi}{3}+\gamma_i} i_j(\omega t)d(\omega t) \\ & + \frac{1}{2\pi}\int_{\frac{2\pi}{3}-\lambda_i}^{\frac{2\pi}{3}+\gamma_i} i_j(\omega t)d(\omega t) + \frac{1}{2\pi}\int_{\pi-\lambda_i}^{\pi+\gamma_i} i_j(\omega t)d(\omega t) \\ & + \frac{1}{2\pi}\int_{\frac{4\pi}{3}-\lambda_i}^{\frac{4\pi}{3}+\gamma_i} i_j(\omega t)d(\omega t) + \frac{1}{2\pi}\int_{\frac{5\pi}{3}-\lambda_i}^{\frac{5\pi}{3}+\gamma_i} i_j(\omega t)d(\omega t) - I_{S1} \end{aligned} \tag{6.25}$$

where I_{S1} can be calculated by

$$
\begin{aligned}
I_{S1} &= \frac{1}{2\pi}\int_{-\lambda_1}^{\gamma_1} i_j(\omega t)d(\omega t) + \frac{1}{2\pi}\int_{\frac{\pi}{3}-\lambda_1}^{\frac{\pi}{3}+\gamma_1} i_j(\omega t)d(\omega t) + \frac{1}{2\pi}\int_{\frac{2\pi}{3}-\lambda_1}^{\frac{2\pi}{3}+\gamma_1} i_j(\omega t)d(\omega t) \\
&+\frac{1}{2\pi}\int_{\pi-\lambda_1}^{\pi+\gamma_1} i_j(\omega t)d(\omega t) + \frac{1}{2\pi}\int_{\frac{4\pi}{3}-\lambda_1}^{\frac{4\pi}{3}+\gamma_1} i_j(\omega t)d(\omega t) + \frac{1}{2\pi}\int_{\frac{5\pi}{3}-\lambda_1}^{\frac{5\pi}{3}+\gamma_1} i_j(\omega t)d(\omega t) \\
&= \frac{1}{2\pi}\int_{-\beta_1}^{\beta_1} i_j(\omega t)d(\omega t) + \frac{1}{2\pi}\int_{\frac{\pi}{3}-\beta_1}^{\frac{\pi}{3}+\beta_1} i_j(\omega t)d(\omega t) + \frac{1}{2\pi}\int_{\frac{2\pi}{3}-\beta_1}^{\frac{2\pi}{3}+\beta_1} i_j(\omega t)d(\omega t) \\
&+\frac{1}{2\pi}\int_{\pi-\beta_1}^{\pi+\beta_1} i_j(\omega t)d(\omega t) + \frac{1}{2\pi}\int_{\frac{4\pi}{3}-\beta_1}^{\frac{4\pi}{3}+\beta_1} i_j(\omega t)d(\omega t) + \frac{1}{2\pi}\int_{\frac{5\pi}{3}-\beta_1}^{\frac{5\pi}{3}+\beta_1} i_j(\omega t)d(\omega t)
\end{aligned}
$$

Under the practical conditions the reinjection current $i_j(\omega t)$ is given by

$$
i_j(\omega t) = \begin{cases}
-k_{\Delta n}\sum_{n=1}^{\infty} I_{Bn}\sin(n\omega t + \frac{n-4}{6}\pi + \theta_{Bn}) - k_{Yn}\sum_{n=1}^{\infty} I_{Cn}\sin(n\omega t + \frac{2}{3}\pi + \theta_{Cn}) & -\frac{\pi}{6} < \omega t < 0 \\
-k_{\Delta n}\sum_{n=1}^{\infty} I_{Bn}\sin(n\omega t + \frac{n-4}{6}\pi + \theta_{Bn}) + k_{Yn}\sum_{n=1}^{\infty} I_{Bn}\sin(n\omega t - \frac{2}{3}\pi + \theta_{Bn}) & 0 < \omega t < \frac{\pi}{6} \\
k_{\Delta n}\sum_{n=1}^{\infty} I_{An}\sin(n\omega t + \frac{n}{6}\pi + \theta_{An}) + k_{Yn}\sum_{n=1}^{\infty} I_{Bn}\sin(n\omega t - \frac{2}{3}\pi + \theta_{Bn}) & \frac{\pi}{6} < \omega t < \frac{\pi}{3} \\
k_{\Delta n}\sum_{n=1}^{\infty} I_{An}\sin(n\omega t + \frac{n}{6}\pi + \theta_{An}) - k_{Yn}\sum_{n=1}^{\infty} I_{An}\sin(n\omega t + \theta_{An}) & \frac{\pi}{3} < \omega t < \frac{\pi}{2} \\
-k_{\Delta n}\sum_{n=1}^{\infty} I_{Cn}\sin(n\omega t + \frac{n+4}{6}\pi + \theta_{Cn}) - k_{Yn}\sum_{n=1}^{\infty} I_{An}\sin(n\omega t + \theta_{An}) & \frac{\pi}{2} < \omega t < \frac{2\pi}{3} \\
-k_{\Delta n}\sum_{n=1}^{\infty} I_{Cn}\sin(n\omega t + \frac{n+4}{6}\pi + \theta_{Cn}) + k_{Yn}\sum_{n=1}^{\infty} I_{Cn}\sin(n\omega t + \frac{2}{3}\pi + \theta_{Cn}) & \frac{2\pi}{3} < \omega t < \frac{5\pi}{6} \\
k_{\Delta n}\sum_{n=1}^{\infty} I_{Bn}\sin(n\omega t + \frac{n-4}{6}\pi + \theta_{Bn}) + k_{Yn}\sum_{n=1}^{\infty} I_{Cn}\sin(n\omega t + \frac{2}{3}\pi + \theta_{Cn}) & \frac{5\pi}{6} < \omega t < \pi \\
k_{\Delta n}\sum_{n=1}^{\infty} I_{Bn}\sin(n\omega t + \frac{n-4}{6}\pi + \theta_{Bn}) - k_{Yn}\sum_{n=1}^{\infty} I_{Bn}\sin(n\omega t - \frac{2}{3}\pi + \theta_{Bn}) & \pi < \omega t < \frac{7\pi}{6} \\
-k_{\Delta n}\sum_{n=1}^{\infty} I_{An}\sin(n\omega t + \frac{n}{6}\pi + \theta_{An}) - k_{Yn}\sum_{n=1}^{\infty} I_{Bn}\sin(n\omega t - \frac{2}{3}\pi + \theta_{Bn}) & \frac{7\pi}{6} < \omega t < \frac{4\pi}{3} \\
-k_{\Delta n}\sum_{n=1}^{\infty} I_{An}\sin(n\omega t + \frac{n}{6}\pi + \theta_{An}) + k_{Yn}\sum_{n=1}^{\infty} I_{An}\sin(n\omega t + \theta_{An}) & \frac{4\pi}{3} < \omega t < \frac{3\pi}{2} \\
k_{\Delta n}\sum_{n=1}^{\infty} I_{Cn}\sin(n\omega t + \frac{n+4}{6}\pi + \theta_{Cn}) + k_{Yn}\sum_{n=1}^{\infty} I_{An}\sin(n\omega t + \theta_{An}) & \frac{3\pi}{2} < \omega t < \frac{5\pi}{3} \\
k_{\Delta n}\sum_{n=1}^{\infty} I_{Cn}\sin(n\omega t + \frac{n+4}{6}\pi + \theta_{Cn}) - k_{Yn}\sum_{n=1}^{\infty} I_{Cn}\sin(n\omega t + \frac{2}{3}\pi + \theta_{Cn}) & \frac{5\pi}{3} < \omega t < \frac{11\pi}{6} \\
-k_{\Delta n}\sum_{n=1}^{\infty} I_{Bn}\sin(n\omega t + \frac{n-4}{6}\pi + \theta_{Bn}) - k_{Yn}\sum_{n=1}^{\infty} I_{Cn}\sin(n\omega t + \frac{2}{3}\pi + \theta_{Cn}) & \frac{11\pi}{6} < \omega t < 2\pi
\end{cases}
\tag{6.26}
$$

Thus the capacitor current differences can be expressed by

$$
\begin{aligned}
I_{ci} - I_{c1} = -I_{S1} + \tfrac{1}{2\pi}\{&-2k_{\Delta n}\textstyle\sum_{n=1}^{\infty}\frac{I_{Bn}[1-(-1)^n]}{n}\sin(\frac{n(\gamma_i+\lambda_i)}{2})\sin[\frac{n(\gamma_i-\lambda_i)}{2} + \frac{(n-4)\pi}{6} + \theta_{Bn}] \\
&+2k_{\Delta n}\textstyle\sum_{n=1}^{\infty}\frac{I_{An}[1-(-1)^n]}{n}\sin\frac{n(\gamma_i+\lambda_i)}{2}\sin[\frac{n(\gamma_i-\lambda_i)}{2} + \frac{n\pi}{2} + \theta_{An}] \\
&-2k_{\Delta n}\textstyle\sum_{n=1}^{\infty}\frac{I_{Cn}[1-(-1)^n]}{n}\sin(\frac{n(\gamma_i+\lambda_i)}{2})\sin[\frac{n(\gamma_i-\lambda_i)}{2} + \frac{(5n+4)\pi}{6} + \theta_{Cn}] \\
&-2k_{Yn}\textstyle\sum_{n=1}^{\infty}\frac{I_{An}[1-(-1)^n]}{n}[\sin(\frac{n\pi}{6})\sin(\frac{n\pi}{2} + \theta_{An}) + \sin(\frac{n(\gamma_i+\lambda_i)}{2} - \frac{n\pi}{6})\sin(\frac{n\pi}{2} + \frac{n(\gamma_i-\lambda_i)}{2} + \theta_{An})] \\
&-2k_{Yn}\textstyle\sum_{n=1}^{\infty}\frac{I_{Bn}[1-(-1)^n]}{n}[\sin(\frac{n\pi}{6})\sin(\frac{(n+2)\pi}{6} + \theta_{Bn}) + \sin(\frac{n(\gamma_i+\lambda_i)}{2} - \frac{n\pi}{6})\sin(\frac{(n+2)\pi}{6} + \frac{n(\gamma_i-\lambda_i)}{2} + \theta_{Bn})] \\
&-2k_{Yn}\textstyle\sum_{n=1}^{\infty}\frac{I_{Cn}[1-(-1)^n]}{n}[\sin(\frac{n\pi}{6})\sin(\frac{(n+2)\pi}{6} - \theta_{Cn}) + \sin(\frac{n(\gamma_i+\lambda_i)}{2} - \frac{n\pi}{6})\sin(\frac{(n+2)\pi}{6} - \frac{n(\gamma_i-\lambda_i)}{2} - \theta_{Cn})]\}
\end{aligned}
$$

Since $\gamma_i + \lambda_i = 2\beta_i$, $\gamma_i - \lambda_i = 2\delta_i$, and the factor $[1-(-1)^n]$ forces the equation above

to be zero when n is an even number, this equation is simplified to

$$\begin{aligned}
I_{ci}-I_{c1} = &-I_{S1}+\tfrac{1}{\pi}\{k_{\Delta n}\textstyle\sum_{n=1}^{\infty}\frac{I_{Bn}[1-(-1)^n]}{n}\sin(n\beta_i)\sin[\frac{(n+2)\pi}{6}+n\delta_i+\theta_{Bn}]\\
&-k_{Yn}\textstyle\sum_{n=1}^{\infty}\frac{I_{An}[1-(-1)^n]}{n}[\sin(\frac{n\pi}{6})\sin(\frac{n\pi}{2}+\theta_{An})+\sin(n\beta_i-\frac{n\pi}{6})\sin(\frac{n\pi}{2}+n\delta_i+\theta_{An})]\\
&-k_{Yn}\textstyle\sum_{n=1}^{\infty}\frac{I_{Bn}[1-(-1)^n]}{n}[\sin(\frac{n\pi}{6})\sin(\frac{(n+2)\pi}{6}+\theta_{Bn})+\sin(n\beta_i-\frac{n\pi}{6})\sin(\frac{(n+2)\pi}{6}+n\delta_i+\theta_{Bn})]\\
&-k_{Yn}\textstyle\sum_{n=1}^{\infty}\frac{I_{Cn}[1-(-1)^n]}{n}[\sin(\frac{n\pi}{6})\sin(\frac{(n+2)\pi}{6}-\theta_{Cn})+\sin(n\beta_i-\frac{n\pi}{6})\sin(\frac{(n+2)\pi}{6}-n\delta_i-\theta_{Cn})]\\
&+k_{\Delta n}\textstyle\sum_{n=1}^{\infty}\frac{I_{An}[1-(-1)^n]}{n}\sin(n\beta_i)\sin[\frac{n\pi}{2}+n\delta_i+\theta_{An}]\\
&+k_{\Delta n}\textstyle\sum_{n=1}^{\infty}\frac{I_{Cn}[1-(-1)^n]}{n}\sin(n\beta_i)\sin[\frac{(n+2)\pi}{6}-n\delta_i-\theta_{Cn}]\}
\end{aligned} \tag{6.27}$$

and

$$\begin{aligned}
I_{S1} = &\tfrac{1}{\pi}\{k_{Yn}\textstyle\sum_{n=1}^{\infty}\frac{I_{An}[1-(-1)^n]}{n}[\sin(\frac{n\pi}{6})\sin(\frac{n\pi}{2}+\theta_{An})+\sin(n\beta_1-\frac{n\pi}{6})\sin(\frac{n\pi}{2}+\theta_{An})]\\
&+k_{Yn}\textstyle\sum_{n=1}^{\infty}\frac{I_{Bn}[1-(-1)^n]}{n}[\sin(\frac{n\pi}{6})\sin(\frac{(n+2)\pi}{6}+\theta_{Bn})+\sin(n\beta_1-\frac{n\pi}{6})\sin(\frac{(n+2)\pi}{6}+\theta_{Bn})]\\
&+k_{Yn}\textstyle\sum_{n=1}^{\infty}\frac{I_{Cn}[1-(-1)^n]}{n}[\sin(\frac{n\pi}{6})\sin(\frac{(n+2)\pi}{6}-\theta_{Cn})+\sin(n\beta_1-\frac{n\pi}{6})\sin(\frac{(n+2)\pi}{6}-\theta_{Cn})]\\
&-k_{\Delta n}\textstyle\sum_{n=1}^{\infty}\frac{I_{Bn}[1-(-1)^n]}{n}\sin(n\beta_1)\sin(\frac{(n+2)\pi}{6}+\theta_{Bn})\\
&-k_{\Delta n}\textstyle\sum_{n=1}^{\infty}\frac{I_{An}[1-(-1)^n]}{n}\sin(n\beta_1)\sin(\frac{n\pi}{2}+\theta_{An})\\
&-k_{\Delta n}\textstyle\sum_{n=1}^{\infty}\frac{I_{Cn}[1-(-1)^n]}{n}\sin(n\beta_1)\sin(\frac{(n+2)\pi}{6}-\theta_{Cn})\}
\end{aligned} \tag{6.28}$$

6.5 BASIC REQUIREMENTS OF CAPACITOR VOLTAGE BALANCE

In the MLVR-VSC system the current and voltage waveforms have very low harmonic content and the source voltage is usually symmetrical. Therefore to simplify the development of the basic requirements for capacitor voltage balancing, the analysis is carried out under the ideal conditions that the converter system output currents are symmetrical and undistorted (i.e. $I_{A1}=I_{B1}=I_{C1}$, $\theta_{A1}=\theta_{B1}=\theta_{C1}=\theta$ and $I_{An}=I_{Bn}=I_{Cn}=0$), and the two interface transformer turns ratios $k_{Yn}=k_{\Delta n}=k_n$. Under these conditions Equations 6.27 and 6.28 become

$$I_{ci}-I_{c1}=\frac{12}{\pi}k_nI_{A1}[-\frac{1}{4}\cos(\theta)+\sin(\frac{\pi}{12})\cos(\delta_i+\theta)\cos(\beta_i-\frac{\pi}{12})]-I_{S1}$$

$$I_{S1}=\frac{12}{\pi}k_nI_{A1}[-\frac{1}{4}\cos(\theta)+\sin(\frac{\pi}{12})\cos(\delta_1+\theta)\cos(\beta_1-\frac{\pi}{12})]$$

Thus the capacitor dc current differences (for $i=2,3,\cdots,(m-1)$) can be obtained and as the same as equation 6.24, i.e.

$$I_{ci}-I_{c1}=\frac{12}{\pi}k_nI_{A1}\sin(\frac{\pi}{12})[\cos(\delta_i+\theta)\cos(\beta_i-\frac{\pi}{12})-\cos(\delta_1+\theta)\cos(\beta_1-\frac{\pi}{12})] \tag{6.29}$$

From equation 6.29 the following basic requirements for the capacitor voltage balance can be deduced:

1. The dc current differences between the capacitors, $I_{ci}-I_{c1}$ (and thus the capacitor voltage increments or decrements after every cycle), can be controlled by the reinjection switch firing adjustment, δ_i $(i = 2, 3, \cdots, (m-1))$. The regulation is strongly influenced by θ, the phase displacement between the converter system output current and voltage. For example, in the region of $-90^o < \theta < 90^o$, the increment of δ_i will cause the i^{th} capacitor voltage to decrease, but for the regions of $-90^o > \theta > -180^o$ and $90^o < \theta < 180^o$, the increment of δ_i will cause the reverse results.

2. To keep the firing synchronization between the main bridge and reinjection switches, and allow sufficient time for the main bridge valves to switch under the zero voltage, the adjustments δ_1 and $\delta_{(m-1)}$ should be set to 0. Thus to maintain the sequence order, adjustments, δ_2 to $\delta_{(m-2)}$ have to be in the following range:

$$\begin{cases} -\frac{\pi}{6(m-1)} < \delta_2 < \frac{\pi}{6(m-1)}, \\ -\frac{\pi}{6(m-1)} - \delta_2 < \delta_3 < \frac{\pi}{6(m-1)} + \delta_2, \\ \quad\vdots \qquad\quad \vdots \qquad\quad \vdots \\ -\frac{\pi}{6(m-1)} - \delta_2 - \delta_3 - \cdots - \delta_{(m-3)} < \delta_{(m-2)} < \frac{\pi}{6(m-1)} + \delta_2 + \delta_3 + \cdots + \delta_{(m-3)}. \end{cases} \tag{6.30}$$

3. Under the limitation imposed by equation 6.30, the capacitor balance can only be achieved if θ is within the region

$$\frac{11\pi}{12} + \frac{\pi}{4(m-1)} > |\theta| > \frac{\pi}{12} - \frac{\pi}{4(m-1)} \tag{6.31}$$

   To keep the unbalance within the specified tolerance, the maximum number of cycles in which θ remains out of this region has to be limited and this is dependent on the capacitance of the dc capacitors.

4. When θ is within the region in steady state and $\delta_1 = 0$, to keep the capacitor voltage balance the adjustments must satisfied the expression

$$\cos(\theta + \delta_i) = \frac{\cos(\theta + \delta_1)\cos(\frac{\pi}{12} - \beta_1)}{\cos(\frac{\pi}{12} - \beta_i)} = \frac{\cos\theta\cos(\beta_1 - \frac{\pi}{12})}{\cos(\beta_i - \frac{\pi}{12})} \tag{6.32}$$

Figures 6.2 and 6.3 illustrate the main bridge and the reinjection switch firing sequence, the on-state combinations and the firing adjustments of the reinjection switch paths required for capacitor voltage balance.

In Figures 6.2 and 6.3 the three concentric annuluses represent the on-state combinations of the three groups of switches. The center one is divided into six sectors to express the six on-state combinations of S_{Y1} to S_{Y6}, the six valves of the main bridge connected to the Y/Y connection transformer; the middle annulus is also divided into six sectors to express the six on-state combinations of $S_{\Delta 1}$ to $S_{\Delta 6}$, the six switches of

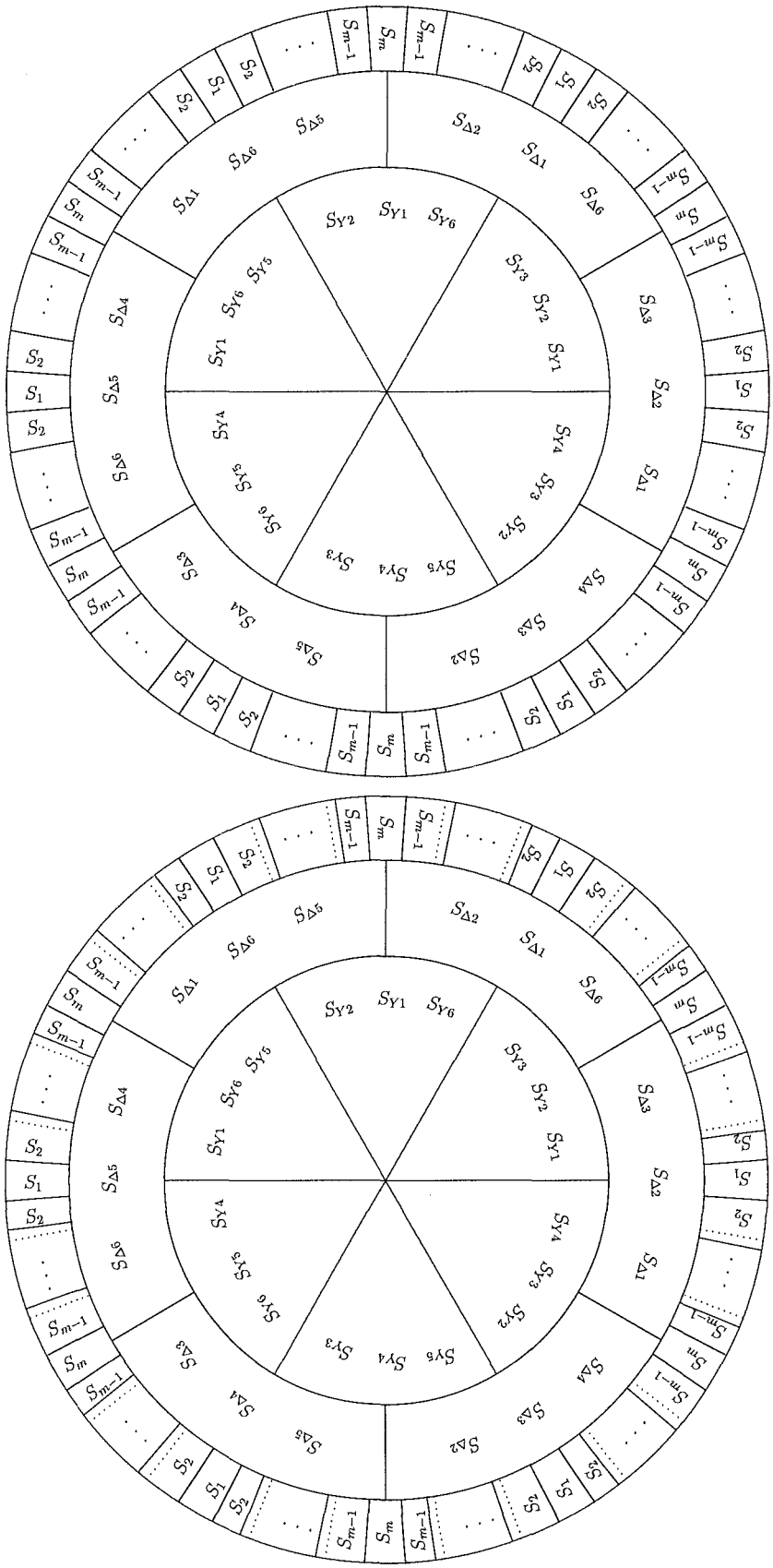


Figure 6.2 Firing sequence of the MLVR-VSC

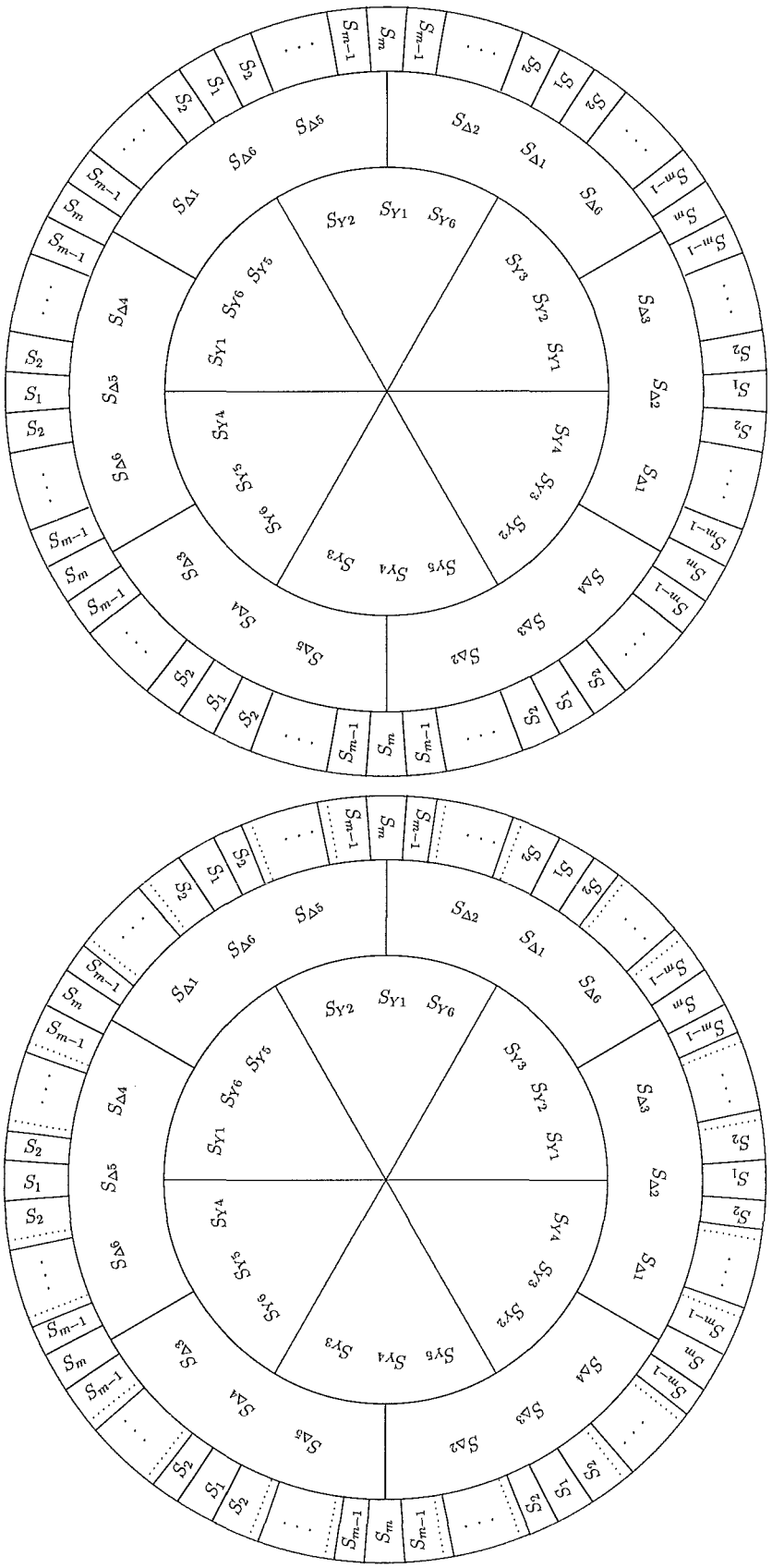


Figure 6.3 Firing sequence of the MLVR-VSC

the main bridge connected to the Y/Δ connection transformer; the third one is divided into $12(m-1)$ sectors, and every $2(m-1)$ sectors forms a group, that corresponds to an on-state sequence of the reinjection switches. The on-state combinations denoted on the three concentric annuluses rotate in the clockwise direction corresponding to the switch state changes in the time domain; at any instant, i.e. at any angle position, the on-state combinations of the three switch groups can be determined by the switches that appear in the appropriate area where the angle is located, otherwise the switches are in the off-state.

In Figures 6.2 and 6.3, the top graphs show the on-state combination features for $\theta = 90^o$ and $\theta = -90^o$ respectively, while the lower graphs show the effects of operating outside the $\theta = \pm 90^o$ regions, (the lower graph in Figure 6.2 with adjustments for $-90^o < \theta < -15^o$ and $15^o < \theta < 90^o$; the lower graph in Figure 6.3 with adjustments for $-90^o > \theta > -165^o$ and $165^o > \theta > 90^o$). Under those conditions the reinjection switch on-states are shifted except switch paths S_1 and S_m; for example, the on-state interval of the switches S_2 and S_{m-1} are shifted from the dash lines to their nearest solid lines. The on-state adjustments of the switches S_3 to S_{m-2} are not shown in the figures.

Figures 6.4 and 6.5 show the on-state interval adjustments of the reinjection switch paths of an eight level example for the cases of $\theta = 30^o$ and $\theta = -150^o$ respectively. The dc components of the reinjection switch path currents are regulated to zero by the adjustments. The waveforms in Figures 6.4 and 6.5 are in the same order as in Figure 6.1. Currents I_{S2} to I_{S7} are regulated in different lengths for the two adjacent on-state intervals to achieve the zero dc average; while I_{S1} and I_{S8} are set with no adjustments, i.e. they contain dc current components.

6.6 ASYMMETRICAL CURRENT INFLUENCE

By using precise on-state time sequence control of the reinjection switch paths and the main bridge switches, the converter system three phase output voltage waveforms can be made symmetrical. The source voltage on the other hand can be asymmetrical for a variety of uncontrollable reasons. The following analysis is made under the assumption that the source voltage, although asymmetrical, is perfectly sinusoidal, the converter system output current harmonic components are ignored (i.e. $I_{An} = I_{Bn} = I_{Cn} = 0 \quad n = 2, 3, \cdots$), and the two interface transformer turns ratios are $k_n : 1$ and $k_n : \sqrt{3}$ for Y/Y and Y/Δ connections (i.e. $k_{Yn} = k_{\Delta n} = k_n$). Equations 6.27 and 6.28 then

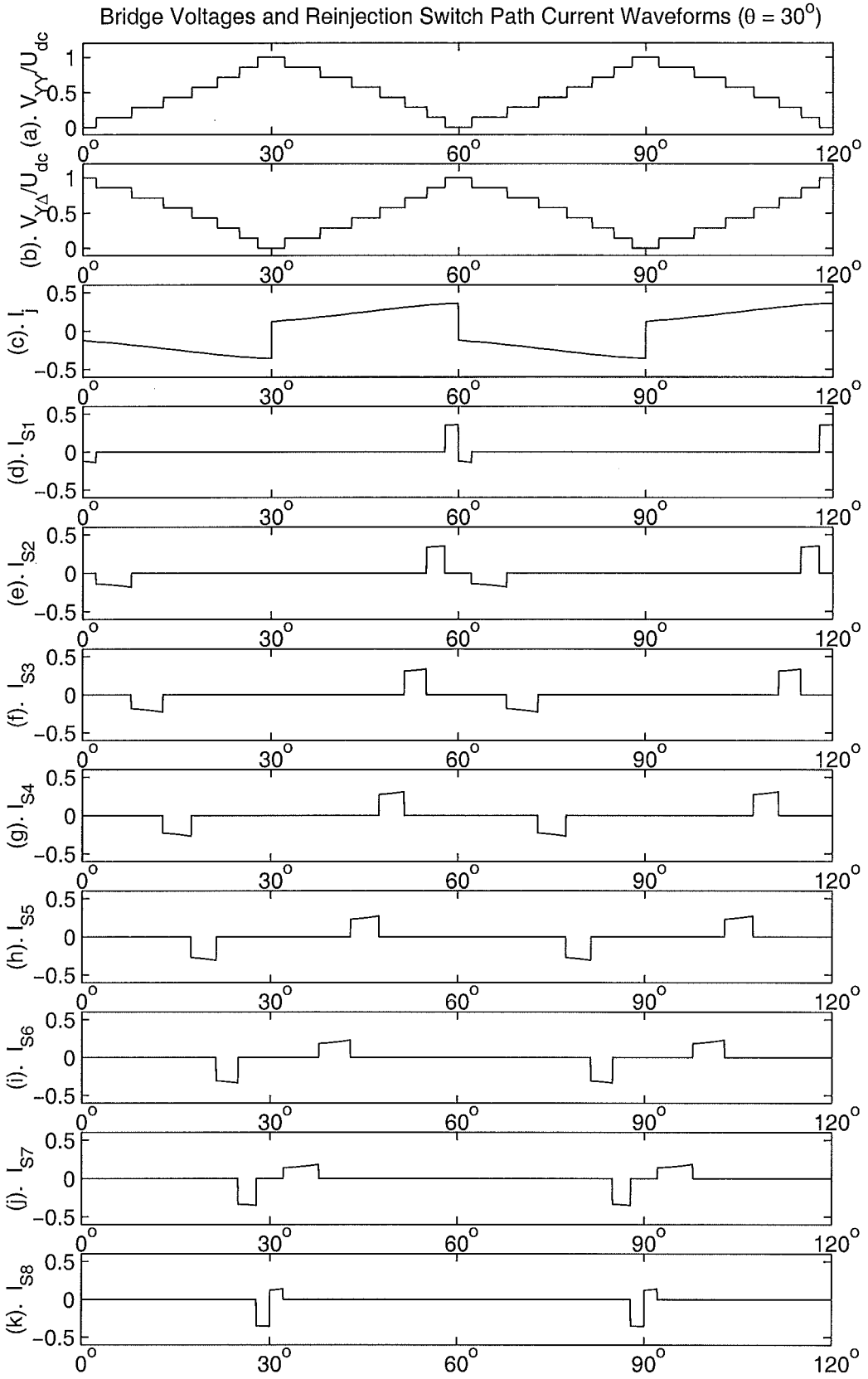


Figure 6.4 The Reinjection Waveforms under capacitor voltage balance control

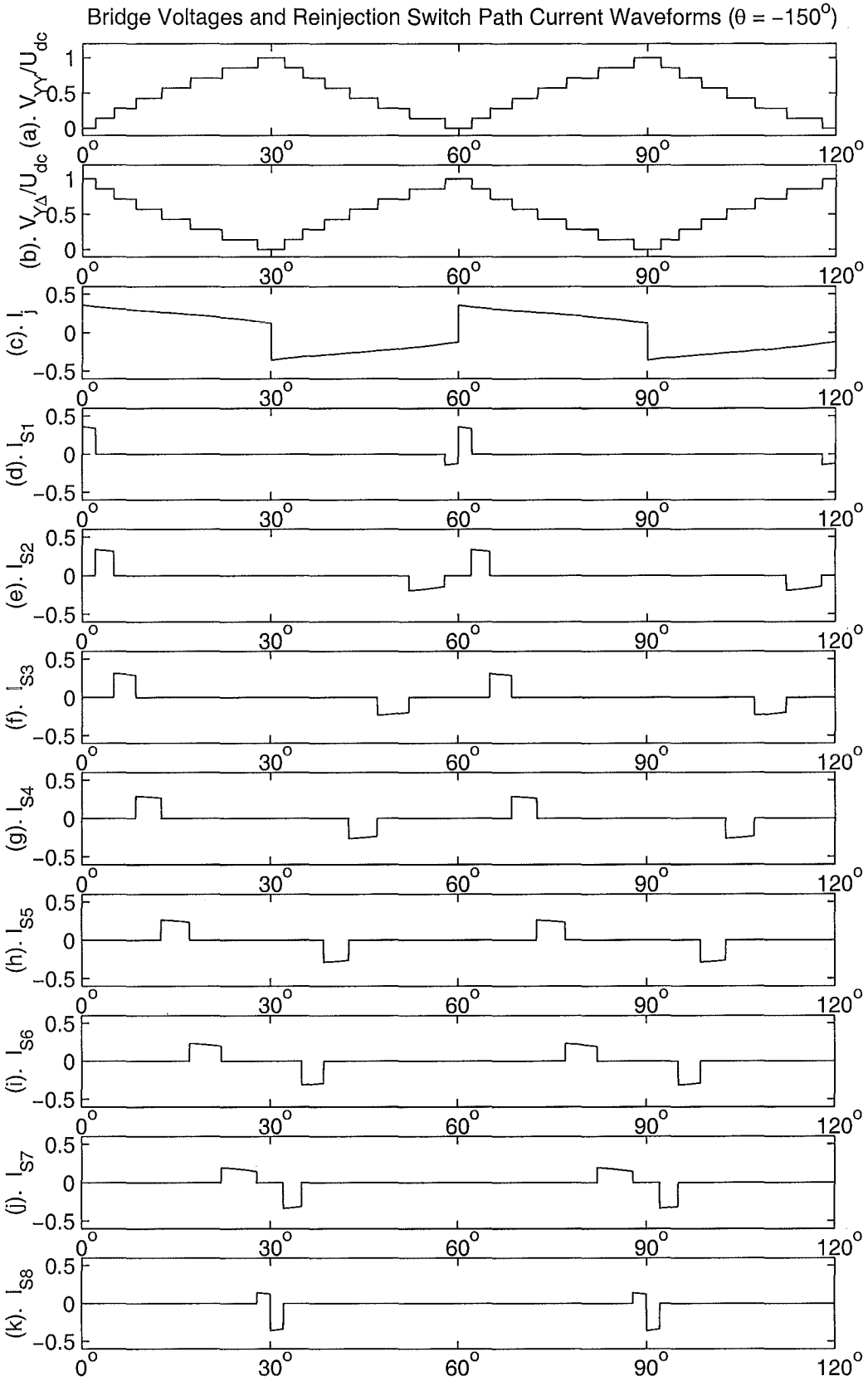


Figure 6.5 The Reinjection Waveforms under capacitor voltage balance control

become

$$\begin{aligned} I_{ci} - I_{c1} = \frac{k_n}{\pi}\{&I_{A1}[-\cos(\theta_{A1}) + 4\sin(\frac{\pi}{12})\cos(\delta_i + \theta_{A1})\cos(\beta_i - \frac{\pi}{12})] \\ &+I_{B1}[-\cos(\theta_{B1}) + 4\sin(\frac{\pi}{12})\cos(\delta_i + \theta_{B1})\cos(\beta_i - \frac{\pi}{12})] \\ &+I_{C1}[-\cos(\theta_{C1}) + 4\sin(\frac{\pi}{12})\cos(\delta_i + \theta_{C1})\cos(\beta_i - \frac{\pi}{12})]\} - I_{S1} \end{aligned}$$

$$\begin{aligned} I_{S1} = \frac{k_n}{\pi}\{&I_{A1}[-\cos(\theta_{A1}) + 4\sin(\frac{\pi}{12})\cos(\delta_1 + \theta_{A1})\cos(\beta_1 - \frac{\pi}{12})] \\ &+I_{B1}[-\cos(\theta_{B1}) + 4\sin(\frac{\pi}{12})\cos(\delta_1 + \theta_{B1})\cos(\beta_1 - \frac{\pi}{12})] \\ &+I_{C1}[-\cos(\theta_{C1}) + 4\sin(\frac{\pi}{12})\cos(\delta_1 + \theta_{C1})\cos(\beta_1 - \frac{\pi}{12})]\} \end{aligned}$$

Then under the condition specified above, the dc current differences of the reinjection switches are given by

$$\begin{aligned} I_{ci} - I_{c1} = \tfrac{4k_n}{\pi}\sin(\tfrac{\pi}{12})\{&I_{A1}[\cos(\delta_i + \theta_{A1})\cos(\beta_i - \tfrac{\pi}{12}) - \cos(\delta_1 + \theta_{A1})\cos(\beta_1 - \tfrac{\pi}{12})] \\ &+I_{B1}[\cos(\delta_i + \theta_{B1})\cos(\beta_i - \tfrac{\pi}{12}) - \cos(\delta_1 + \theta_{B1})\cos(\beta_1 - \tfrac{\pi}{12})] \\ &+I_{C1}[\cos(\delta_i + \theta_{C1})\cos(\beta_i - \tfrac{\pi}{12}) - \cos(\delta_i + \theta_{C1})\cos(\beta_i - \tfrac{\pi}{12})]\} \end{aligned} \tag{6.33}$$

To ensure capacitor voltage balance, with the equal on-state time for every reinjection switch path set as the base criterion, the m ideal switch path on-state intervals are shifted by angles, δ_i $(i = 2, 3, \cdots, m-1)$. If the ON interval middle of the switch path S_1 is used as the reference, the first on-state starting instant of the i^{th} switch path is delayed from $-\frac{(2i-1)\pi}{12(m-1)}$ to $-\frac{(2i-1)\pi}{12(m-1)} + \delta_i$, and its second on-state finishing point prolonged from $\frac{(2i-1)\pi}{12(m-1)}$ to $\frac{(2i-1)\pi}{12(m-1)} + \delta_i$. Thus for $I_{ci} - I_{c1} = 0$ Equation 6.33 becomes

$$\begin{aligned} &\cos(\frac{\pi}{12} - \beta_1)[I_{A1}\cos(\theta_{A1} + \delta_1) + I_{B1}\cos(\theta_{B1} + \delta_1) + I_{C1}\cos(\theta_{C1} + \delta_1)] \\ &= \cos(\frac{\pi}{12} - \beta_i)[I_{A1}\cos(\delta_i + \theta_{A1}) + I_{B1}\cos(\delta_i + \theta_{B1}) + I_{C1}\cos(\delta_i + \theta_{C1})] \end{aligned} \tag{6.34}$$

or for $\delta_1 = \delta_{m-1} = 0$

$$\begin{aligned} &\cos(\tfrac{\pi}{12} - \beta_i)[I_{A1}\cos(\delta_i + \theta_{A1}) + I_{B1}\cos(\delta_i + \theta_{B1}) + I_{C1}\cos(\delta_i + \theta_{C1})] \\ &= \cos(\tfrac{\pi}{12} - \beta_1)[I_{A1}\cos(\theta_{A1}) + I_{B1}\cos(\theta_{B1}) + I_{C1}\cos(\theta_{C1})] \end{aligned} \tag{6.35}$$

Equation 6.35 gives the on-state adjustments δ_i $(i = 2, 3, \cdots, m-1)$ of the reinjection switch paths required to maintain capacitor voltage balance when the converter system output current is asymmetrical.

As described in the previous section (equation 6.30) to maintain the firing sequence

the following restrictions apply to the adjustments:

$$\begin{cases} -\frac{\pi}{6(m-1)} < \delta_2 < \frac{\pi}{6(m-1)}, \\ -\frac{\pi}{6(m-1)} - \delta_2 < \delta_3 < \frac{\pi}{6(m-1)} + \delta_2, \\ \quad \vdots \qquad \vdots \qquad \vdots \\ -\frac{\pi}{6(m-1)} - \delta_2 - \delta_3 - \cdots - \delta_{(m-3)} < \delta_{(m-2)} < \frac{\pi}{6(m-1)} + \delta_2 + \delta_3 + \cdots + \delta_{(m-3)} \end{cases} \tag{6.36}$$

It is clear that under asymmetrical output current operation the adjustments described by equations 6.34 and 6.35 can maintain the capacitor voltages balanced, not at every one sixth period but for the full cycle period of the source fundamental; therefore the capacitor voltages will fluctuate more than in the case of symmetrical operation.

6.7 HARMONIC CURRENTS INFLUENCE

As the output voltage of the reinjection converter is a high pulse waveform, the resulting output current harmonic components will be very small. In practice however the source voltage may be distorted, and therefore the MLVR-VSC output current harmonic components are caused partly by the distorted source voltage. The following analysis is carried out under the condition that the converter system output current includes symmetrical harmonics caused by a distorted voltage source and the converter system output voltage. Under such conditions $\theta_{An} = \theta_{Bn} = \theta_{Cn} = \theta_n$, $I_{An} = I_{Bn} = I_{Cn}$ $(n = 1, 2, 3, \cdots)$ and $k_{Yn} = k_{\Delta n} = k_n$, Equations 6.27 and 6.28 then become

$$\begin{aligned} I_{ci} - I_{c1} = \frac{k_n}{\pi} \sum_{n=1}^{\infty} \frac{I_{An}[1-(-1)^n]}{n} \Big\{ & [\sin(\frac{n\pi}{2} + n\delta_i + \theta_n) + \sin(\frac{n+2}{6}\pi + n\delta_i + \theta_n) \\ & + \sin(\frac{n+2}{6}\pi - n\delta_i - \theta_n)][\sin(n\beta_i) - \sin(n\beta_i - \frac{n\pi}{6})] \\ & - \sin(\frac{n\pi}{6})[\sin(\frac{n\pi}{2} + \theta_n) + \sin(\frac{n+2}{6}\pi + \theta_n) + \sin(\frac{n+2}{6}\pi - \theta_n)] \Big\} - I_{S1} \end{aligned}$$

$$\begin{aligned} I_{S1} = \frac{k_n}{\pi} \sum_{n=1}^{\infty} \frac{I_{An}[1-(-1)^n]}{n} \{ & [\sin(\frac{n\pi}{2} + n\delta_1 + \theta_n) + \sin(\frac{n+2}{6}\pi + n\delta_1 + \theta_n) \\ & + \sin(\frac{n+2}{6}\pi - n\delta_1 - \theta_n)][\sin n\beta_1 - \sin(n\beta_1 - \frac{n\pi}{6})] \\ & - \sin(\frac{n\pi}{6})[\sin(\frac{n\pi}{2} + \theta_n) + \sin(\frac{n+2}{6}\pi + \theta_n) + \sin(\frac{n+2}{6}\pi - \theta_n)] \} \end{aligned}$$

Under the above conditions, the dc current differences of the reinjection switch paths are given by

$$I_{ci}-I_{c1}=\frac{2k_n}{\pi}\sum_{n=1}^{\infty}\frac{I_{An}[1-(-1)^n]}{n}\sin(\frac{n\pi}{12})\Big[\sin\frac{n\pi}{2}+2\sin(\frac{(n+2)\pi}{6})\Big]$$
$$\times\Big[\cos(n\delta_i+\theta_n)\cos(n\beta_i-\frac{n\pi}{12})-\cos(n\delta_1+\theta_n)\cos(n\beta_1-\frac{n\pi}{12})\Big] \quad (6.37)$$

Because the factor $[1-(-1)^n]$ is equal to zero when $n=2k$ $(k=1,2,\cdots)$ and the factor $(\sin(\frac{n\pi}{2})+2\sin(\frac{(n+2)\pi}{6}))$ is equal to zero when $n=3(2k-1)$ or $n=6k-1$ $(k=1,2,\cdots)$ only harmonic of orders $6k+1$, $(k=1,2,\cdots)$ influence the capacitor current dc component difference, which is given by

$$I_{ci}-I_{c1}=\frac{12k_n}{\pi}\sum_{k=1}^{\infty}\frac{(-1)^kI_{A(6k+1)}}{6k+1}\sin(\frac{(6k+1)\pi}{12})\Big\{$$
$$\cos[(6k+1)\delta_i+\theta_{(6k+1)}]\times\cos[(6k+1)\beta_i-\frac{(6k+1)\pi}{12}]$$
$$-\cos[(6k+1)\delta_1+\theta_{(6k+1)}]\cos[(6k+1)\beta_1-\frac{(6k+1)\pi}{12}]\Big\} \quad (6.38)$$

With an ideal sinusoidal source voltage, the converter output current harmonics are caused only by the converter output voltage harmonics. Therefore the output current only contains the harmonics of orders $12k\pm1$ $(k=1,2,\cdots)$, and the harmonic component phase angles are all 90^o, i.e. $\theta_{12k\pm1}=90^o$ $(k=1,2,\cdots)$; thus the capacitor current dc component differences become

$$I_{ci}-I_{c1}=\frac{12k_n}{\pi}\sum_{k=1}^{\infty}\frac{I_{A(12k+1)}}{12k+1}\sin(\frac{\pi}{12})\Big\{$$
$$\cos[(12k+1)\delta_i+\theta_{(12k+1)}]\times\cos[(12k+1)\beta_i-\frac{\pi}{12}]$$
$$-\cos[(12k+1)\delta_1+\theta_{(12k+1)}]\cos[(12k+1)\beta_1-\frac{\pi}{12})]\Big\} \quad (6.39)$$
$$=\frac{12k_n}{\pi}\sum_{k=1}^{\infty}\frac{I_{A(12k+1)}}{12k+1}\sin\frac{\pi}{12}\Big\{-\sin[(12k+1)\delta_i]\times\cos[(12k+1)\beta_i-\frac{\pi}{12}]$$
$$+\sin[(12k+1)\delta_1]\cos[(12k+1)\beta_1-\frac{\pi}{12})]\Big\} \quad (6.40)$$

Equation 6.40 indicates that the current harmonics caused by the converter output voltage harmonics do not influence the capacitor voltage balance, because $I_{ci}-I_{c1}=0$, if $\delta_i=0$ $(i=1,\ 2,\ \cdots\ m)$. Thus there is no need for adjustments to cancel the effects caused by the converter voltage harmonics.

Therefore only the current harmonics caused by the distorted source voltage will influence capacitor voltage balance; equation 6.38 indicates that capacitor voltage balance can be achieved by appropriate on-state interval adjustments. For example, with refer-

ence to a current harmonic of order 7 (for $k = 1$) caused by a source voltage harmonic of order 7, when the adjustments δ_i $(i = 2, 3, \cdots, m-1)$ satisfy the equation
$\cos(7\delta_i + \theta_7) \times \sin(\frac{\pi}{12} - 7\beta_i) = \cos(\theta_7)\cos(\frac{\pi}{12} - \beta_1)$
the effects of the 7^{th} harmonic on capacitor voltage balance is eliminated.

6.8 TURNS RATIO ERROR INFLUENCE

Although the nominal turns ratios of the two interface transformers are $(k_{Yn} : 1)$ and $(k_{\Delta n} : \sqrt{3})$, in practice there are always small differences as the turns ratios can only be rational numbers. Let us consider the case where $k_{Yn} = k_n + k_e$, and $k_{\Delta n} = k_n - k_e$, where $k_n = (k_{Yn} + k_{\Delta n})/2$, and k_e is the error from the theoretical required value.

In practice the two interface transformer turns ratios are arranged as close to the theoretical value as possible to prevent unequal voltage and current rating for the two bridge valves and the interface transformer windings. Thus $|k_e/k_n|$ is reasonably small.

To simplify the analysis the converter output current fundamental components are assumed symmetrical (i.e. $I_{A1} = I_{B1} = I_{C1}$, $\theta_{A1} = \theta_{B1} = \theta_{C1} = \theta$), and their harmonics are ignored (i.e. $I_{An} = I_{Bn} = I_{Cn} = 0 \quad for \quad n = 2, 3, \cdots$). The 30^o delay firing relationship between the Y/Δ and Y/Y connection bridges is now adjusted to $30^o + \delta_e$ to make the two main bridge dc output currents equal ($I_{Ydc} = k_{Yn} I_{A1}\cos(\theta + \delta_e)$ and $I_{\Delta dc} = k_{\Delta n} I_{A1}\cos(\theta)$ being the dc components of Y/Y and Y/Δ bridge dc output currents respectively).

Under these conditions with the time reference set by equation 6.1, the Y/Y and Y/Δ connected bridge dc side currents i_{Ydc} and $i_{\Delta dc}$ are given by

$$i_{Ydc} = \begin{cases} k_{Yn} I_{A1}\cos(\omega t + \theta + \frac{\pi}{6}) & -\frac{\pi}{3} < \omega t < \delta_e \\ k_{Yn} I_{A1}\cos(\omega t + \theta - \frac{\pi}{6}) & \delta_e < \omega t < \frac{\pi}{3} \end{cases}$$

$$i_{\Delta dc} = k_{\Delta n} I_{A1}\cos(\omega t + \theta) \qquad -\frac{\pi}{6} < \omega t < \frac{\pi}{6}$$

Then the reinjection current $i_j = i_{\Delta dc} - i_{Ydc}$ is given by

$$i_j(\omega t) = \begin{cases} I_{A1}[k_{\Delta n}\cos(\omega t + \theta) - k_{Yn}\cos(\omega t + \theta + \frac{\pi}{6})] & -\frac{\pi}{6} < \omega t < \delta_e \\ I_{A1}[k_{\Delta n}\cos(\omega t + \theta) - k_{Yn}\cos(\omega t + \theta - \frac{\pi}{6})] & \delta_e < \omega t < \frac{\pi}{6} \end{cases} \tag{6.41}$$

Based on equation 6.24, the dc component differences of the $(m-1)$ capacitor currents

are given by

$$\begin{aligned} I_{ci} - I_{c1} &= \frac{3}{\pi}\int_{-\beta_i+\delta_i}^{\beta_i+\delta_i} i_j(\omega t)d\omega t - I_{S1} \\ &= \frac{3}{\pi}\left[\int_{-\beta_i+\delta_i}^{-\beta_1+\delta_1} i_j(\omega t)d\omega t + \int_{\beta_1+\delta_1}^{\beta_i+\delta_i} i_j(\omega t)d\omega t\right] \\ &= \frac{6I_{A1}}{\pi}\Big\{k_{\Delta n}[\cos(\theta+\delta_i)\sin\beta_i - \cos(\theta+\delta_1)\sin\beta_1] \\ &\quad -k_{Yn}[\cos(\theta+\delta_1)\sin(\frac{\pi}{6}-\beta_1) - \cos(\theta+\delta_i)\sin(\frac{\pi}{6}-\beta_i)]\Big\} \\ &\qquad\qquad \text{for } i = 2, 3, \cdots, (m-1) \end{aligned} \tag{6.42}$$

Equation 6.42 reveals that

1. the main bridge firing adjustment (δ_e) does not influence the dc capacitor voltage balance;

2. by adjusting the reinjection switch path on-state intervals, the capacitor voltage can be regulated;

3. to ensure that the voltage across the highest capacitor is equal to the voltage across the lowest capacitor, in steady state, the balance condition, $I_{c(m-1)} - I_{c1} = 0$, must be satisfied, i.e.

   $k_{\Delta n}[\cos(\theta+\delta_{(m-1)})\sin(\beta_{(m-1)}) - \cos(\theta+\delta_1)\sin(\beta_1)]$
   $= k_{Yn}[\cos(\theta+\delta_1)\sin(\beta_{(m-1)}) - \cos(\theta+\delta_{(m-1)})\sin(\beta_1)]$ or

   $\frac{k_e}{k_n}[\sin(\beta_{(m-1)}) - \sin(\beta_1)][\cos(\theta+\delta_{(m-1)}) + \cos(\theta+\delta_1)]$
   $= [\sin(\beta_{(m-1)}) + \sin(\beta_1)][\cos(\theta+\delta_{(m-1)}) - \cos(\theta+\delta_1)]$

   because $|\delta_1| < \beta_1$, $|\delta_{(m-1)}| < \beta_1$ ($\beta_1 = \frac{\pi}{12(m-1)}$) and $\beta_{(m-1)} = (2m-3)\beta_1$, the turns ratio differences from the theoretical requirement must be limited within the range

   $$|k_e/k_n| < \frac{[\sin\beta_{(m-1)}+\sin\beta_1]\sin\theta\sin\beta_1}{[\sin\beta_{(m-1)}-\sin\beta_1]\cos\theta\cos\beta_1}$$

   for the capacitor voltage balance control to be effective.

For turns ratios deviating from the theoretical requirement, the on-state interval adjustments for the reinjection switch paths S_1 and S_m are different (i.e. $\delta_1 \neq \delta_{m-1}$). To provide sufficient zero voltage duration for the main bridge valves to ensure switching in the period, the adjustments, δ_1 and δ_{m-1} ought to have the relation $\delta_1 = -\delta_{m-1}$.

6.9 WAVEFORM DISTORTION BY CAPACITOR VOLTAGE BALANCING

The reinjection switch path on-state interval adjustments used to balance the capacitor voltages change the voltage waveforms across the two main bridges and thus the

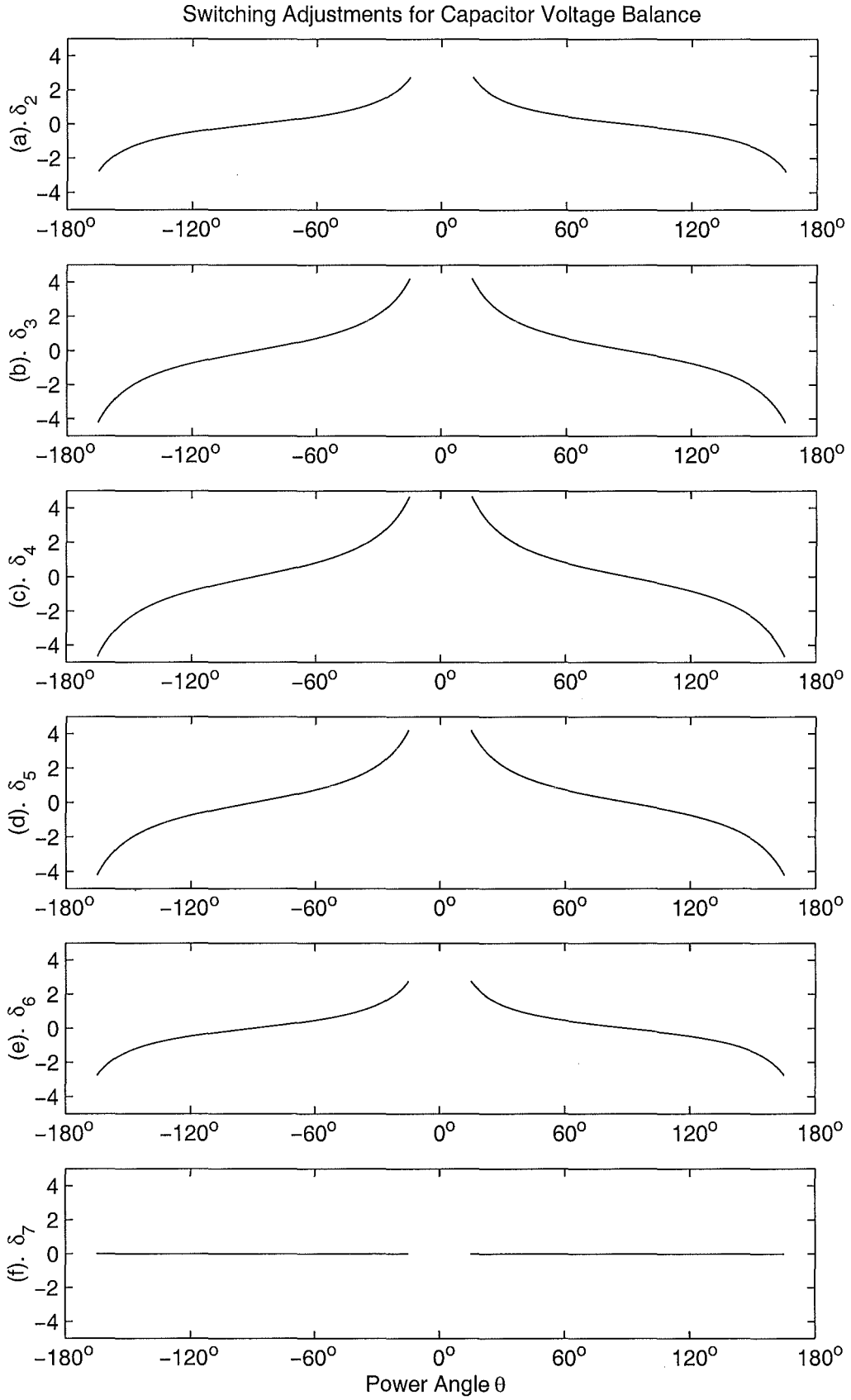


Figure 6.6 The ON-state Interval Adjustments for Capacitor Voltage Balance

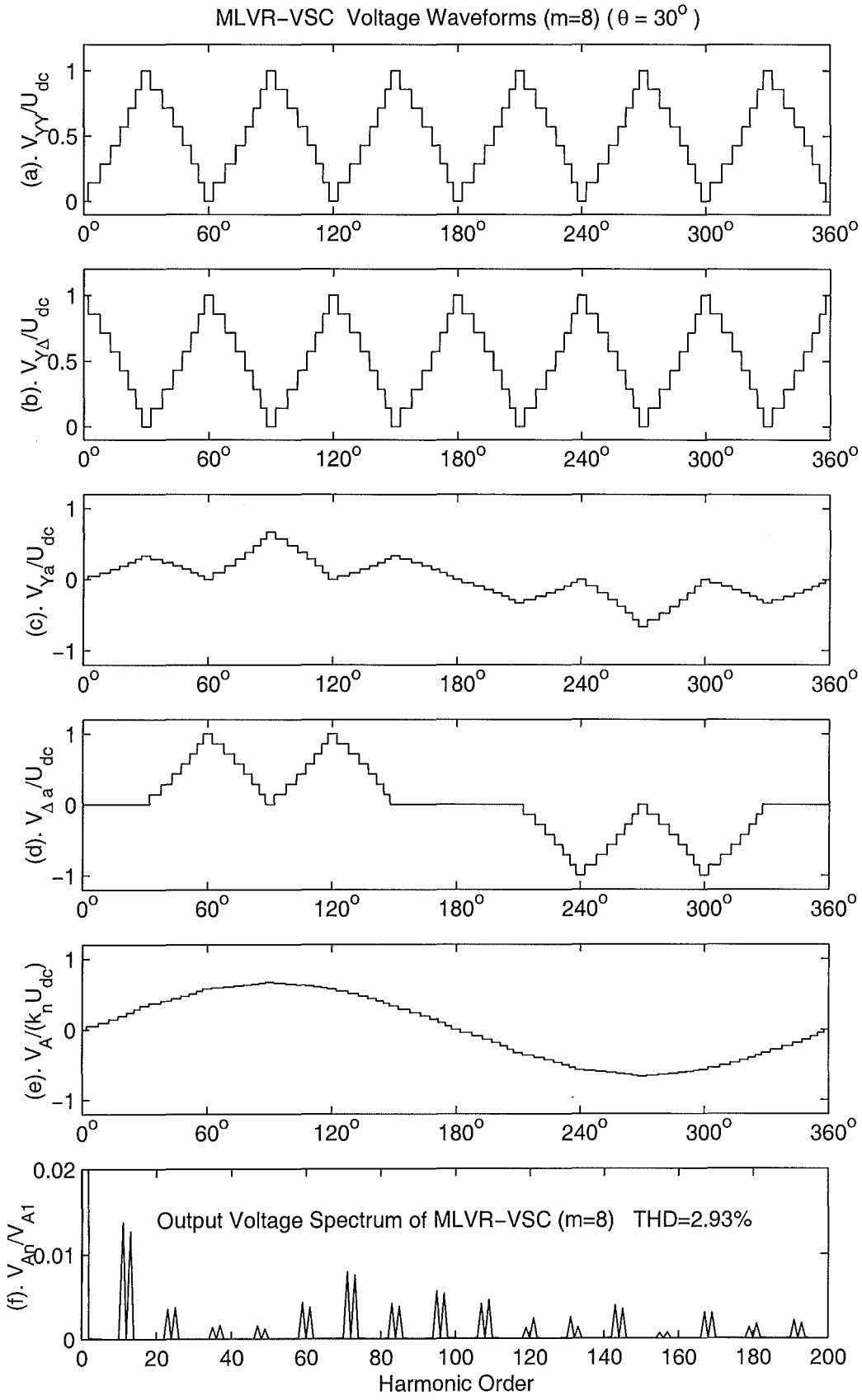


Figure 6.7 Voltage Waveforms under capacitor voltage balance control

output voltage waveform. In this chapter the effect of the switch path on-state adjustments is made with reference to the operating condition, represented by θ (the phase displacement between the converter system output current and voltage fundamentals). Equations 6.27, 6.28 and 6.32 describe the relationship between the adjustments and the phase placement θ under steady state operation conditions.

For an eight-level MLVR-VSC example, the adjustments, δ_i $(i = 2, 3, \cdots, 7)$, derived from equations 6.27 and 6.28, are shown in Figure 6.6. In the regions $-150^o < \theta < -30^o$ and $30^o < \theta < 150^o$, the adjustments are small, but in the regions $-165^o < \theta < -150^o$, $-30^o < \theta < -15^o$, $15^o < \theta < 30^o$ and $150^o < \theta < 165^o$, the adjustments increase sharply except for δ_7. Outside the region $8.5^o < |\theta| < 171.4^o$ the capacitor voltage balance will be lost for the eight-level MLVR-VSC.

Figure 6.7 shows the voltage waveforms of the eight-level MLVR-VSC for $\theta = 30^o$. The total harmonic distortion is calculated from the adjusted waveform as $THD = 2.93\%$.

Finally Figure 6.8 shows the total harmonic distortion of the eight-level MLVR-VSC output voltage versus the possible range of power angles θ.

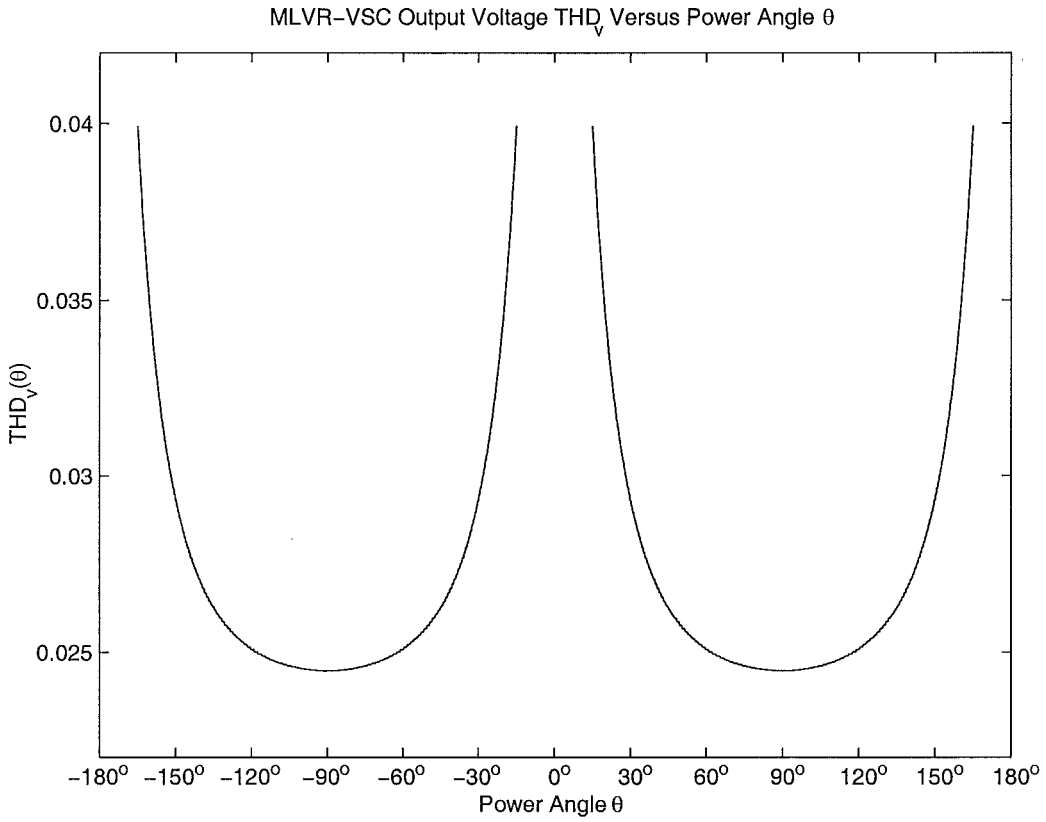


Figure 6.8 Voltage THD Variation Versus Power Angle

6.10 CONCLUSIONS

This chapter has analyzed the capacitor voltage balance conditions for the MLVR-VSC. The main conclusions are:

1. The MLVR-VSC can be used to control real and reactive power; when the power angle θ is not equal to $\pm 90^o$ the capacitor voltage balance can be maintained by adjustments of the reinjection path on-state intervals.

2. The waveform distortion caused by the adjustments is insignificant if the power angle θ is within the regions of $-150^o < \theta < -30^o$ and $30^o < \theta < 150^o$.

3. The MLVR-VSC can operate properly and maintain capacitor voltage balance in the power angle range of $(\frac{11\pi}{12} + \frac{\pi}{4(m-1)} > |\theta| > \frac{\pi}{12} - \frac{\pi}{4(m-1)})$; but can not operate in the regions of $-15^o < \theta < 15^o$, $165^o < \theta < 180^o$ and $-180^o < \theta < -165^o$ for a long period with balanced capacitor voltage.

4. The current harmonic components caused by the converter voltage harmonics have no effect on the capacitor voltage balance.

5. The source voltage asymmetry and harmonic distortion influence the capacitor voltage balance, but can also be removed by adjustments of the reinjection path on-state intervals.

Chapter 7

ESEDS-VSC AND MLVR-VSC SIMULATION STUDIES

7.1 INTRODUCTION

FACTS devices based on the self-commutated VSC are becoming more attractive than conventional FACTS controllers for their high performance, lower energy consumption, flexible active power transfer and reactive power generation control ability.

The Static Compensator (STATCOM) is a good example of self-commutated VSC application for reactive power injection control. Compared to the Static VAr Compensator (SVC), the STATCOM responds more rapidly to change system operation conditions and offers a superior voltage performance, while acts as a reactive power generator. The MLVR-VSC is particularly suitable for high power STATCOM applications because it offers a practically undistorted waveform, lower power losses and reliable operating conditions.

Another interesting application of the self-commutated VSC is the Back-To-Back Voltage Source Converter Link (BTBVSCL) for the asynchronous interconnection of two separate systems. The BTBVSCL is more reliable than the back-to-back HVdc link formed by the conventional line-commutated thyristor converters, because it is not subjected to commutation failures during system voltage disturbances. Another advantage of the BTBVSCL compared to the conventional HVdc back-to-back link is that as well as transferring the active power it can generate reactive power at both sides of the link, i.e. functions as a STATCOM as well.

The purpose of this chapter is to verify and investigate the use of the MLVR-VSC and ESEDS-VSC configurations for STATCOM and BTBVSCL applications respectively. The verification demonstrates their ability to suppress the voltage and current harmonics, their dynamic control performance, active and reactive power flow control flexibility.

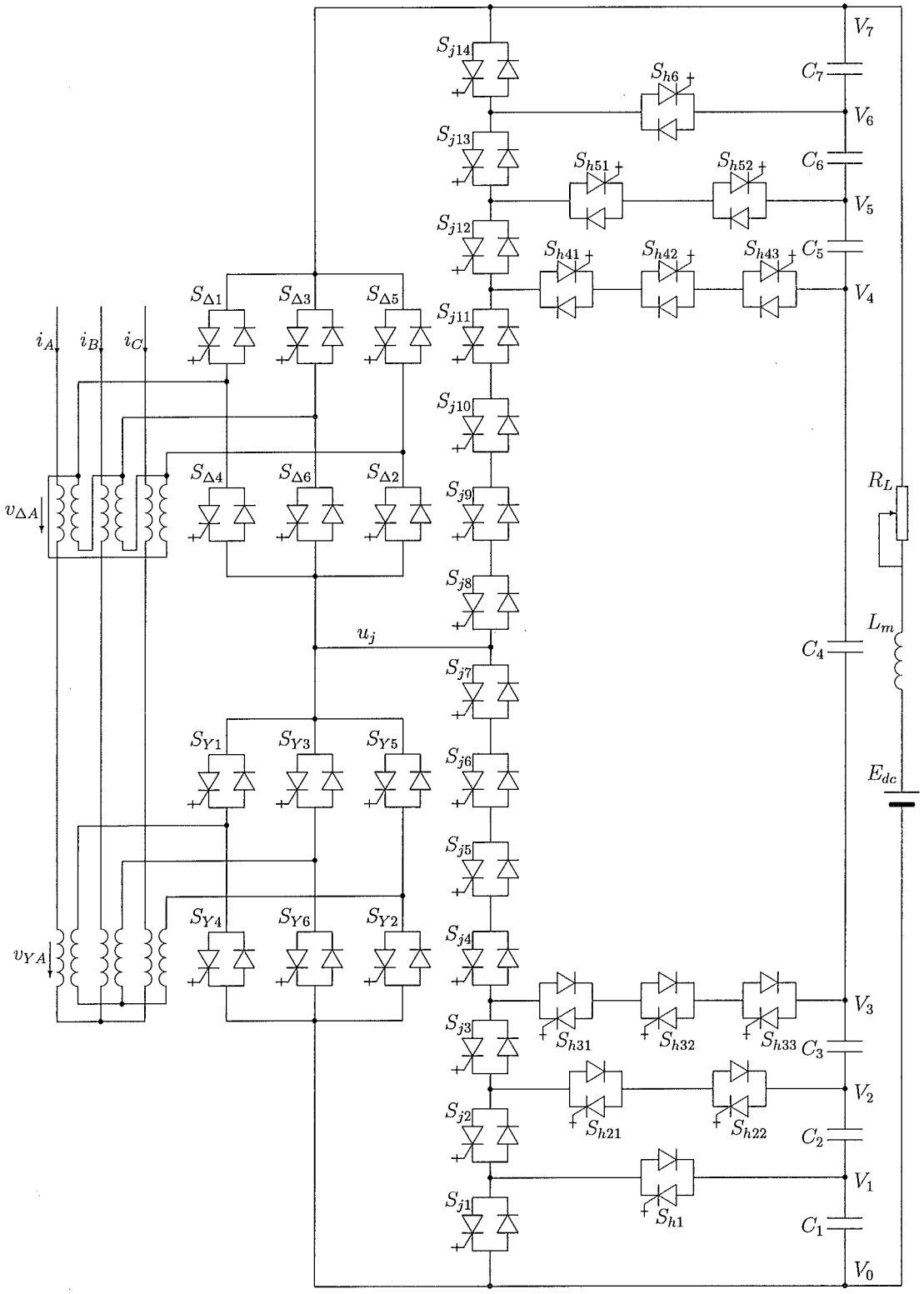


Figure 7.1 Test MLVR-VSC for STATCOM Application

7.2 THE MLVR-VSC OPERATED AS A STATCOM

7.2.1 MLVR-VSC control model

The test MLVR-VSC STATCOM is shown in Figure 7.1. A variable resistor and a dc source are placed in parallel with dc capacitors at the dc side to represent the losses in the MLVR-VSC and to simulate the capability to transfer active power between dc and ac systems, although this is not required by the conventional STATCOM application. The basic operation of the MLMVR-VSC STATCOM can be explained by the model shown in Figure 7.2. Due to the fundamental frequency switching the MLVR-VSC does not have independent amplitude and phase angle control, unlike PWM switching converters which do. There are only two control parameters in the MLVR-VSC case,

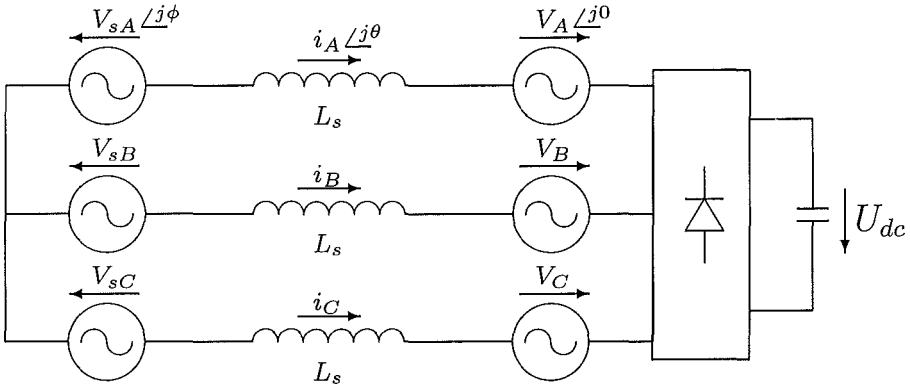


Figure 7.2 The reinjection VSC System Model

i.e. U_{dc}, the dc side capacitor bank voltage and ϕ, the phase angle differences between the converter output voltages and the source voltage. For STATCOM application the generated reactive power and the dc side voltage can be thought of as the variables to be controlled; however, a more directly relevant selection of variables is the reactive current component and the dc side voltage. The dc side voltage is controlled by changing ϕ, which controls the active power transfer to charge or discharge the dc side capacitors. The dc capacitor voltage U_{dc} then determines the amplitude of the MLVR-VSC ac output voltage. With reference to Figure 7.2, the following equations can be written:

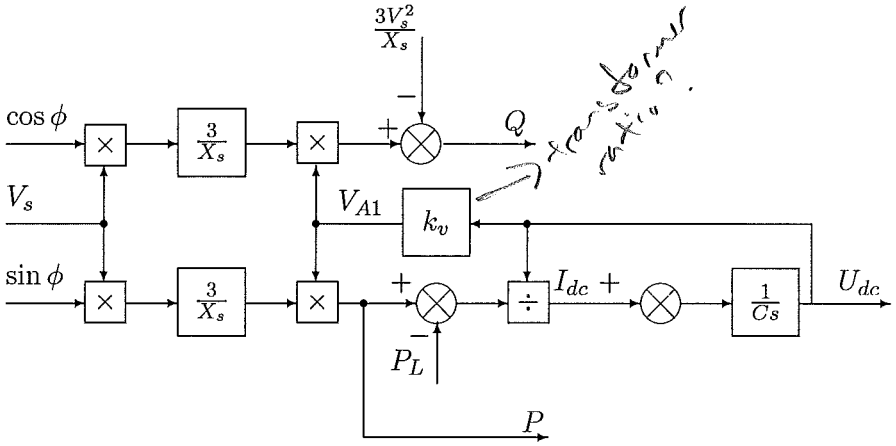
$$P = \frac{3V_sV_{A1}}{X_{s1}}\sin\phi \qquad Q = \frac{3V_sV_{A1}}{X_s}\cos\phi - \frac{3V_s^2}{X_s}$$

$$I_{Re} = \frac{V_{A1}}{X_{s1}}\sin\phi \qquad I_{Im} = \frac{V_{A1}}{X_{s1}}\cos\phi_1 - \frac{V_{s1}}{X_{s1}}$$

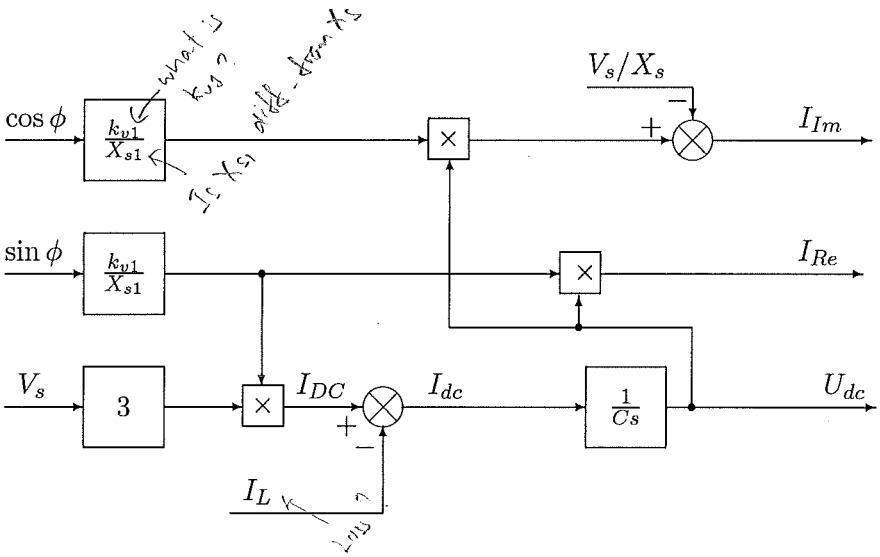
$$I_{dc} = [P - P_L]/U_{dc} \qquad U_{dc} = \frac{1}{C}\int I_{dc}dt$$

Based on the equations above the control block diagrams of the MLVR-VSC are drawn in Figure 7.3; diagram (a) is used for the control of the active (P) and reactive (Q)

powers , while diagram (b) is used for the control of real(I_{Re}) and imaginary (I_{Im}) current components.



(a). real and reactive power control diagram



(b). real and imaginary component currents control diagram

Figure 7.3 MLVR-VSC control block diagrams

7.2.2 MLVR-VSC STATCOM control system

The structure of the control system used for STATCOM operation is shown in Figure 7.4. The reactive power required by the ac system is set as the main reference order of the closed-loop control of an eight-level MLVR-VSC test system. The reactive power order is then converted to the imaginary current order I_{Im}^* as the direct reference order of the closed loop system to ensure that the MLVR-VSC is under the direct current control. By measuring the ac source 3-phase voltages and currents and performing a real and imaginary transformation, the actual imaginary current signal

I_{Im} is detected. The MLVR-VSC firing logic is synchronized with the ac power system to generate the required voltage waveforms. The current error $(I^*_{Im} - I_{Im})$ is sent to a PI controller to generate the required phase angle order for the MLVR-VSC to control the dc side voltage and output current and thus generate the required reactive power.

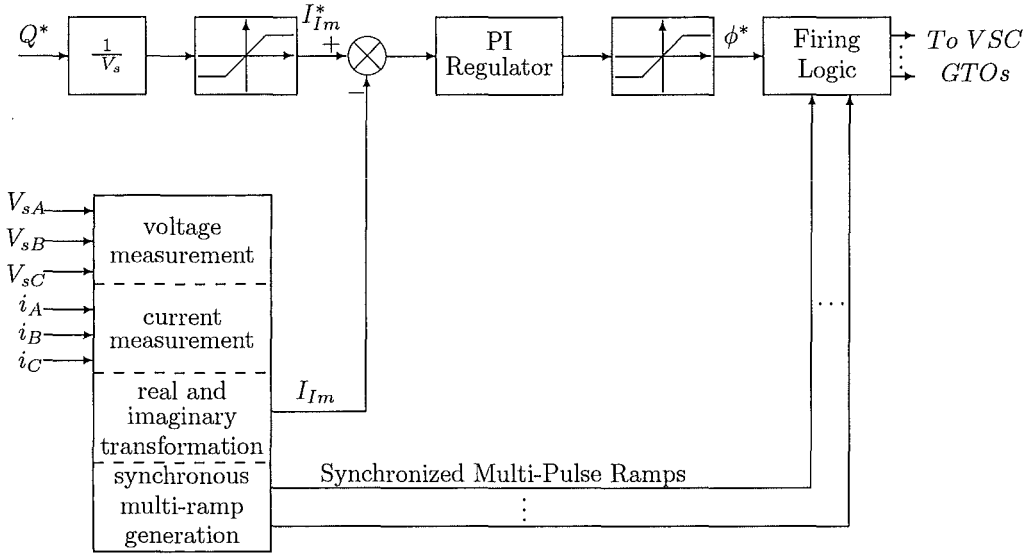


Figure 7.4 MLVR-VSC closed loop control structure

7.2.3 MLVR-VSC Simulations

A. MLVR-VSC Waveform Verification

The MLVR-VSC theoretical waveforms are verified by EMTDC simulation. The simulated waveforms, shown in Figure 7.5, correspond to an MLVR-VSC rated at 100MVA (i.e. two 50MVA converter bridges) and 100kV rated voltage, the nominal leakage reactance of the interface transformer is 10%. To test the capacitive operation under nearly ideal conditions the dc source is set to zero voltage ($E_{dc} = 0$) and the dc side variable load resistor to a very large value ($R_L > 10k\Omega$).

The waveforms in Figure 7.5 are:

- (a) U_j/U_{dc} the normalized reinjection voltage, also the voltage across the bridge connected to the Y/Y interface transformer.
- (b) I_j the reinjection current from the output terminal of the reinjection circuit to the neutral common point of the two series connected main bridges.
- (c) V_A/U_{dc} the normalized ac output voltage of the 8-level MLVR-VSC.
- (d) V_{An}/V_{A1} the output voltage spectrum of the 8-level MLVR-VSC.

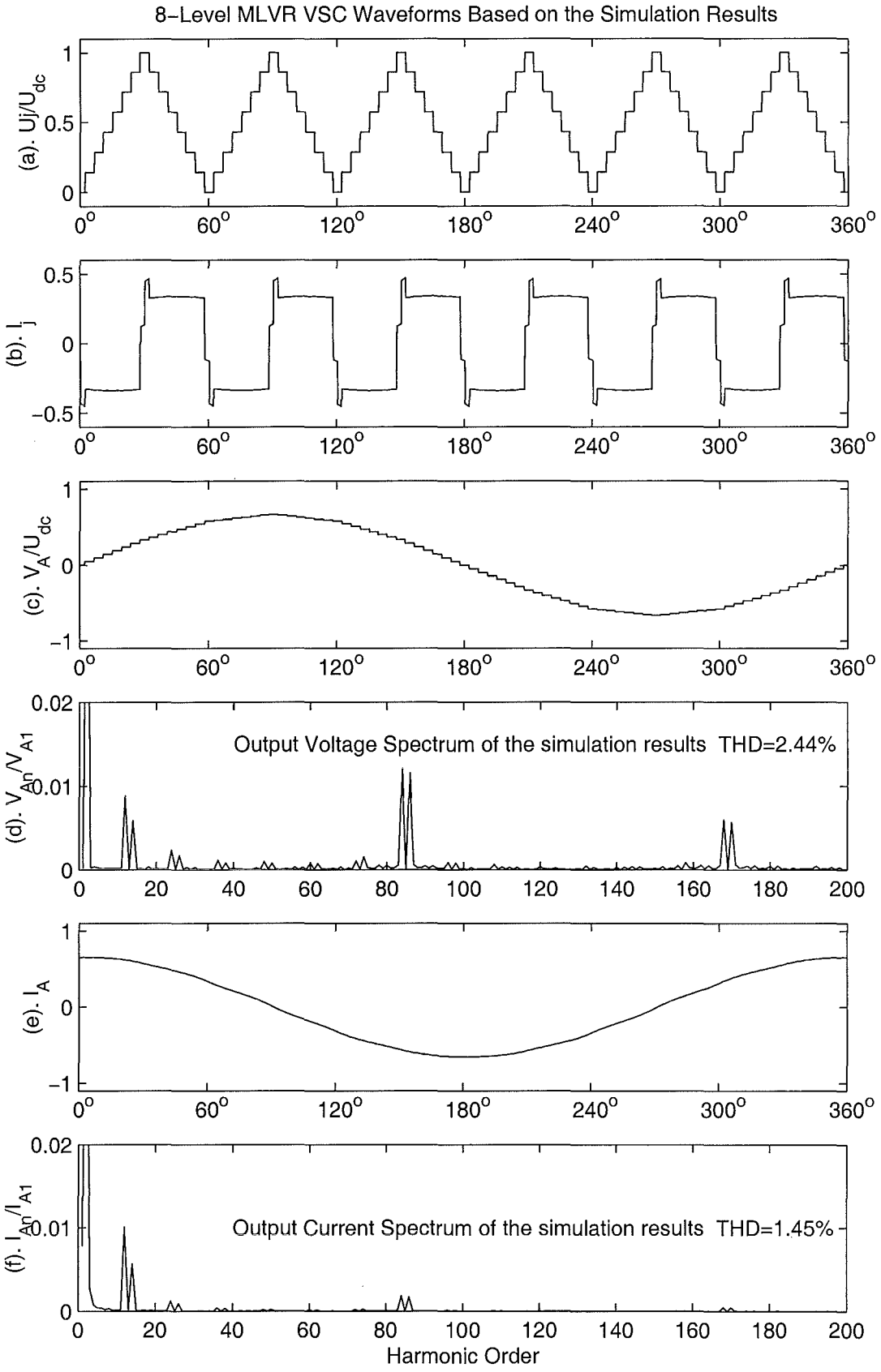


Figure 7.5 MLVR-VSC simulated Waveforms of Capacitive Operation

- (e) I_A the ac output current of the 8-level MLVR-VSC.
- (f) I_{An}/I_{A1} the output current spectrum of the 8-level MLVR-VSC.

These waveforms are almost the same as the previously derived theoretical waveforms. The simulated output voltage THD is 2.44%, while the theoretical value was 2.45%. Comparing the simulated I_A [Figure 7.5(e)] with the theoretical output current I_A [Figure 5.6(a)] practically there is no difference in their shape although the simulated amplitude is lower. The total harmonic distortions are 1.03% and 1.45% for the theoretical and simulated output currents respectively; this difference is caused by the amplitude difference (the higher ac output current has lower THD from Equation 5.32).

B. Dynamic Performance

The MLVR-VSC requires smaller size of dc capacitors compared with conventional multi-level diode clamped VSC because the dc capacitor current frequency of the MLVR-VSC is six times the ac power source fundamental frequency, while the frequency is 3 times for the conventional multi-level diode clamped VSC. The smaller size of capacitors implies that faster dynamic response can be expected for the proposed MLVR-VSC. The dynamic performances of the 8-level MLVR-VSC as a STATCOM is investigated by EMTDC simulation.

The simulation for STATCOM operation is performed under the following conditions: rated apparent power (S_s) 100MVA, rated line voltage 100kV (the nominal base of the phase voltage is $V_{SR} = \frac{100kV}{\sqrt{3}}$), the nominal leakage impedance of the interface transformer $k_s = \frac{X_S}{3V_{SR}^2/S_s} = 10\%$. To test inductive and capacitive operation with about 1MW losses the dc source is set to zero ($E_{dc} = 0$) and the dc side load resistor to $R_L \approx 1.5k\Omega$.

The following normalized waveforms are shown in Figure 7.6:

- (a) Q, Q_{ref}: generated reactive power and reactive power order (capacitive being set to positive and inductive to negative)
- (b) $V_1 \cdots V_6$, U_{dc}: capacitor voltages and the total dc side voltage
- (c) V_A I_A: ac output voltage and current of the 8-level MLVR-VSC
- (d) $V_1 \cdots V_6$, U_{dc}: capacitors and total dc voltages in reduced time scale
- (e) V_A I_A Q_{ref}: ac output voltage and current in reduced time scale (Q_{ref} is added to indicate the order change instant)

The normalized bases for the waveforms in Figure 7.6 are

- $Q_{sR} = S_s = 100MVA$ for Q and Q_{ref}

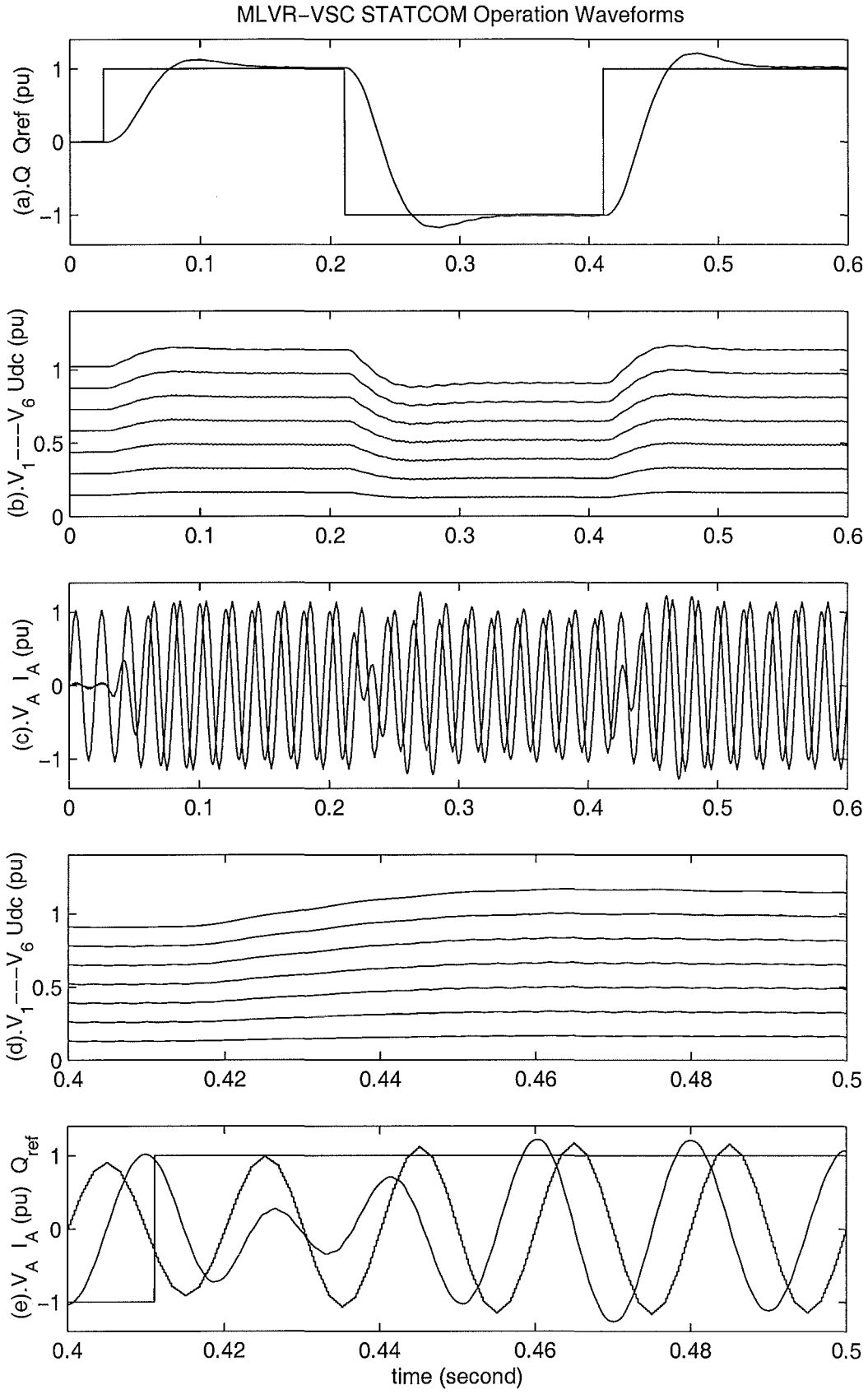


Figure 7.6 MLVR-VSC Dynamic Responses Under Step Reactive Orders

- $V_{SR} = \frac{100\sqrt{2}}{\sqrt{3}}kV$ for V_A
- $I_{SR} = \frac{\sqrt{2}S_s}{3V_{SR}}$ for I_A
- $U_{dcSR} = \frac{3\sqrt{2}}{2}V_{SR}$ for $V_1 \cdots V_6,\ U_{dc}$

The waveforms in Figure 7.6 show the steady and dynamic state performances of the 8-level MLVR-VSC functioning as STATCOM under closed loop control. In a period of 0.6 seconds the reactive power order is changed three times in full step increasing and decreasing. By choosing appropriate P and I parameters for the PI controller, the 8-level MLVR-VSC under closed loop control responds to these orders very well and generates the required reactive power without steady-state error.

Referring to Figure 7.6(a), the following dynamic performance is observed.

1. the reactive power order Q_{ref} changes from 0 to $1pu$ after 0.025 seconds, and the generated reactive power Q reaches the required value at 0.075 seconds; the dynamic process is completed at 0.125 seconds with a maximum over shoot of about 15%.

2. the reactive power order Q_{ref} changes from $1pu$ to $-1pu$ at 0.21 seconds, and the generated reactive power Q reaches the required value at 0.26 seconds; the dynamic process is completed at 0.33 seconds with a maximum over shoot of less than 18%.

3. the reactive power order Q_{ref} changes from $-1pu$ to $1pu$ at 0.41 seconds, and the generated reactive power Q reaches the required value at 0.46 seconds; the dynamic process is completed at 0.53 seconds with a maximum over shoot of less than 18%.

The waveforms in Figures 7.6 (b) and (d) demonstrate that the capacitor voltage balance is maintained under steady and dynamic state operating conditions. The waveforms in Figure 7.6(b) are for a 0.6 second period, while those in Figure 7.6(d) correspond to a period from 0.4 second to 0.5 second to show in greater detail that the capacitor voltages increase equally.

The waveforms in Figures 7.6 (c) and (e) demonstrate the ac output voltage and current waveforms in the dynamic and steady state regions. The waveforms in Figure 7.6(c) are for a 0.6 second period, while those in Figure 7.6(e) correspond to a period from 0.4 second to 0.5 second and demonstrate the dynamic response process in greater detail. The waveforms in Figure 7.6(e) show that the output voltage and current responses to the reactive power order are smooth, and that the MLVR-VSC can change its operating state from full scale inductive operation to full scale capacitive operation in 2 cycles approximately. Figure 7.6(e) also shows that the harmonic distortions of the output voltage and current waveforms are very low.

The simulation results verifies that the 8-level MLVR-VSC under closed loop control has fast dynamic performance and no steady-state error, with negligible harmonic distortion, and is thus suited to high power STATCOM application.

C. STATCOM Operation with Resistive Load

As described in chapter 6, the MLVR-VSC can operate properly for a range of power angle ($\frac{11\pi}{12} + \frac{\pi}{4(m-1)} > |\theta| > \frac{\pi}{12} - \frac{\pi}{4(m-1)}$), and that implies that a MLVR-VSC functioning as STATCOM can also supply dc power to a load on the dc side, that may be required. For STATCOM application the dc output voltage of the MLVR-VSC varies from 0.9pu to 1.1pu (for a nominal leakage reactance of 10%); it can therefore be used as a source of dc power for a load that does not require very stable dc voltage.

When the MLVR-VSC for STATCOM application also supplies dc power to a load, the capacitor voltage balancing control must continue to function very well to preserve the waveform quality of the MLVR-VSC. The EMTDC simulation results show that the capacitor voltage balancing control loops working well, the capacitor voltages being kept balanced with and without the dc load.

There are 6 loops for the test MLVR-VSC, all of them with the structure shown in Figure 7.7. The bottom capacitor voltage (V_1) is set as the reference, and all the others are controlled to be equal to V_1. The polarity of the measured reactive power Q_m is used to ensure that control action is taken in the right direction. The on-state interval adjustment δ_i for the i^{th} path is limited within the range required to keep the firing sequence in order.

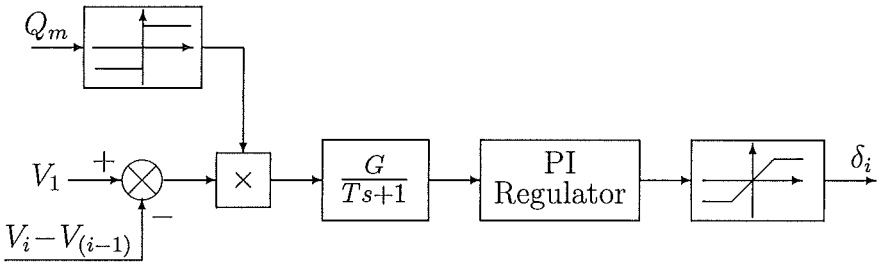


Figure 7.7 Capacitor Voltage Balance Control Loop

The simulation of STATCOM operation with a resistive dc load is performed under the same settings, except now $R_L \approx 300\Omega$. The simulation results shown in Figure 7.8 are arranged in the same order as those in Figure 7.6.

The active power P is added to Figure 7.8 (a) to show that the exchange of active power between the MLVR-VSC and the power system varies with the dc voltage U_{dc}. The waveforms in Figure 7.8 show that the MLVR-VSC can generate the required reactive power and transfer power to a load at dc side. When the operating power angle deviates

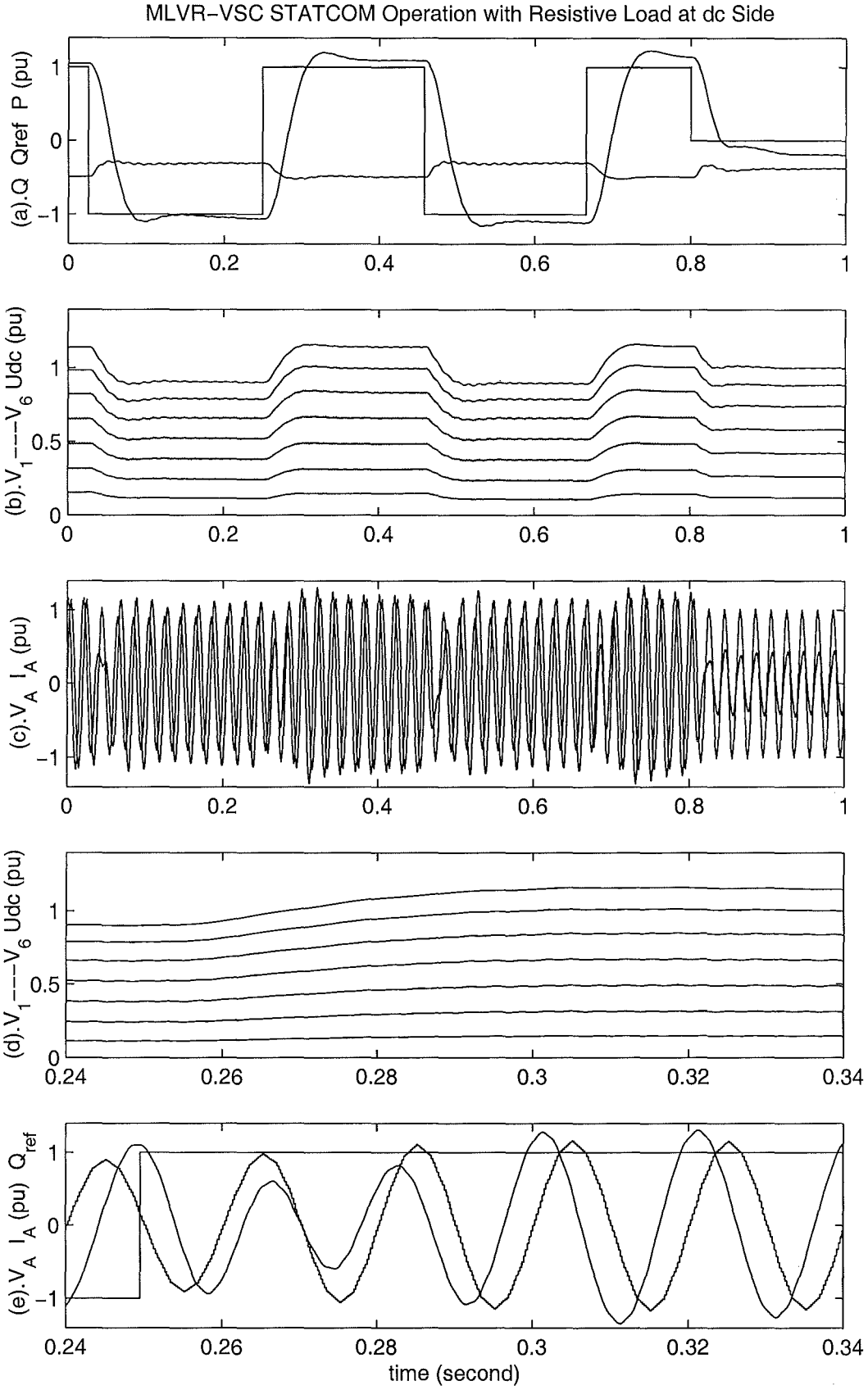


Figure 7.8 STATCOM Operation with resistive dc load

from $\pm 90^o$, i.e. the power is neither pure inductive nor pure capacitive, the MLVR-VSC can operate properly and the capacitor voltage can be kept in balanced condition.

D. Operation under Asymmetrical Source

In practice the power system voltage will always contain some asymmetry and thus the behaviour of the MLVR-VSC operating under asymmetrical conditions needs to be investigated. The purpose of the simulation is to verify whether the MLVR-VSC can operate normally, and the basic function of a STATCOM maintained, under the simple control strategy.

Under this control strategy the MLVR-VSC firing system keeps the MLVR-VSC output voltage symmetrical, i.e. setting $\phi_A = \phi_B = \phi_C$, and the three phase currents injected into the power system from the converter are very sensitive to the the source voltage asymmetry.

Independent control of the individual phase displacements can provide more control flexibility; however, the amplitudes of the converter output voltage fundamental of the individual phases are fixed by the dc voltage, and it is thus impossible to achieve symmetrical converter output currents when the source voltage amplitudes are different.

In practice the source voltage asymmetry is caused by imbalanced load currents and, therefore, even if the STATCOM supplied symmetrical current that would not improve the situation. It is difficult to make a decision on what kind of asymmetrical currents should be injected to the power system because this will depend on the operation conditions of the converter functioning as STATCOM and the compensation strategies.

The simulations for the MLVR-VSC controlled by the simple firing strategy are performed under the following asymmetrical source voltage conditions

1. A 5% voltage drop in one phase;
2. A 5% voltage drop in one phase and a 5% increase in another phase;
3. A 10% voltage drop in one phase;
4. A 10% voltage drop in one phase and a 10% increase in another phase;

The simulations are performed with negligible source impedance (i.e. less than 0.1%) and significant (about 5%) rated converter system impedance respectively and the results are shown in Figures 7.9 to 7.12 for case 1 to 4 respectively.

The waveforms shown in Figures 7.9 to 7.12 are

(a) Q, Q_{ref} the reactive power order and the measured reactive power;

(b) $V_1 \cdots V_6$, U_{dc} the dc capacitor voltages

(c) $\mathbf{V_m}$ the source three phase voltage amplitudes
to indicate asymmetrical level and period.

(d) I_A, I_B, I_C the converter system output currents of three phases

(e) V_A, V_{sA} the converter output and source voltages of phase "A"

(f) I_A, I_B, I_C the converter system output currents of three phases

(g) V_A, V_{sA} the converter output and source voltages of phase "A"

These simulated waveforms show that the MLVR-VSC can operate normally under asymmetrical source conditions; however the dc voltage U_{dc} contains a higher amplitude ripple of lower frequency; thus to maintain the ripple amplitude within the required margin for large asymmetry levels larger size of capacitors are required.

The time interval for the waveforms in (a) (b) (c) of Figures 7.9 to 7.12 is 1.6 seconds. In this interval the asymmetrical source voltages are set up as follows: first the source voltage of phase 'A' is dropped by 5% or 10% for about 0.6 seconds; then the source voltages of phases 'A' and 'B' are dropped and increased by 5% or 10% respectively for another interval of 0.6 seconds. These waveforms show that the MLVR-VSC can generate the required reactive power according to order under symmetrical and asymmetrical source voltages.

The waveforms in (d) (e) (f) (g) of Figures 7.9 to 7.12 are arranged in two groups (d–e and f–g group) each group is for a period lasting 0.4 seconds. Theses results illustrate in detail the three phase currents and voltages across the terminals on both sides of the interface transformer leakage reactance.

For inductive operation the waveforms provide the following information:

1. the amplitude of the symmetrical converter output voltage is closer to the amplitude of the lowest phase voltage (i.e. phase "A" for the performed simulations);

2. the lowest phase output current is produced by the lowest phase voltage of the asymmetrical source and the highest phase output current is produced by the highest phase voltage of the asymmetrical source;

3. with negligible source impedance and 10% nominal leakage reactance, in phase "A" with the voltage dropping by 5%, the other two phase output currents will be 1.5 times I_A;

4. as well as asymmetrical output currents the asymmetrical source voltage causes extra harmonic current distortion, the phase with the lowest output current being the most distorted;

5. with higher source impedance the asymmetrical level of the converter output currents and the harmonic distortion of the phase with the lowest output current are reduced.

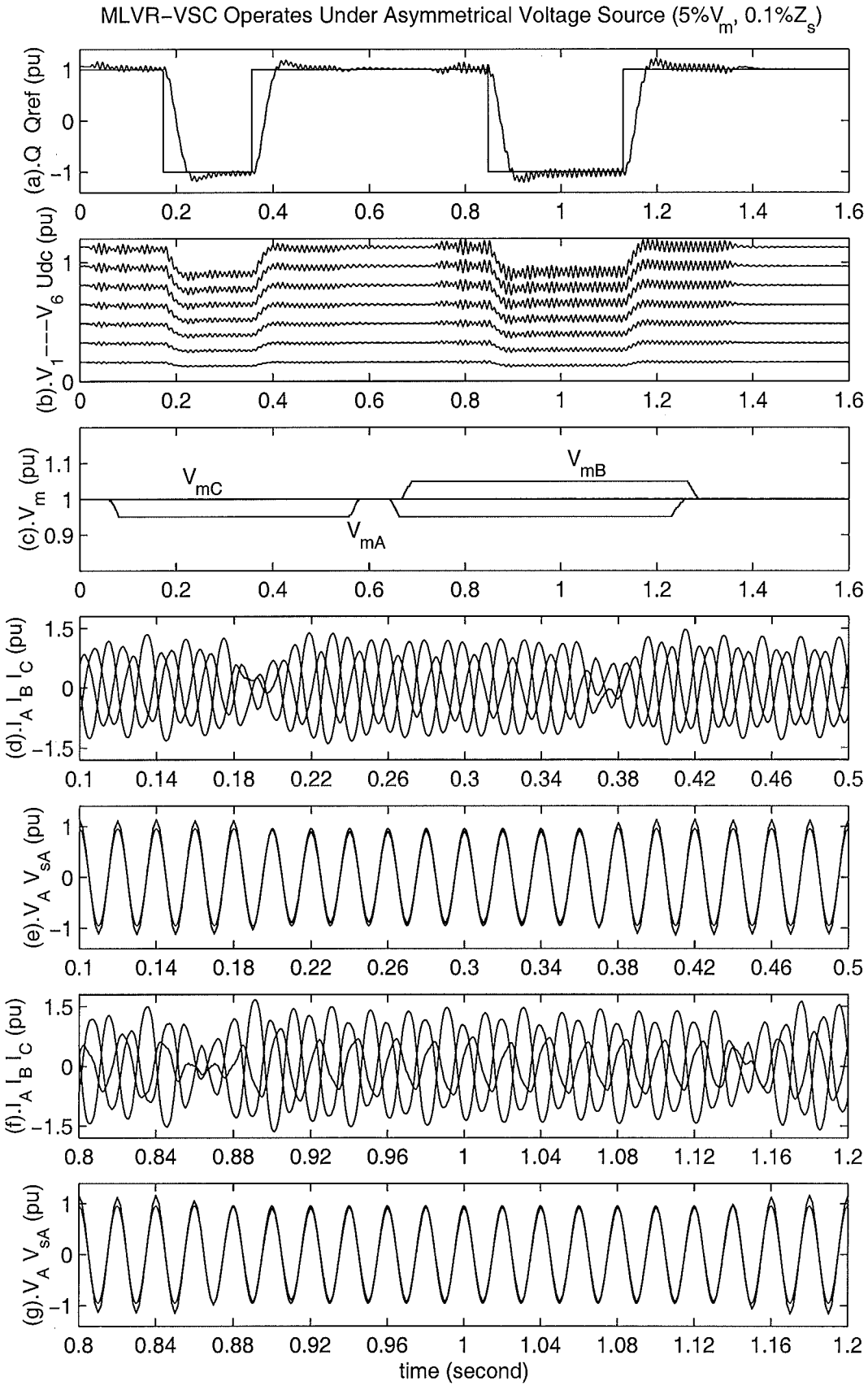


Figure 7.9 Asymmetrical Source Operation of MLVR-VSC (1)

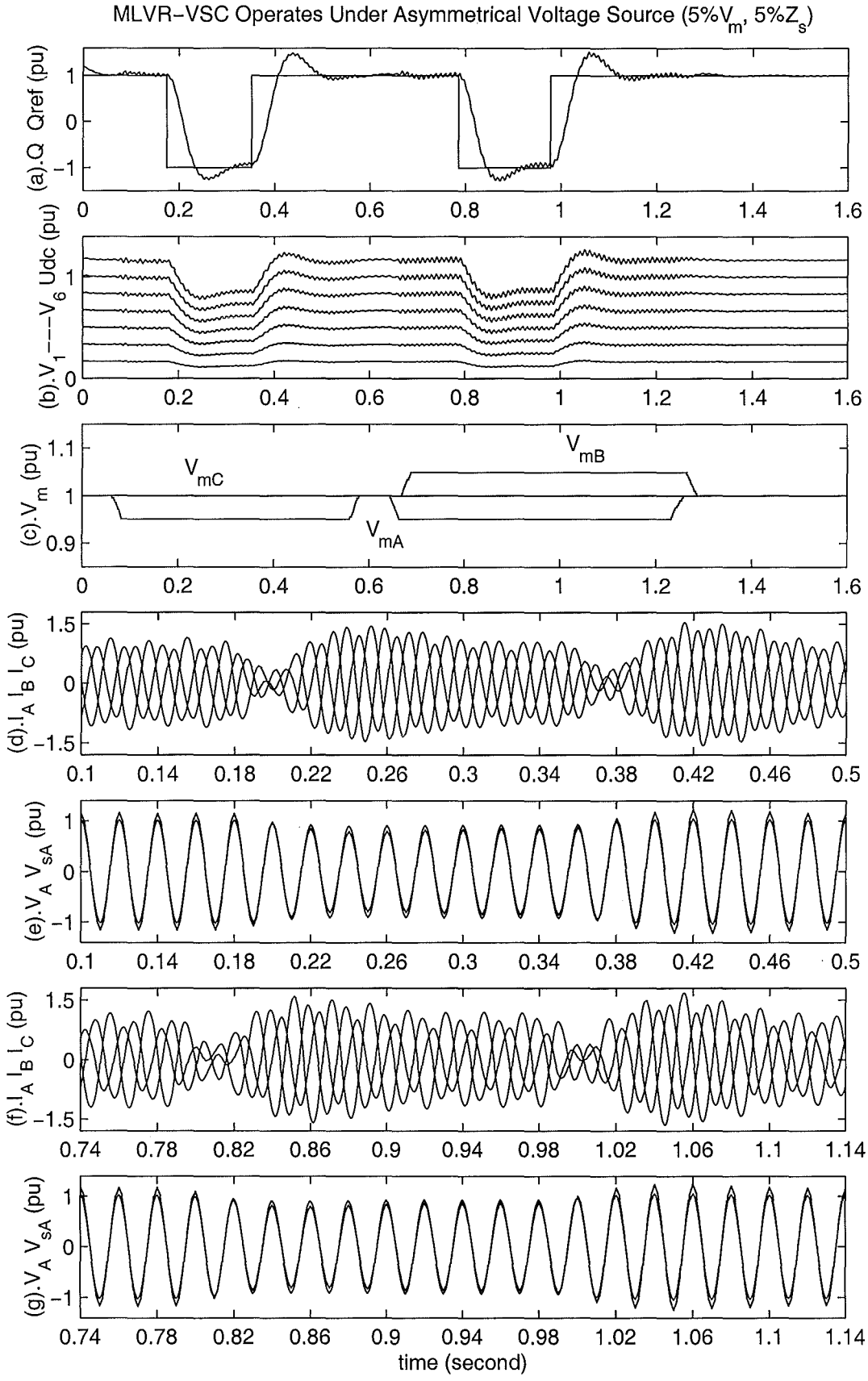


Figure 7.10 Asymmetrical Source Operation of MLVR-VSC (2)

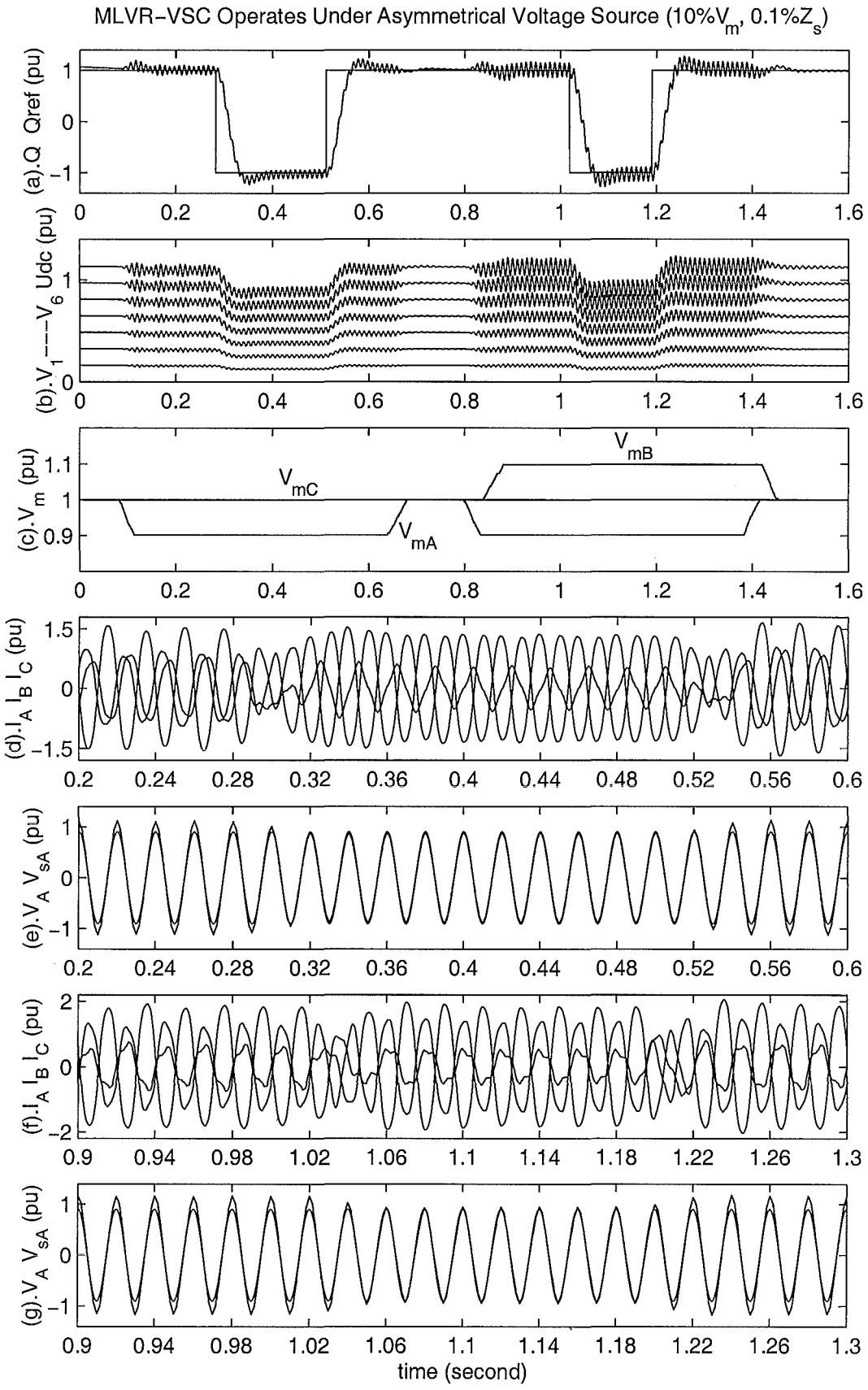


Figure 7.11 Asymmetrical Source Operation of MLVR-VSC (3)

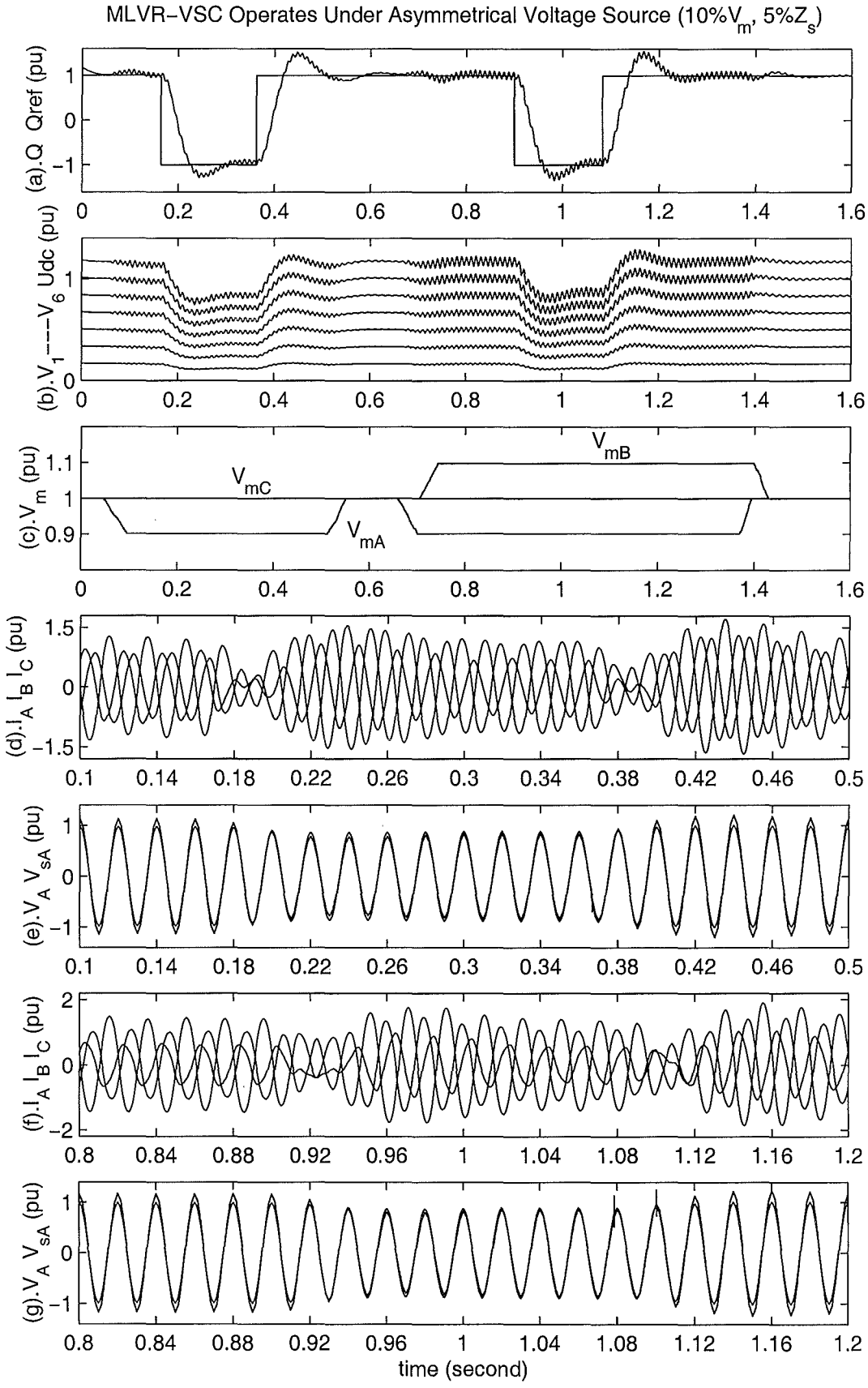


Figure 7.12 Asymmetrical Source Operation of MLVR-VSC (4)

For capacitive operation the waveforms provide the following information:

1. the amplitude of the symmetrical converter output voltage is closer to the amplitude of the highest phase voltage (phase "B" for the performed simulations);

2. the highest phase output current is produced by the lowest phase voltage of the asymmetrical source and the lowest phase output current is produced by the highest phase voltage of the asymmetrical source;

3. with negligible source impedance and 10% nominal leakage reactance if the voltage of phase "A" drops by 5%, the amplitudes of the other two phase output currents will be 1.5 times I_A;

4. as well as asymmetrical output currents, the asymmetrical source voltage causes harmonic current distortion, the phase with the lowest output current being the most distorted;

5. with higher source impedance the asymmetrical level of the converter output currents and the harmonic distortion of the phase with the lowest output current are reduced.

When the voltage source is asymmetrical the MLVR-VSC under the simple symmetrical firing control still provides the required compensation action by injecting more capacitive current to the phase with the lowest voltage or absorbing less inductive current from the phase with the lowest voltage.

7.3 BACK-TO-BACK DUAL ESEDS-VSC LINK

The ESEDS-VSC configuration (introduced in chapter 3) is used here as a basis for a Back-To-Back VSC Link (BTBVSCL). In order to reduce the switching losses, as described in chapter 3, the main bridges operate under fundamental frequency switching, while the reinjection bridges operate at six times the fundamental frequencies. A common dc capacitor links the two reinjection VSCs. A simplified model of the BTB link is shown in Figure 7.13, each reinjection VSC in the figure representing an ESEDS-VSC (shown in Figure 3.1). This test system is used to investigate active power transfer control and reactive power generation control.

7.3.1 The control model of the BTBVSCL

The high-level control of the BTBVSCL has to be developed taking into account the fundamental switching restriction that prevents independent amplitude and phase angle control. In the BTBVSCL there are only two input control parameters for the dual converters, i.e. the phase angle differences between the converter output voltages and

their respective source voltages. For active power transfer and reactive power generation control, the transferred active power, the generated reactive power and the dc side voltage can be thought as the output parameters; however a more relevant parameter selection is the active and reactive current components and the dc side voltage.

The dynamic model of the dual converter system is developed with reference to the model shown in Figure 7.13. Under the assumption of balanced operation, the interface transformers are modelled by their fundamental leakage reactances X_{s1} and X_{s2}. Through these two reactors the dual converter system is connected to two infinite power systems, which are modelled by ideal voltage sources with RMS voltage V_{s1}, (at 50Hz) and V_{s2} (at 60Hz). The ac output voltages are specified by the symbols V_{A1} and V_{A2} (RMS), and ϕ_1, ϕ_2 for the phase angle differences between the power system voltages and the converter system output voltages respectively. The ac output currents are specified by their real and imaginary components (I_{Re1}, I_{Im1}) and (I_{Re2}, I_{Im2}). The dc output currents are I_{dc1} and I_{dc2} and the shared capacitor voltage is denoted as U_{dc}.

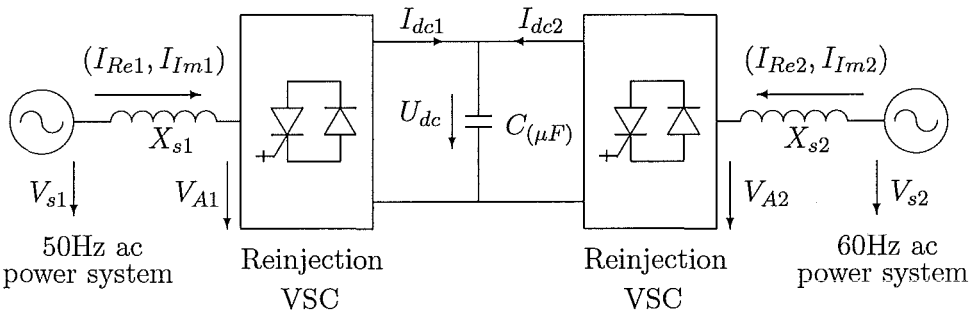


Figure 7.13 BTBVSCL System Model

Based on the model in Figure 7.13 the following formulas can be written:

$$P_1 = \frac{3V_{s1}V_{A1}}{X_{s1}}\sin(\phi_1) \qquad P_2 = \frac{3V_{s2}V_{A2}}{X_{s2}}\sin(\phi_2) \tag{7.1}$$

$$I_{Re1} = \frac{V_{A1}}{X_{s1}}\sin(\phi_1) \qquad I_{Re2} = \frac{V_{A2}}{X_{s2}}\sin(\phi_2) \tag{7.2}$$

$$I_{dc1} = [P_1 - P_{L1}]/U_{dc} \qquad I_{dc2} = [P_2 - P_{L2}]/U_{dc} \tag{7.3}$$

$$Q_1 = \frac{3V_{s1}V_{A1}}{X_{s1}}\cos(\phi_1) - \frac{3V_{s1}^2}{X_{s1}} \qquad Q_2 = \frac{3V_{s2}V_{A2}}{X_{s2}}\cos(\phi_2) - \frac{3V_{s2}^2}{X_{s2}} \tag{7.4}$$

$$I_{Im1} = \frac{V_{A1}}{X_{s1}}\cos(\phi_1) - \frac{V_{s1}}{X_{s1}} \qquad I_{Im2} = \frac{V_{A2}}{X_{s2}}\cos(\phi_2) - \frac{V_{s2}}{X_{s2}} \tag{7.5}$$

$$U_{dc} = \frac{1}{C}\int(I_{dc1} + I_{dc2})dt \tag{7.6}$$

where P_1 and P_2 are the real powers transferred from the 50Hz and the 60Hz power systems to the converters, P_{L1} and P_{L2} are the losses in the two converters, and Q_1 and Q_2 are the reactive powers generated by the two converters respectively.

Based on the equations above and the relations of $V_{A1} = k_{v1}U_{dc}$ and $V_{A2} = k_{v2}U_{dc}$

(which are obtained directly from Equation 3.11), Figure 7.14 shows the block diagram of the BTBVSCL used for the control of the active and reactive power.

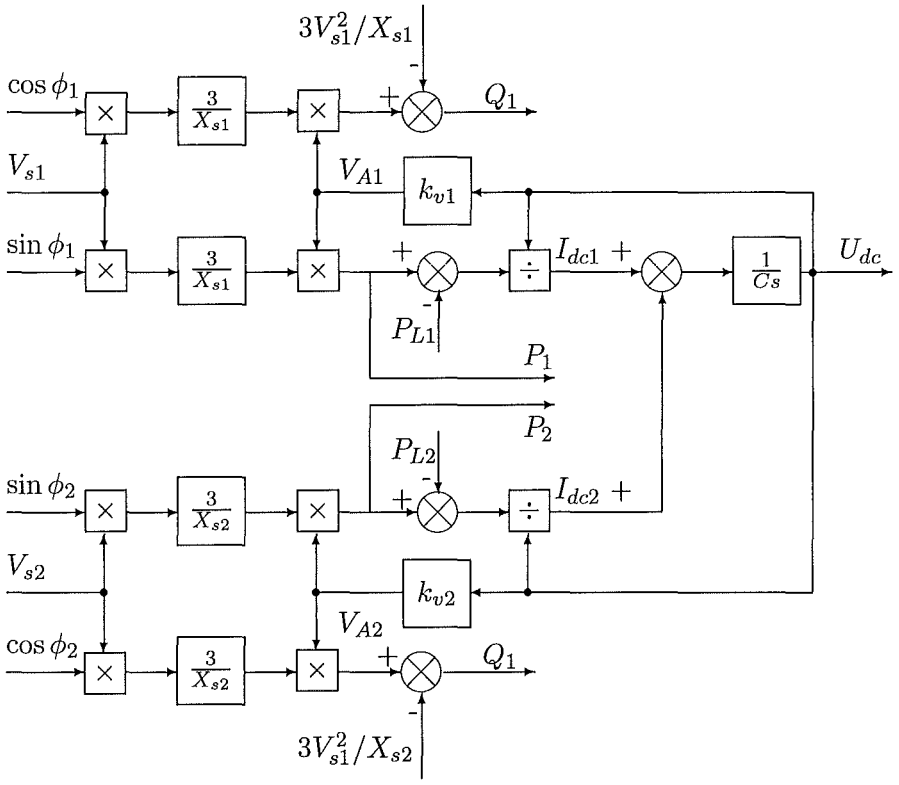


Figure 7.14 BTBVSC Link Block Diagram for Control of active and reactive power

Using the expressions $I_{DC1} = P_1/U_{dc} = [(k_{v1}/X_{s1})\sin(\phi_1)] \cdot (3V_{s1})$,
$I_{DC2} = P_2/U_{dc} = [(k_{v2}/X_{s2})\sin(\phi_2)] \cdot (3V_{s12})$
and $I_{L1} = P_{L1}/U_{dc}$, $I_{L2} = P_{L2}/U_{dc}$
the block diagram in Figure 7.14 can be simplified as shown in Figure 7.15, which applies more directly to the control of the active and reactive current components.

7.3.2 Operation Region of the BTBVSCL

As already indicated, the choice of fundamental frequency switching reduces control flexibility in that there is no independent amplitude and frequency control (like in PWM switching converters).

In the model of Figure 7.13, the topological structures of the two reinjection converter are the same, and therefore their ac output voltage amplitudes ought to be equal, i.e. $V_{A1} = k_{v1}U_{dc} \equiv V_{A2} = k_{v2}U_{dc} = V_A$. To deliver the same real power in either direction and generate the same reactive power, the rated source voltages and converter output ac currents ought to be equal, and also the leakage reactance of the two converter interface

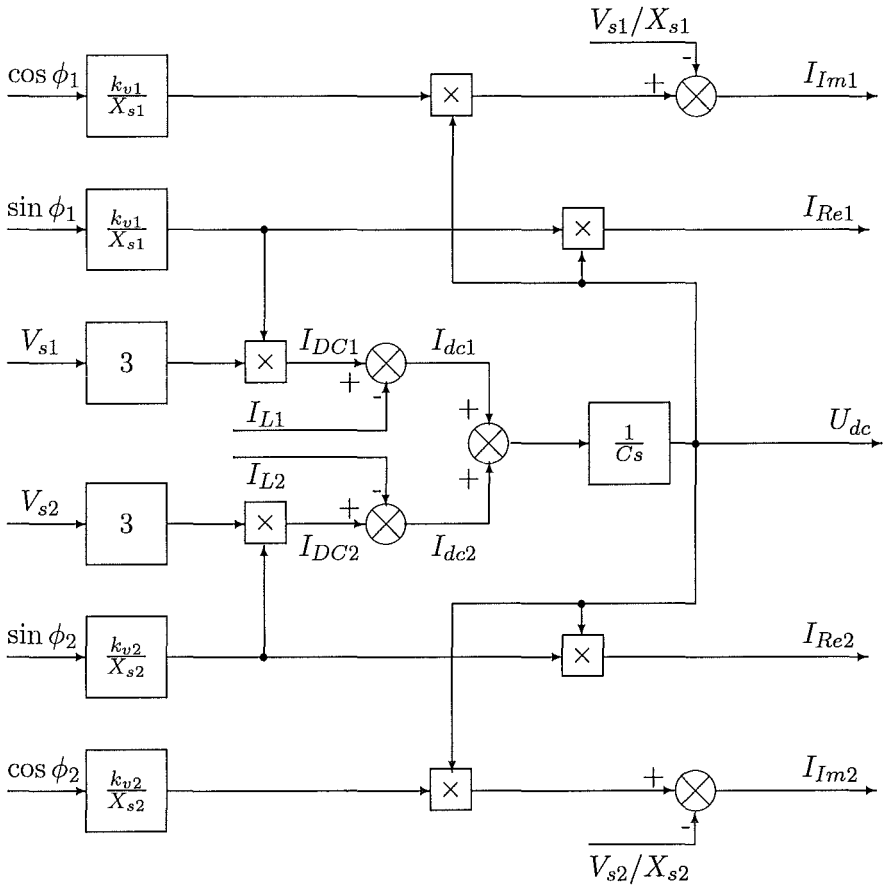
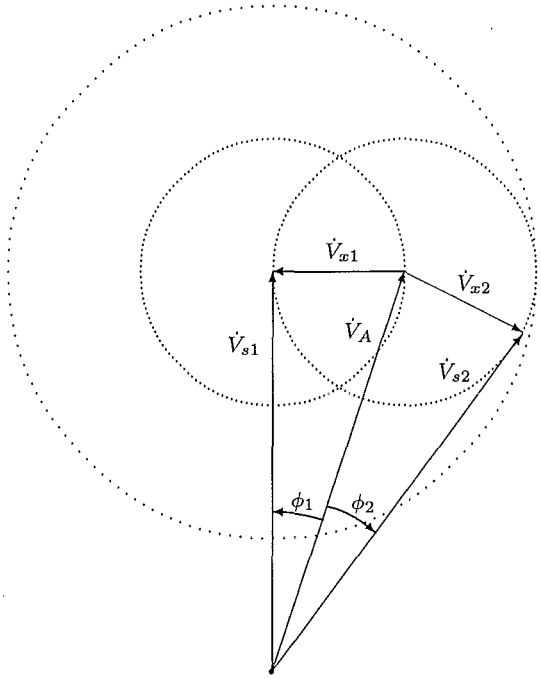


Figure 7.15 BTBVSC Link Block Diagram for Control of real and imaginary current

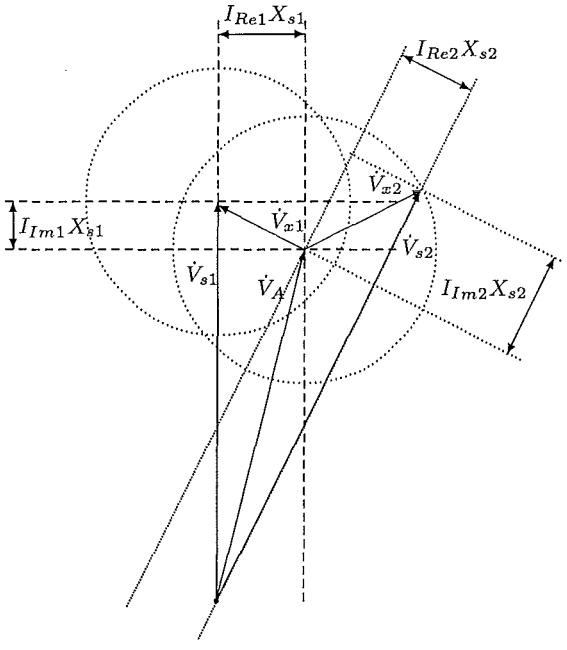
transformers should be approximately the same, i.e. $V_{sRated} = V_{s1Rated} = V_{s2Rated}$, $I_{ARated} = I_{A1Rated} = I_{A2Rated}$ and $X_{s1} \approx X_{s2}$.

Safe operation requires that the converter output currents must be equal or less than their rated values, and therefore the voltages across the two reactors are $V_{x1} = I_{A1}X_{s1} \leq I_{ARated}X_{s1}$, and $V_{x2} = I_{A2}X_{s2} \leq I_{ARated}X_{s2}$. This requirement in terms of the phasor diagram in Figure 7.16 means that the phasor $\dot{V}_{x1}$ must be located in a circle centered at the end of phasor $\dot{V}_{s1}$ with a radius of $I_{ARated}X_{s1}$. Also phasor $\dot{V}_{x2}$ must be located in a circle centered at the end of phasor $\dot{V}_A$ with a radius of $I_{ARated}X_{s2}$. Because with the adjustment of dc side voltage the end of phasor $\dot{V}_A$ can be anywhere in the circle centered at the end of phasor $\dot{V}_{s1}$ with a radius of $I_{ARated}X_{s1}$, the possible location for the end of phasor $\dot{V}_{s2}$ is in the circle centered at the end of phasor $\dot{V}_{s1}$ with a radius of $I_{ARated}(X_{s1} + X_{s2})$. These safe operating margins are shown in diagram (a) of Figure 7.16.

The phase angle differences, ϕ_1 and ϕ_2, between the source voltages and the converter output voltages V_{A1}, are the most important and controllable parameters of the dual converter system. For the steady-state operation, based on the safe current operation



a. Safe operation Margin



b. Steady State Operation Relationship Between Two Converters

Figure 7.16 Phaser Diagram of The Dual VSC System

limits, the maximum absolute values of ϕ_1 and ϕ_2 can be derived directly from the phasor diagram, i.e.

$$\Big[\sin|\phi_1|\Big]_{max} = \frac{I_{ARated}X_{s1}}{V_{s1}} = \frac{V_{sRated}}{V_{s1}}\frac{X_{s1}}{V_{sRated}/I_{ARated}} = \frac{V_{sRated}}{V_{s1}}x_{k1} \tag{7.7}$$

and

$$\left[\sin|\phi_2|\right]_{max} = \frac{I_{ARated}X_{s2}}{V_{s1}} = \frac{V_{sRated}}{V_{s2}}\frac{X_{s2}}{V_{sRated}/I_{ARated}} = \frac{V_{sRated}}{V_{s2}}x_{k2} \tag{7.8}$$

Using the rated voltages, i.e. $V_{s1} = V_{s2} = V_{sRated}$, the equations above become

$$\left[\sin|\phi_1|\right]_{max} = x_{k1}$$
$$\left[\sin|\phi_2|\right]_{max} = x_{k2}$$

These equations imply that the interface transformer nominal leakage reactance x_k governs the possible operating region. For example, if the 50Hz source operates at rated condition, i.e. $V_{s1} = V_{sRated}$, the possible amplitude range of the converter output voltage, V_A, is $V_{sRated}(1 - x_k) \leq V_A \leq V_{sRated}(1 + x_k)$, and that of V_{s2} is $V_{sRated}(1 - 2x_k) \leq V_{s2} \leq V_{sRated}(1 + 2x_k)$. That means that under a $2x_k$ percentage voltage depression the BTBVSCL system can operate safely, but the real power transfer and reactive power generation will be limited.

If one side source has the rated voltage ($V_{s1} = V_{sRated}$), the transferred active power P to the other side and the generated reactive power Q at the local side are those resulting from operating the VSC on this side with the corresponding active I_{Re} and reactive I_{Im} current components. The following analysis is based on a demand for I_{Re} and I_{Im} on the rated voltage system side. Because the efficiency of VSC is high, the losses in the dual converter system are neglected. Thus the active power transferred from the two power systems to the dual converter system must be zero under the steady condition. This restriction and the specified demand of I_{Re}, I_{Im} can be expresses by the equations below.

$$\begin{cases} \frac{k_v V_{s1}}{X_{s1}}\sin(\phi_1) & \approx & -\frac{k_v V_{s2}}{X_{s2}}\sin(\phi_2) \\ \frac{V_A}{X_{s1}}\sin(\phi_1) & = & I_{Re} \\ \frac{V_A}{X_{s1}}\cos(\phi_2) - \frac{V_{s1}}{X_{s1}} & = & I_{Im} \end{cases} \tag{7.9}$$

These equations predict that if the operation condition of one side of the BTBVSC system (I_{Re}, I_{Im}) is fixed, the other side is also fixed. The operating conditions specified by ϕ_1, ϕ_2 and U_{dc} are given as

$$\begin{cases} \sin(\phi_1) = \frac{I_{Re}X_{s1}}{\sqrt{(I_{Re}X_{s1})^2+(V_{s1}+I_{Im}X_{s1})^2}} \\ \sin(\phi_2) \approx -\frac{X_{s2}}{X_{s1}}\frac{V_{s1}}{V_{s2}}\sin(\phi_1) \\ U_{dc} = \frac{1}{k_v}\sqrt{(I_{Re}X_{s1})^2 + (V_{s1} + I_{Im}X_{s1})^2} \end{cases} \tag{7.10}$$

And the operating condition of the other VSC, specified by the (I_{Re2}, I_{Im2}), is

$$\begin{cases} I_{Re2} = & -\frac{V_{s1}}{V_{s2}} I_{Re} \\ I_{Im2} = & \sqrt{(\frac{X_{s1}^2}{X_{s2}^2} - \frac{V_{s1}^2}{V_{s2}^2}) I_{Re}^2 + \frac{X_{s1}^2}{X_{s2}^2}(\frac{V_{s1}}{X_{s1}} + I_{Im})^2} - \frac{V_{s2}}{X_{s2}} \end{cases} \tag{7.11}$$

It is clear that when the two source voltages and the two interface transformer leakage reactances are equal, i.e. $V_{s1} = V_{s2}$, $X_{s1} = X_{s2}$, the dual converter system keeps the real power balance and can generate the same amount of reactive power on both sides. Equation 7.11 also reveals that when the dual converter system does not transfer real power (i.e. $I_{Re2} = I_{Re} = 0$), the two converters can not operate as two STATCOMs independently because $I_{Im2} = I_{Im} + (V_{s1} - V_{s2})/X_{s2}$.

The phasor diagram in Figure 7.16 (b) shows the steady state operation restrictions under specified active and reactive current components (I_{Re}, I_{Im}) at one converter side. The circle centered at the end of phasor $\dot{V}_{s1}$ with radius of $I_{ARated}X_{s1}$ is the area of the end of phasor $\dot{V}_A$ for safe operation; and the circle centered at the end of phasor $\dot{V}_A$ with radius $I_{ARated}X_{s1}$ is the area of the end of phasor $\dot{V}_{s2}$. The circle centered at the end of phasor $\dot{V}_{s1}$ is divided by the line along the phasor $\dot{V}_{s1}$ into two half circles. The left half indicates a supply of real power from the V_{s1} side to the V_{s2} side, and the right half a supply of real power from the V_{s2} side to the V_{s1} side. The circle centered at the end of phasor $\dot{V}_{s1}$ is divided by the horizonal line being vertical to phasor $\dot{V}_{s1}$ into two half circles. The upper and lower half regions indicate reactive power generation and absorbtion at the V_{s1} side respectively. Phasor $\dot{V}_A$ in Figure 7.16 represents the two converter output voltages, because their amplitudes are the same and their phase angle differences from the two source voltages are independent. Figure 7.16 also shows that the amplitude of the two source voltages (V_{s1}, V_{s2}), the dc side voltage U_{dc} (the amplitude of $\dot{V}_A$ is proportional to the dc side voltage U_{dc}), and the two controllable phase angles (ϕ_1, ϕ_2) determine the dual system operating state, and the leakage reactance of the interface transformers determines the possible safe operating region. An appropriate arrangement of the two interface transformer leakage reactances can ensure the safe operation under normal and to some degree under fault conditions.

7.3.3 The Control Structure of The BTB-VSC Link

The transfer of specified real power and the generation of the required reactive power is the main goal of the BTBVSC dc link. Under normal operation conditions the real and imaginary components of the converter output currents directly determine the active and the reactive power, and thus can be used directly as the control variables. Moreover under abnormal conditions the direct current control can operate the system more safely as compared with the use of active and reactive power as control variables.

As shown in the previous subsection the real and imaginary output current components of one side converter are related to those of the other side, therefore the output current real component of the 50Hz side and the output current imaginary component of the 60Hz side are set as the parameters to be controlled, while the imaginary component of the 50Hz side and the real component of the 60Hz side are dependent on the operating state.

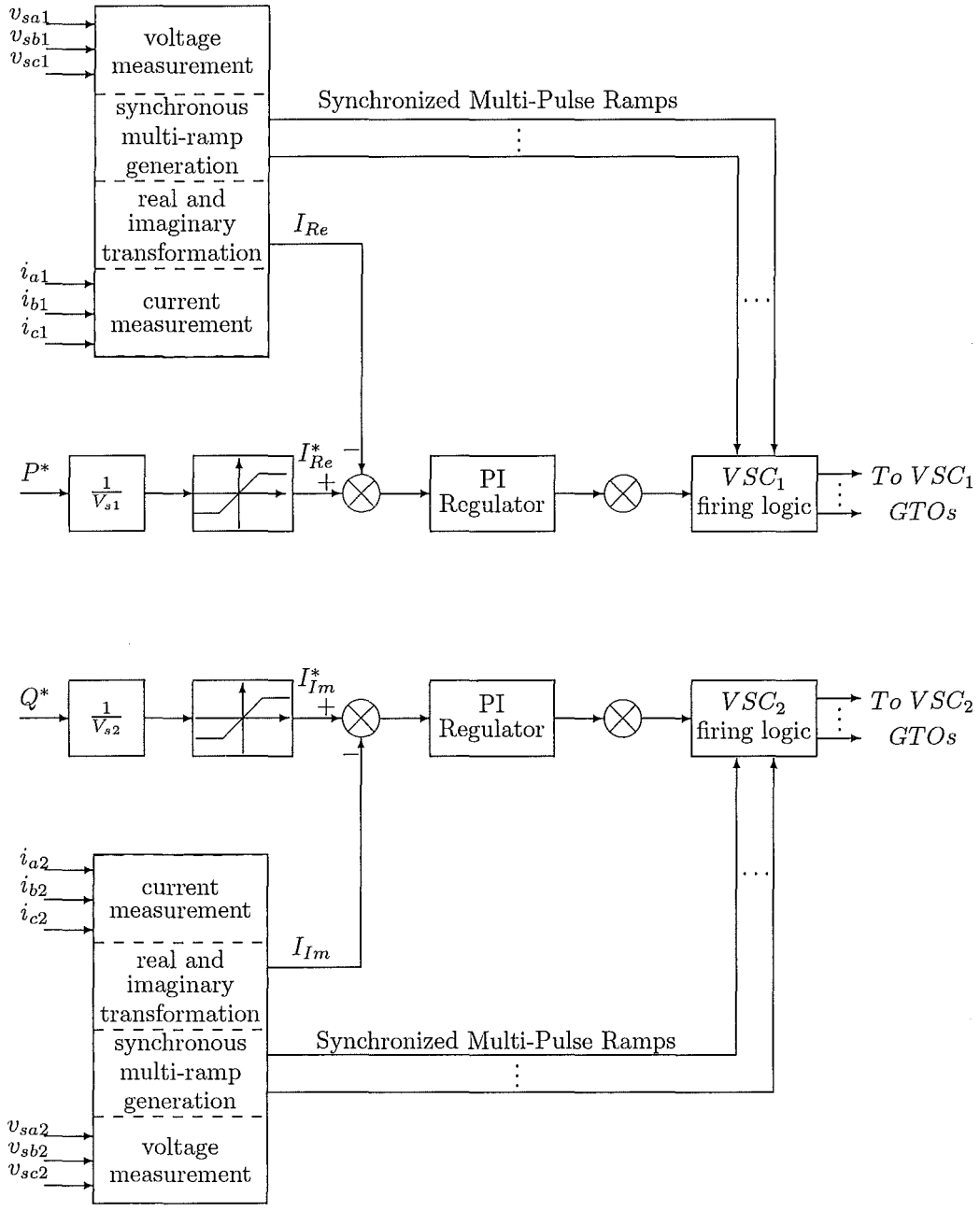


Figure 7.17 The BTB-VSC-Link Control Structure

The simplified control structure of the dual converter system is shown in Figure 7.17. The dual converter system output currents are measured and transformed into real and imaginary current components. The monitored source voltages are then used as a reference for the real and imaginary current transformation. The multi-pulse ramp signals for the converter GTO firing logic are synchronized with the source voltages respectively. The real power and reactive power reference P^* and Q^*, are divided by the source voltages to obtain the real and imaginary current commands. Proportional regulators with saturation limitation ensure the input references of the direct current control system to be in the safe operation region under normal and depressed source voltage conditions. The two PI controllers generate the phase angle displacement commands depending on the real and imaginary current errors for the two converters respectively.

7.3.4 Test System and Simulation Results

The test system of Figure 7.13 shows an asynchronous interconnection between two seperate systems, represented by two ideal three phase voltage sources with a purely reactive impedance in series; their rated voltages are 100kV, and the operation frequencies are 50Hz and 60Hz respectively. The BTB-VSC-Link under investigation is set to deliver 100MW of real power in either direction, and additionally provide ±50 MVAr at each side under normal operation conditions; each interface transformer is rated for 50MVA, 100kV, and 10%($k_s = 10\%$) of the nominal leakage reactance, and their turns ratio is k_n.

A. ESEDS-VSC Waveform Verification

To verify the theoretical ESEDS-VSC waveforms the two ESEDS-VSCs in the BTB-VSC-Link are controlled to generate 0.5pu reactive power. The full cycle waveforms on the 50Hz side obtained from EMTDC simulation, are shown in Figure 7.18; these are

- (a) U_j the normalized reinjection voltage, the nominal base being the dc voltage U_{dc}.
- (b) I_j the normalized reinjection current, the nominal base being $\frac{1000k_n}{\sqrt{3}}$.
- (c) V_A the normalized ac output voltage of the ESEDS-VSC, the base being $k_n U_{dc}$.
- (d) V_{An}/V_{A1} the output voltage spectrum of the 50Hz ESEDS-VSC.
- (e) I_A the normalized ac output current of the ESEDS-VSC, the base being $\frac{1000k_n}{\sqrt{3}}$.
- (f) I_{An}/I_{A1} the output current spectrum of the ESEDS-VSC.

These waveforms are very much the same as the previously derived theoretical waveforms in chapter 3. The simulated output voltage THD is 5.13%, while the theoretical

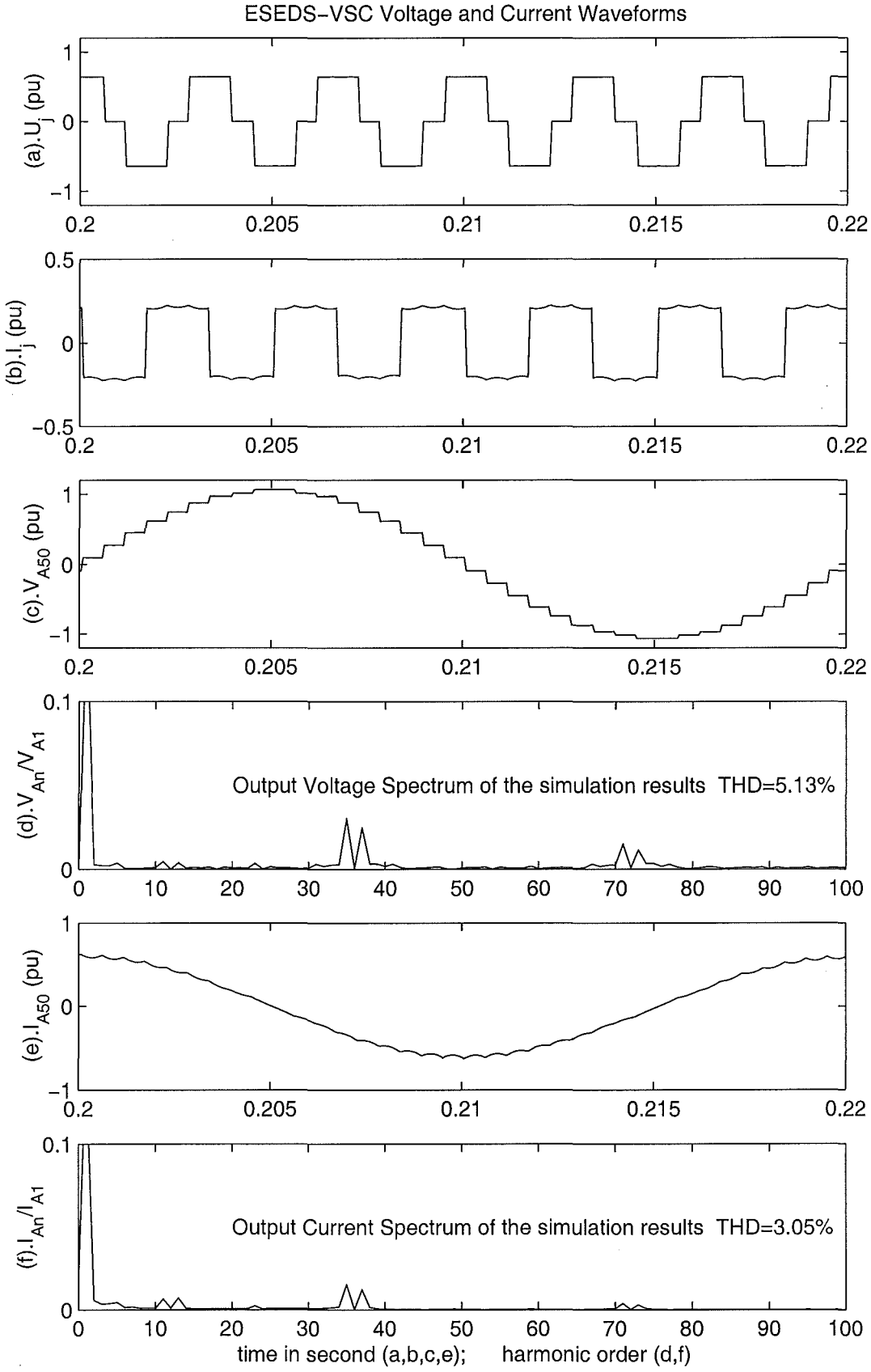


Figure 7.18 Simulated Voltage and Current Waveforms of the ESEDS-VSC

value was 5.09%. Comparing waveform I_A [Figure 7.18(e)] with the theoretical output current waveform in Figure 3.6(a) there is practically no difference in their shapes but the simulated amplitude is somewhat lower. Comparing the spectrum of I_A [Figure 7.18(f)] with the theoretical output current spectrum in Figure 3.7(a) there is practically no difference in harmonic distribution but their respective THDs differ; these are 1.38% and 3.05% for the theoretical and simulated output currents respectively, the difference however is due to the lower amplitude output current in the simulation results.

B. Active Power Response

The effect of using the direct real and imaginary current control strategy depicted in Figure 7.17 is investigated in this section.

Figures 7.19 and 7.20 show the dynamic response under normal conditions to step changes in the real power interchange order and zero imaginary current order. Initially the system operates without real power interchange and zero imaginary current generation. After $t = 50ms$ the real current control order is set to 1 pu that corresponds to 100 MW real power transfer from the 50Hz system to the 60Hz system under the rated voltage condition. After $t = 250ms$ the real current control order is reversed, and at $t = 650ms$ the real current order is set to zero again . The plots in Figure 7.19 show the dynamic behavior of the real and imaginary power of the two systems (P50, Q50, P60, Q60) and two phase angle displacements between the sources and the converter output voltages (ϕ_{50}, ϕ_{60}) in the period of $0 < t < 800ms$. The plots in Figure 7.20 show the voltage and current waveforms, which are

1. i_{dc50} (the dc output current of the 50Hz and 60Hz system side converters),
2. u_{dc} (the dc voltage across the dc capacitor),
3. i_{dc} (the current through the dc capacitor),
4. I_{A50} (the phase current of the 50Hz system),
5. V_{A50} (the phase output voltage of the 50Hz system side converter),
6. I_{A60} (the phase current of the 60Hz system),
7. V_{A60} (the phase output voltage of the 60Hz system side converter).

To show the dynamic process more clearly the waveforms of (I_{A50}, V_{A50}) and (I_{A60}, V_{A60}) are plotted in greater detail for the interval $0.2 < t < 0.4$. All the waveforms show that following the change of real current order it takes about 60ms for the system to reach new steady-state conditions. The plots of (I_{A50}, V_{A50}) and (I_{A60}, V_{A60}) in Figure 7.20 (e) and (f), show clearly that after 2 to 3 cycles the dual converter system

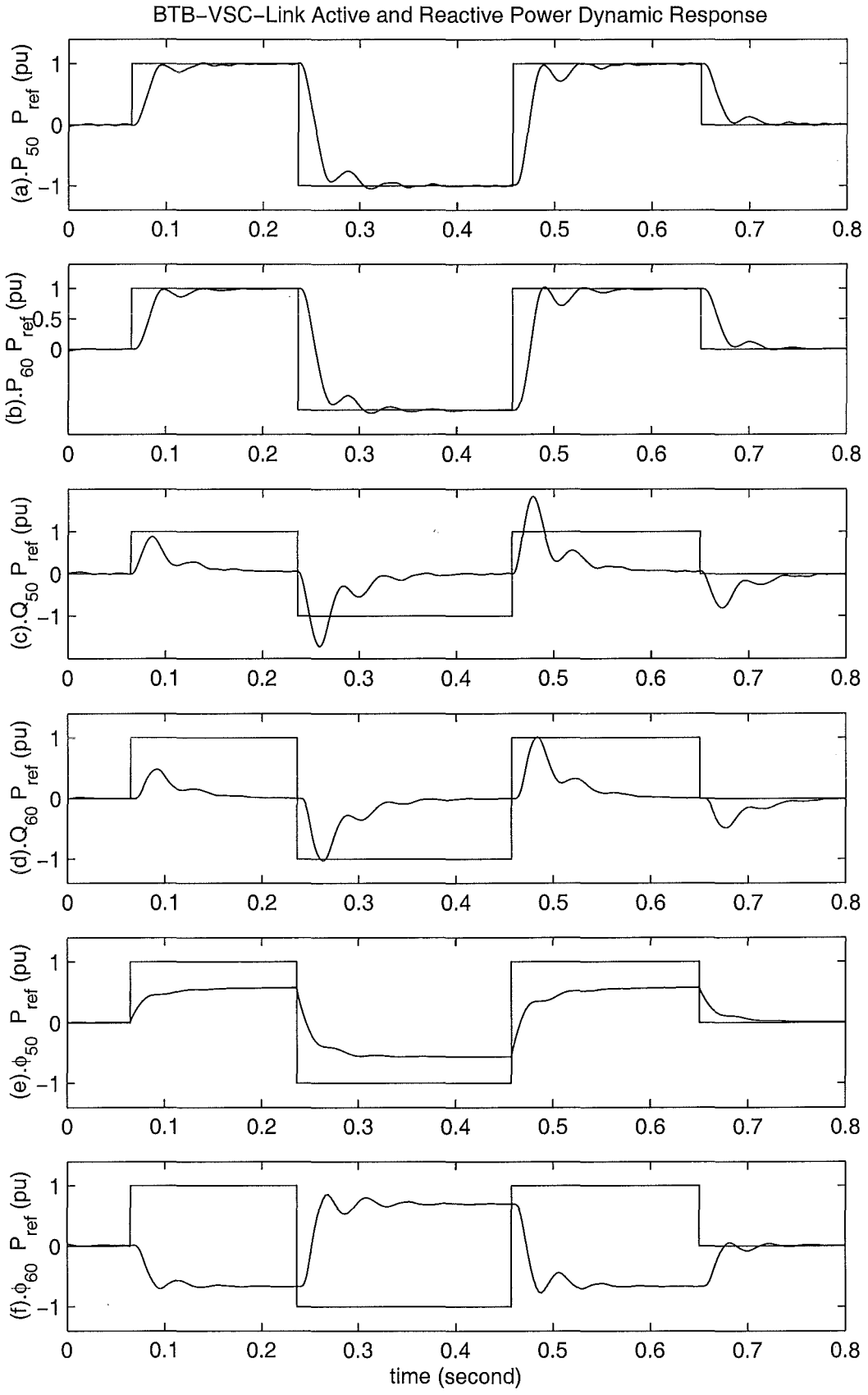


Figure 7.19 Active and Reactive Power Responses to Real Current Order

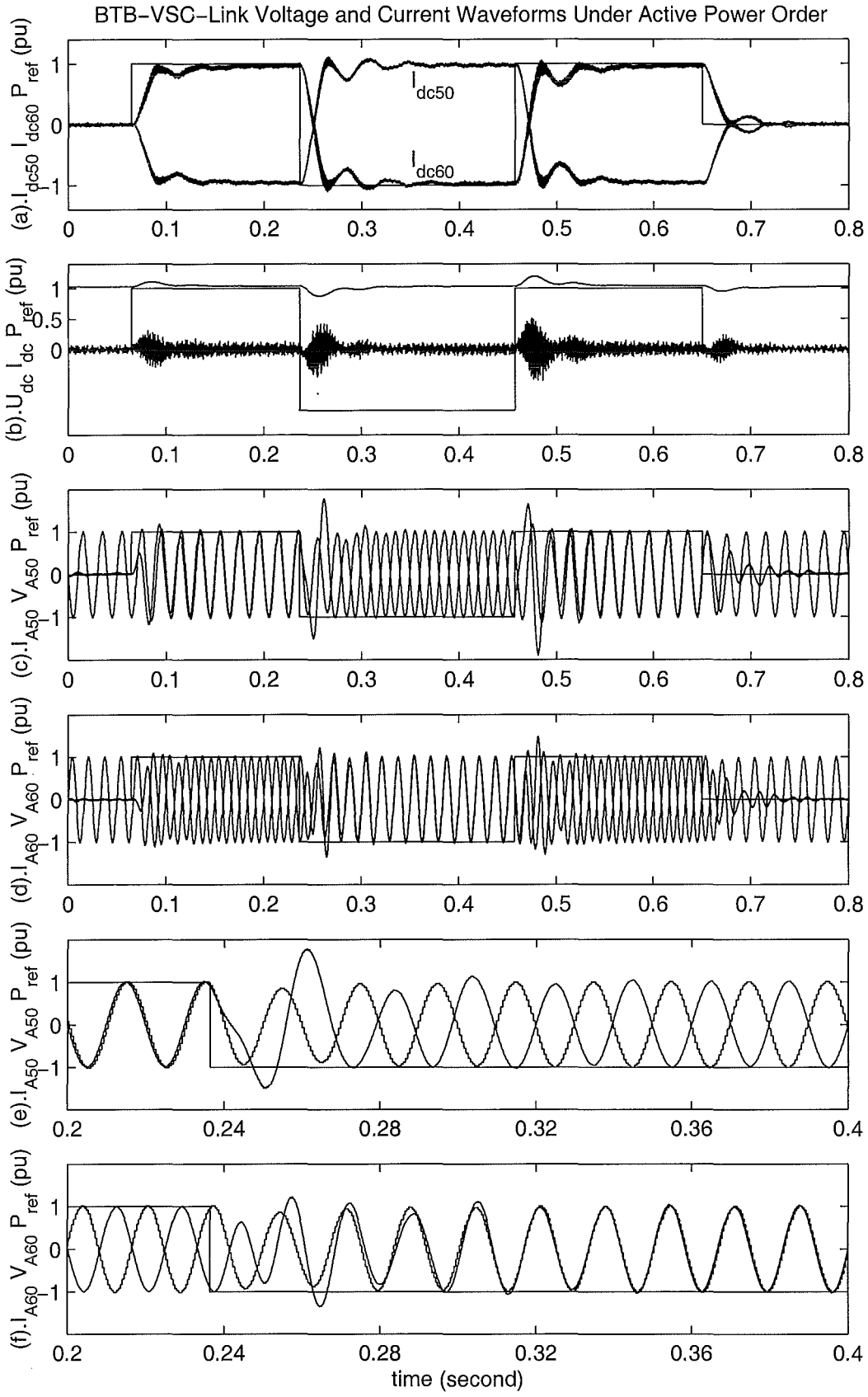


Figure 7.20 Voltage and Current Responses to Real Current Order

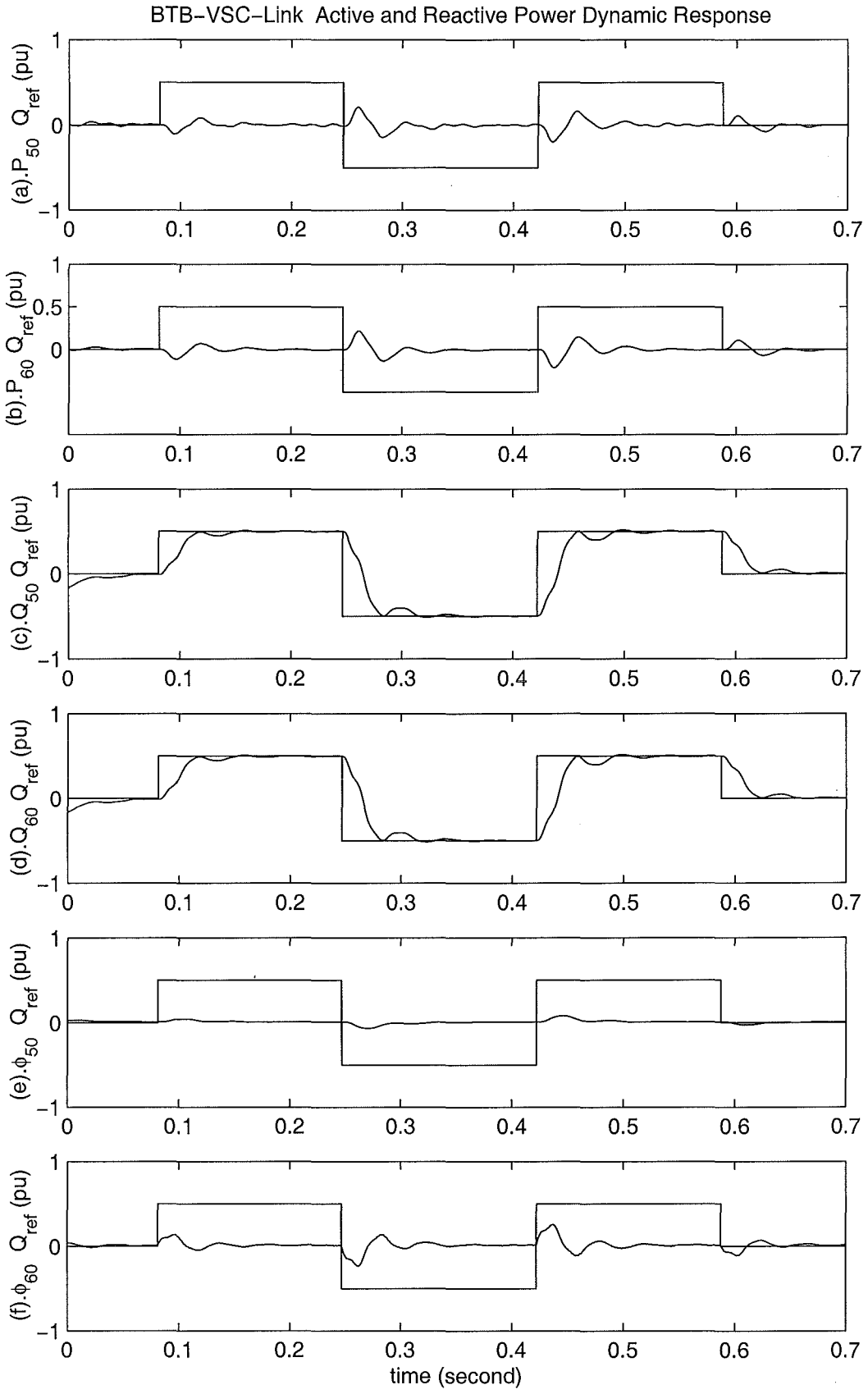


Figure 7.21 Real and Reactive Power Responses to Imaginary Current Order

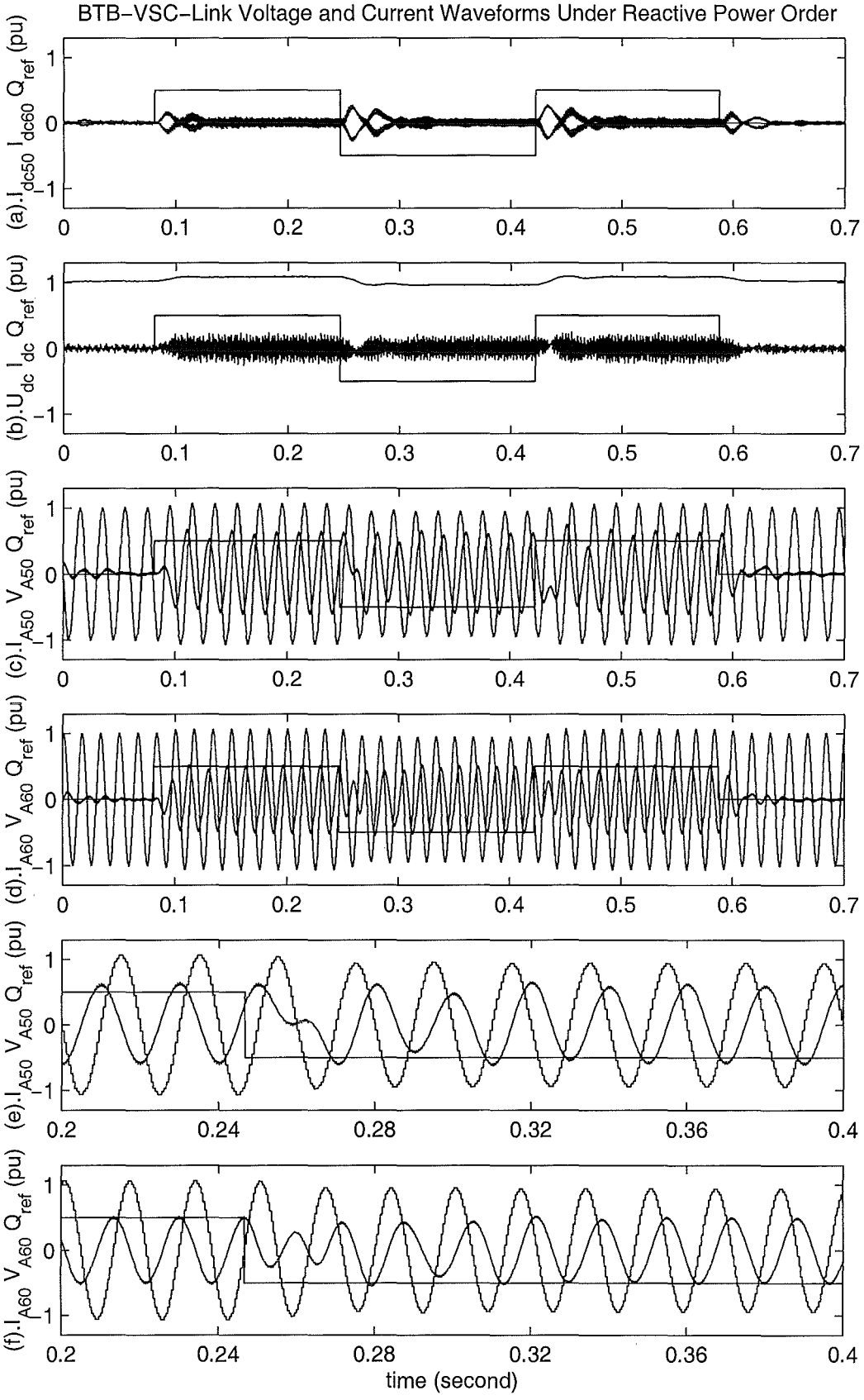


Figure 7.22 Voltage and Current Responses to Imaginary Current Order

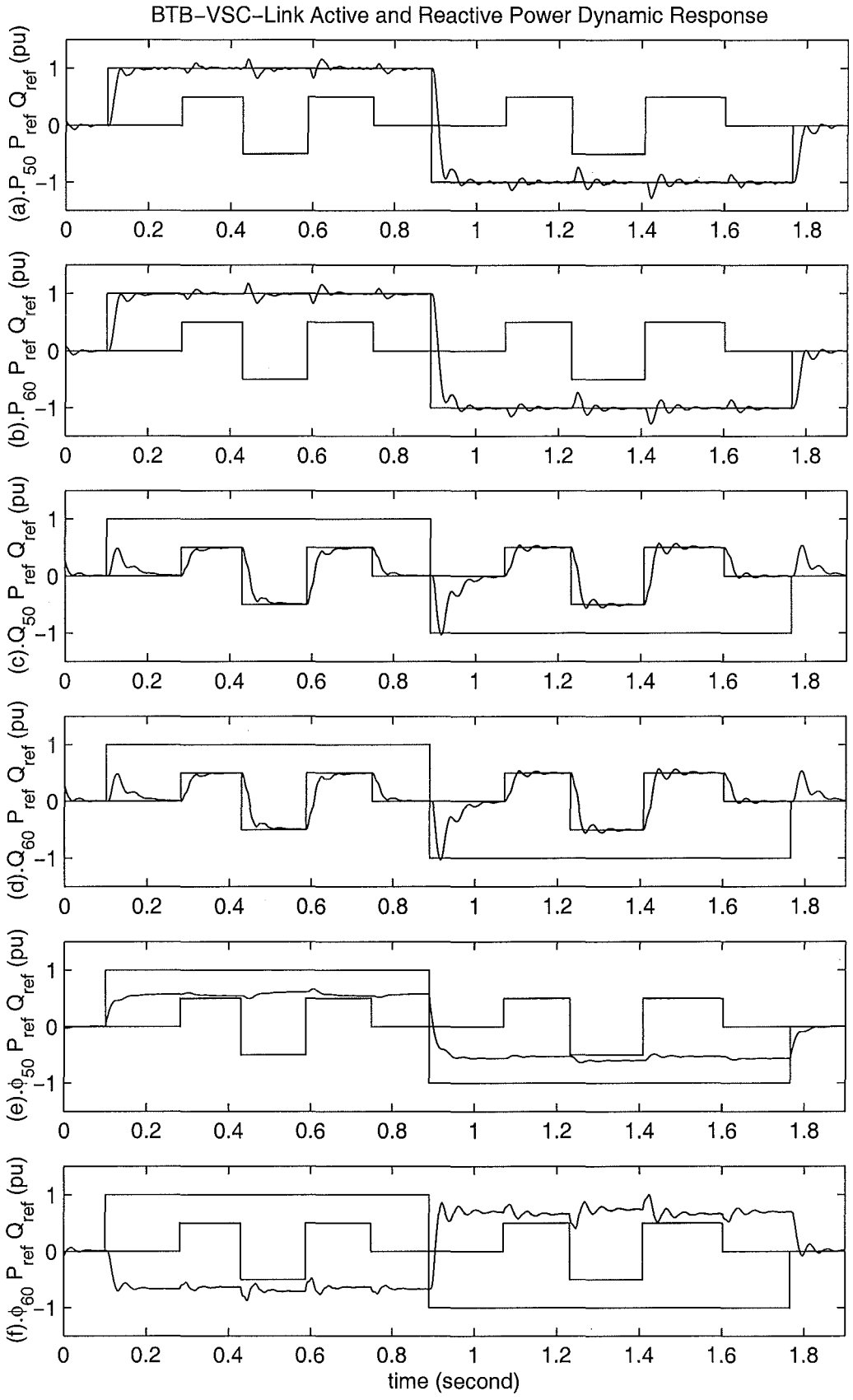


Figure 7.23 Real and Reactive Power Responses to I_{Re}&I_{Im} Current Orders

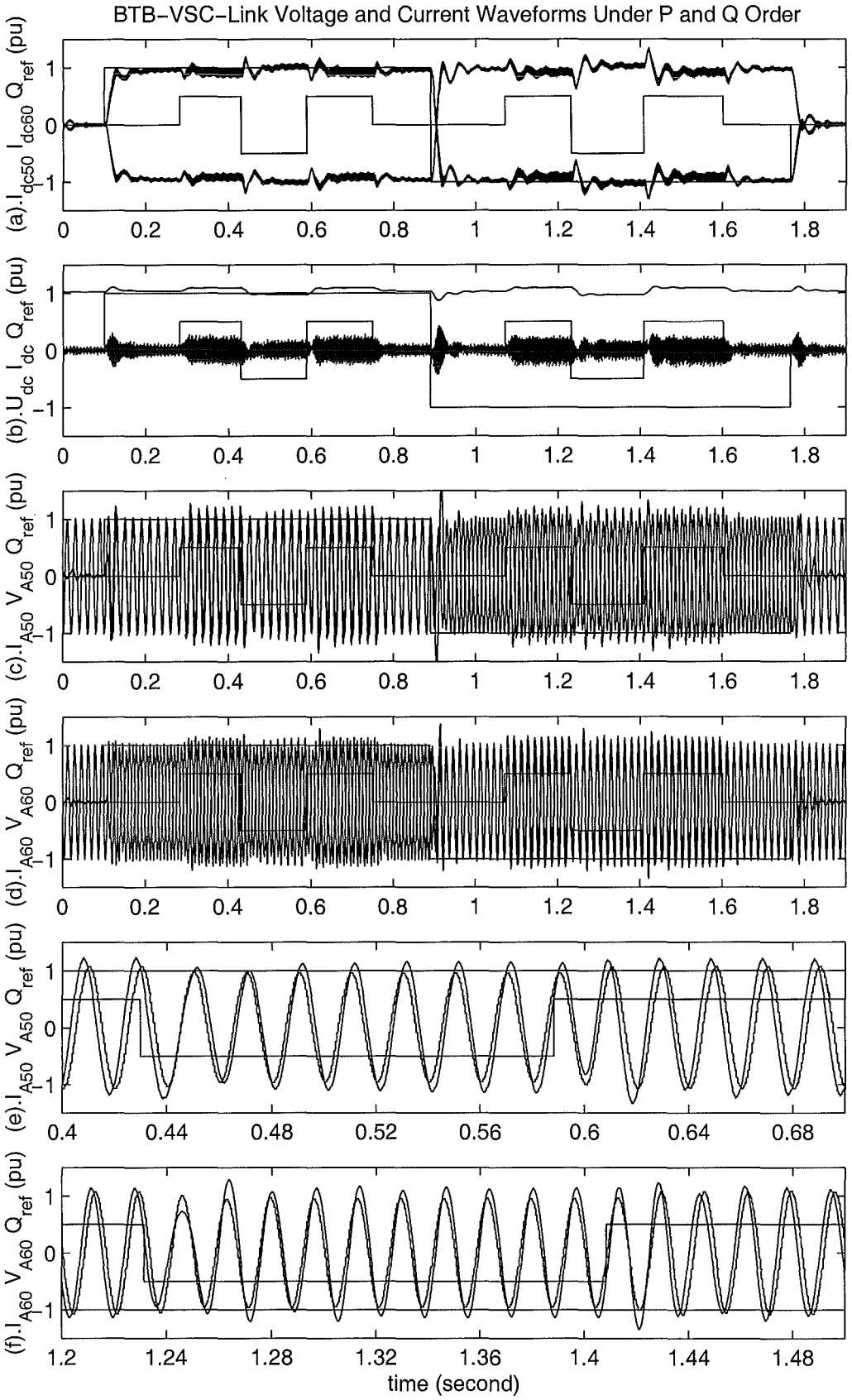


Figure 7.24 Voltage and Current Responses to I_{Re}&I_{Im} Current Orders

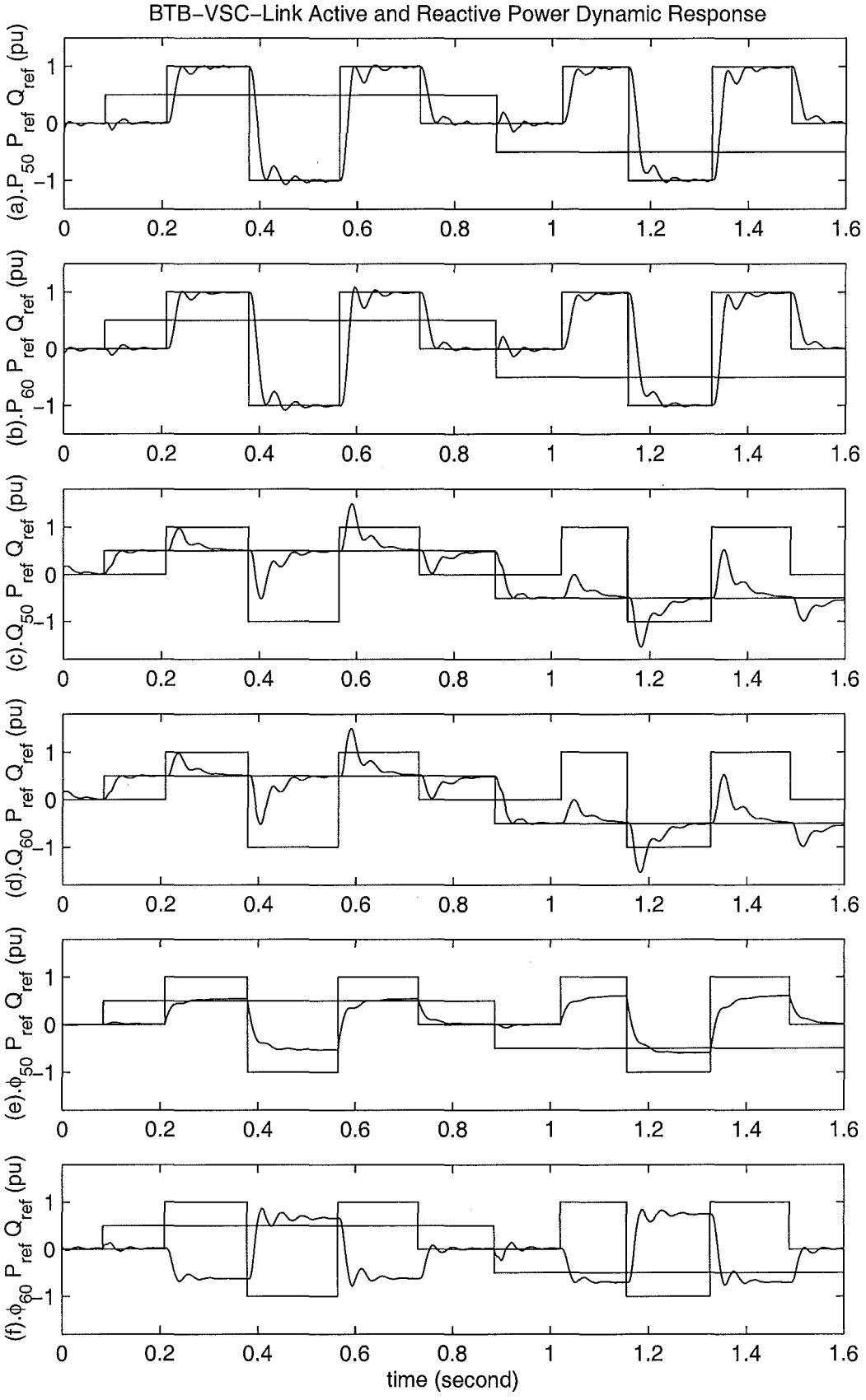


Figure 7.25 Real and Reactive Power Responses to I_{Re}&I_{Im} Current Orders

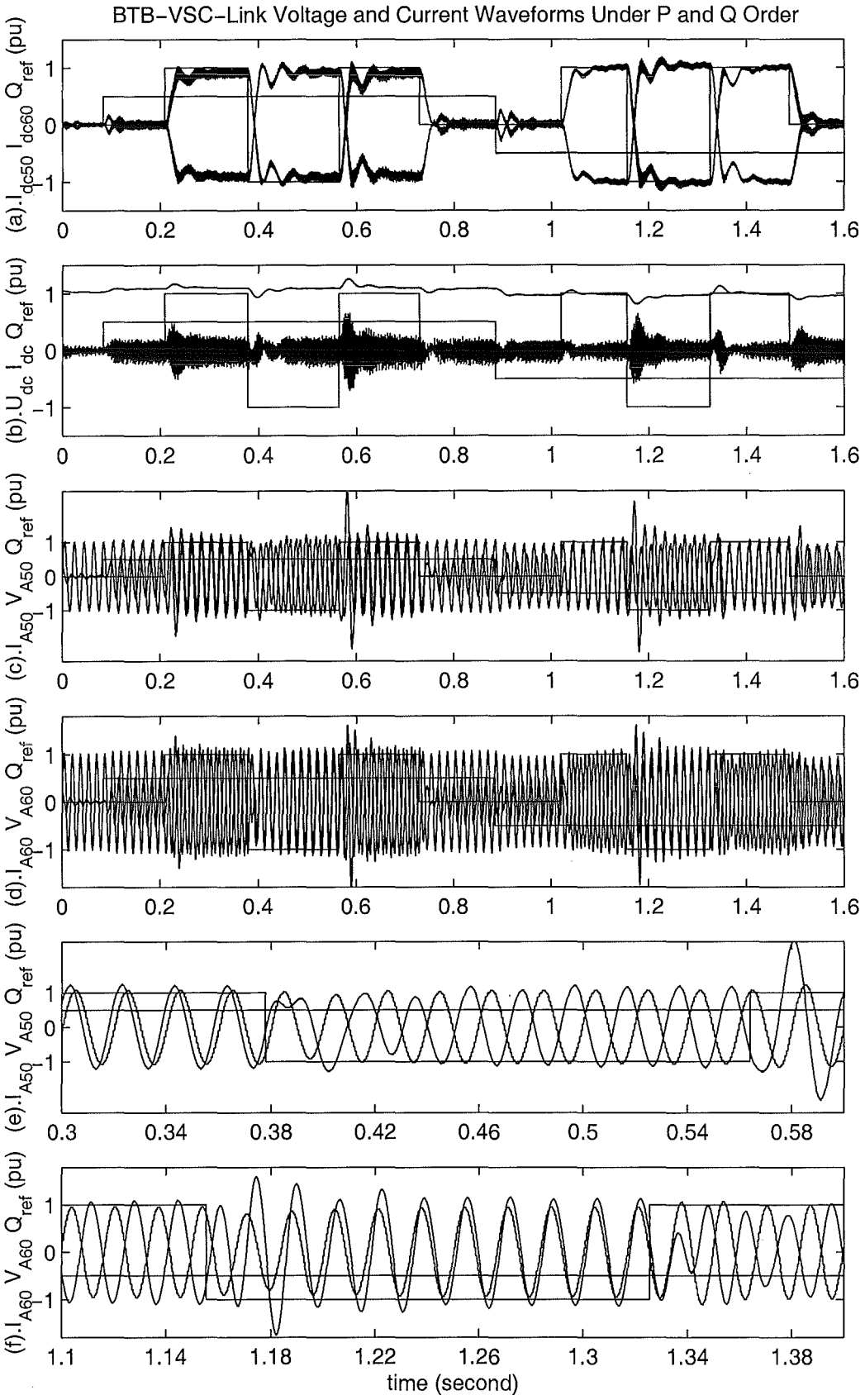


Figure 7.26 Voltage and Current Responses to I_{Re}&I_{Im} Current Orders

output currents and voltages complete the power transferring reversal process without significant over voltage or over current. These also show that the harmonic distortion is well under control.

C. Reactive Power Response

Figures 7.21 and 7.22 are arranged as those in Figures 7.19 and 7.20, and show the dual converter system's dynamic process under zero real current order and $\pm 0.5pu$ imaginary current order.

Again these waveforms show that the dynamic response of the reactive power is of high performance, as there is practically no overshoot and the dynamic process only lasts for about 2-3 cycles.

D. Active and Reactive Power Cross Influence

Figures 7.23 and 7.24 show the dual converter system dynamic process under ± 1 pu real current order, while the imaginary current order changes from 0 pu to 0.5 pu for 100ms, then to -0.5 pu for 100ms, to 0.5pu for another 100ms, and finally returning to 0pu. These waveforms show that the reactive power order changes cause some disturbance on the active power, but not significantly; i.e. the voltage and current over shoot caused by the reactive changes are small.

The plots in Figures 7.23, 7.24, 7.25, and 7.26 are arranged as those in Figures 7.19 and 7.20 respectively.

Figures 7.25 and 7.26 show the dual converter system dynamic process under the ± 0.5 pu imaginary current order while the real current order is changed from 0 pu to 1 pu for 100ms, then to -1 pu for 100ms, to 1 pu for another 100ms, and finally returning to 0pu. These waveforms show that the active power order changes cause significant disturbance on the reactive power, but only for a short period; the voltage and current over shoot caused by the active change is significant, particularly the current overshoot that can reach 1.5 pu.

7.4 SUMMARY OF THE SIMULATION STUDIES

7.4.1 Operation of the MLVR-VSC as a STATCOM

The MLVR-VSC for STATCOM application has been investigated by EMTDC simulations, the main conclusions being:

1. The MLVR-VSC can generate high pulse voltage waveforms with very low THD ($< 2.5\%$) using the fundamental switching frequency for the main bridges and 12 times that frequency for the reinjection switches.

2. The power switches in the main bridges can be connected in series without dynamic voltage balancing problems; the step by step increased and decreased output voltage reduces the dV/dt rating; the zero voltage switching condition reduces the main bridge switching losses and the snubber requirement. These characteristics makes the MLVR-VSC a suitable candidate for high power applications.

3. Functioning as a STATCOM the MLVR-VSC can provide full scale controllability of the capacitive and inductive power. With a full scale reactive power change the dynamic process can be completed in 40-60ms, and is therefore suited for compensation requiring fast response.

4. As well as generating reactive power, the MLVR-VSC can supply some dc real power to a dc load with a small fluctuation in the dc voltage. With active power exchange the dc capacitor voltage of the MLVR-VSC can be balanced by appropriate adjustment of the reinjection switch on-state interval.

5. For asymmetrical source conditions, if the source voltage asymmetry is not very large, the MLVR-VSC can operate normally, and even inject more capacitive current to the lower voltage phase or absorb less inductive current from the lower voltage phase.

6. Further study is needed to develop new control strategies to achieve symmetrical operation under asymmetrical source conditions.

7.4.2 ESEDS-VSC for BTB-VSC-Link

The asynchronous inte-connection of power systems through the dual Reinjection Voltage Source Converter has been investigated, and the main conclusions are:

1. The Reinjection Voltage Source Converter can generate multi-level voltage waveforms with about 5 percent Total Harmonic Distortion under the fundamental switching frequency for the main bridges and six times the fundamental switching frequency for the reinjection bridge. With a suitable value of the leakage reactance of the interface transformers the harmonic current injection into the power system can be reduced to meet strict standards.

2. Although independent amplitude control at both ends is not available, the dual converter system can operate under normal and to some degree fault conditions, to transfer active power bidirectionally between two separate system and to inject or absorb reactive power at both sides. However the reactive power injected into, or absorbed from, the two systems, can not be controlled independently.

3. Based on the proposed control structure and strategy, the dual converter system can respond quickly to track the operating condition order with satisfactory dynamic and steady state characteristics.

Chapter 8

MLCR CURRENT SOURCE CONVERTER

8.1 INTRODUCTION

As described in chapter 2 the multi-level reinjection concept can be applied to current source conversion. The Multi-Level Current Reinjection (MLCR) Current Source Converter (CSC) and MLVR-VSC can be viewed as dual topologies, i.e. current waveforms in MLCR-CSC are dual to the voltage waveforms in MLVR-VSC. In the MLCR-CSC the dc current is assumed constant, while the dc output currents of the two main bridges are variable, constituting multi-level current waveforms.

The MLCR-CSC requires switching devices of different characteristics from those of the MLVR-VSC. The MLVR-VSC requires asymmetrical switching devices (with unidirectional voltage blocking and bidirectional current passing capability), while the MLCR-CSC requires symmetrical switching devices (with bidirectional voltage blocking and unidirectional current passing capability). This requirement is based on the fact that the MLCR-CSC dc current is unidirectional while its dc voltage can reverse instantaneously due to the presence of the dc side inductance. Thus the IGBT can not by itself be used in the MLCR-CSC; a diode connected in series with the IGBT can solve the problem, but the extra power losses makes it unsuitable for high power applications. The symmetrical types GTO and IGCT are the appropriate switching devices for the MLCR-CSC high power configurations due to relatively lower switching frequency of the MLCR-CSC.

A comparison of the MLCR-CSC with the MLVR-VSC characteristics show the following important features:

1. The MLCR-CSC does not have high fault current, because the rise rate of fault current during external or internal faults is limited by the dc reactor, and thus the fault current can be suppressed by the converter control action. In the MLVR-VSC the capacitor charge or discharge current rises very rapidly during faults and thus the fault current can be high and then damage the switching devices.

2. The interface transformer of a six-pulse converter MLVR-VSC requires a path for the triple fluxes generated by triple harmonic voltage components. Such is not

the case with a six-pulse MLCR-CSC, which generates harmonic currents of triple orders, but not harmonic voltages of triple orders. For the 12-pulse MLVR-VSC the interface transformers have to be separated and connected in series, while for 12-pulse MLCR-CSC the two bridges can be powered by a common interface transformer with a set of primary windings and two sets of isolated secondary windings, which are connected to the two main bridges respectively. This reduces the cost of the interface transformers.

3. The MLCR-CSC does not generate high dV/dt output due to the provision of a zero current switching (ZCS) condition.

4. The MLCR-CSC zero current switching feature simplifies its interface with the ac system, because there is no need for a large interfacing ac capacitor to absorb the inductive energy stored in the ac system during the commutation period. The interfacing difficulty has been the main disadvantage of CSC as compared with VSC in the past.

5. The power losses in a dc reactor are much higher than those in a dc capacitor; however the size of the MLCR-CSC dc reactor can be reduced due to the high frequency voltage across the reactor (for a level number m, the dc voltage ripple frequency of the MLCR-CSC is $6(m-1)$ for a 6-pulse system and $12(m-1)$ for a 12-pulse system).

6. The risk of parallel resonance between the ac side inductance and the interface capacitors makes the CSC design difficult, however the MLCR-CSC ZCS condition offers high flexibility in the choice of capacitor to prevent the resonance frequency.

7. Corresponding to the VSC high over current during faults, in the MLCR-CSC over voltages can be caused during faults due to the high voltage across the dc reactor induced by the fault current.

8. The MLVR-VSC has great freedom of choice of power switching devices (i.e. IGBT or GTO), whereas the GTO (or IGCT) is the only appropriate choice for the MLCR-CSC.

For HVDC applications, both of the MLVR-VSC and MLCR-CSC can be used, though they offer different performance. In super-conductor magnetic energy storage system only the MLCR-CSC can be used to supply controllable dc current with full scale dc voltage control ability. This is due to the fact that VSC's can be used to control dc current for full range but small range of dc voltage, while CSC's can offer full range of control for both dc current and voltage.

The topological structures and the control strategies of the ripple reinjection concept [60, 64, 65, 66, 67], developed for the line commutated thyristor current source converters, can be adopted for self-commutated current source converters. Although self-commutation provides greater control flexibility and freedom, it also has difficulties for the current source converters, like switching dynamic voltage balance, switching losses, high di/dt and dv/dt $\cdots$. These need further study.

8.2 MLCR-CSC TOPOLOGICAL STRUCTURES

As for the MLVR-VSC, the reinjection currents can be formed in two ways: either an ac current adds to, and subtracts from, the dc current components to the two main bridges; or the dc current is appropriately distributed to the two main bridges.

Because the addition and subtraction of currents in a transformer can be made by appropriate connection of the windings, only an interface transformer is required. The reinjection currents to the two main bridges are derived by means of multi-winding reinjection transformers. In both cases the basic converter configuration can be of the 6-pulse or 12-pulse type.

8.2.1 MLCR-CSC Based on 6-Pulse System

A full 3-phase bridge can be treated as two half bridges connected in series, i.e. a common anode and common cathode groups. The common cathode group supplies the positive currents and the common anode group supplies the negative currents to the three phase windings of the interface transformer.

Figure 8.1 shows the conventional 6-pulse current source converter with the reinjection circuit included. The dc current circulates through the reinjection switches, the two reinjection transformers, smoothing reactor L_m and dc voltage source E_d. With a sufficiently large inductance (L_m), the dc current will remain constant. The dc current is chopped into a multi-level ac current waveform at 3 times the source fundamental frequency, and this ac current circulates through the secondary windings of the two reinjection transformers. This current is coupled to the reinjection transformer primary windings to shape the main bridge output currents I_{BP} and I_{BN} into the waveforms described in chapter 2.

Because the reinjection transformer winding current direction can be changed by the switching actions of the reinjection switches, a winding divided into $\frac{m}{2}$ portions with $\frac{m}{2}+1$ taps can be used to generate m-levels of the reinjection current; the addition of the two optional switches S_{pj0} and S_{nj0} provides an extra level, such that no reinjection current passes by the reinjection transformer windings. Thus the reinjection circuit in Figure 8.1 can generate (m+1)-level currents I_{BP} and I_{BN}.

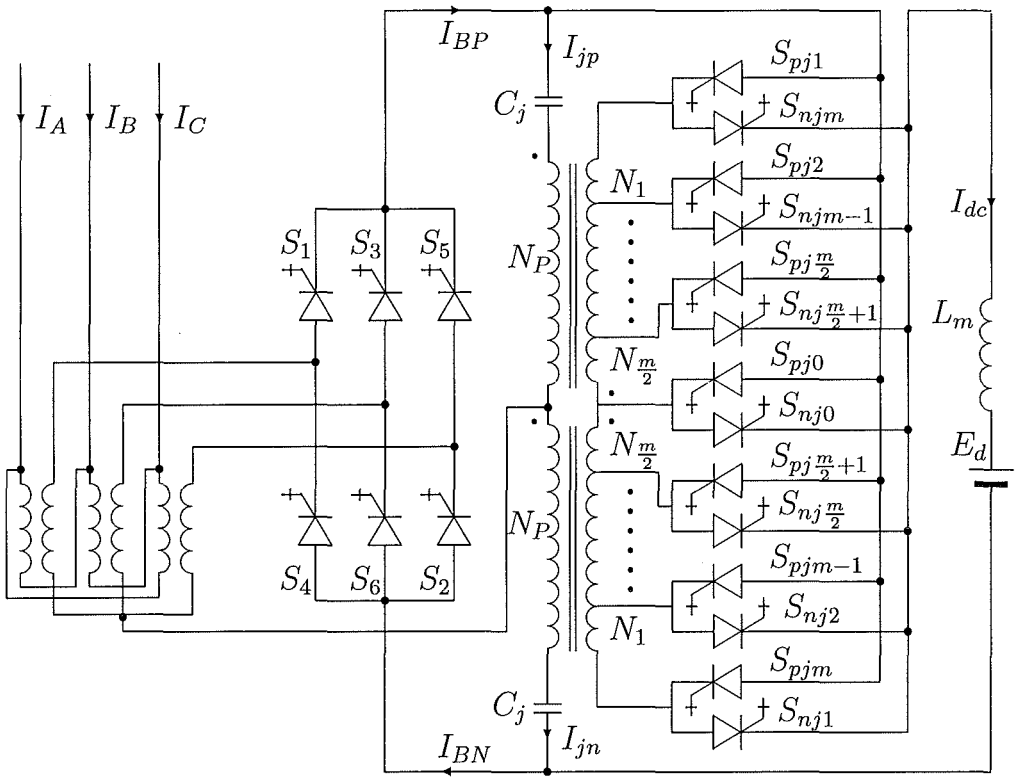


Figure 8.1 The Topological Structures of MLCR-CSC Based on 6-Pulse System

The (m+1)-level main bridge output currents, I_{BP} and I_{BN}, are formed by the switching combinations, shown in tables 8.1 and 8.2.

Tables 8.1 and 8.2 give the corresponding relationships between the (m+1)-levels of currents I_{BP} and I_{BN}, the required reinjection switches in ON-state, the windings connections of the reinjection transformers and the currents I_{jp} and I_{jn} used to shape the dc output currents I_{BP} and I_{BN}.

The winding connections of the reinjection transformers in Figure 8.1 ensures that $I_{jn} = -I_{jp}$ and the main bridge output currents are formed by I_{dc}, I_{jp} and I_{jn}, i.e. $I_{BP} = I_{dc} + I_{jp}$ and $I_{BN} = I_{dc} + I_{jn} = I_{dc} - I_{jp}$. Because I_{jp} and I_{jn} are determined by the turns ratio of the reinjection transformers, the main bridge output currents I_{BP} and I_{BN} can be shaped into the required multi-level forms from constant dc by selecting the appropriate winding turns ratio. The required current waveforms I_{BP} and I_{BN}, are synchronized with the firing control of the main bridge switches, therefore by supplying the required reinjection current waveforms the converter output current waveforms are also shaped into the expected waveforms.

The three-phase half-bridge 6-pulse configuration connected to the load via a multi-tapped balancing reactor was used to describe the implementation of the ripple reinjection concept in the current source converter [59, 62]. A modified configuration for self-commutated switching converters is shown in Figure 8.2 to implement the multi-

Table 8.1 Switching Combinations and Multi-level Reinjection Current

ON-State Switches	I_{BP}	Winding Combinations (P-group)	I_{jp}
S_{pj1} and S_{nj1}	I_{Lm}	$N_{S1} = N_1 + N_2 + \cdots + N_{\frac{m}{2}}$	$\frac{N_{S1}}{N_P} I_{dc}$
S_{pj2} and S_{nj2}	I_{Lm-1}	$N_{S2} = N_2 + N_3 + \cdots + N_{\frac{m}{2}}$	$\frac{N_{S2}}{N_P} I_{dc}$
...	...	...	...
$S_{pj\frac{m}{2}}$ and $S_{nj\frac{m}{2}}$	$I_{L\frac{m}{2}+1}$	$N_{S\frac{m}{2}} = N_{\frac{m}{2}}$	$\frac{N_{S\frac{m}{2}}}{N_P} I_{dc}$
S_{pj0} and S_{nj0}	I_{dc}	$N_{S0} = 0$	0
$S_{pj\frac{m}{2}+1}$ and $S_{nj\frac{m}{2}+1}$	$I_{L\frac{m}{2}}$	$N_{S\frac{m}{2}} = N_{\frac{m}{2}}$	$-\frac{N_{S\frac{m}{2}}}{N_P} I_{dc}$
...	...	...	...
S_{pjm-1} and S_{njm-1}	I_{L2}	$N_{S2} = N_{\frac{m}{2}} + \cdots + N_3 + N_2$	$-\frac{N_{S2}}{N_P} I_{dc}$
S_{pjm} and S_{njm}	I_{L1}	$N_{S1} = N_{\frac{m}{2}} + \cdots + N_2 + N_1$	$-\frac{N_{S1}}{N_P} I_{dc}$

Table 8.2 Switching Combinations and Multi-level Reinjection Current

ON-State Switches	I_{BN}	Winding Combinations (N-group)	I_{jn}
S_{pj1} and S_{nj1}	I_{L1}	$N_{S1} = N_{\frac{m}{2}} + \cdots + N_2 + N_1$	$-\frac{N_{S1}}{N_P} I_{dc}$
S_{pj2} and S_{nj2}	I_{L2}	$N_{S2} = N_{\frac{m}{2}} + \cdots + N_3 + N_2$	$-\frac{N_{S2}}{N_P} I_{dc}$
...	...	...	...
$S_{pj\frac{m}{2}}$ and $S_{nj\frac{m}{2}}$	$I_{L\frac{m}{2}}$	$N_{S\frac{m}{2}} = N_{\frac{m}{2}}$	$-\frac{N_{S\frac{m}{2}}}{N_P} I_{dc}$
S_{pj0} and S_{nj0}	I_{dc}	$N_{S0} = 0$	0
$S_{pj\frac{m}{2}+1}$ and $S_{nj\frac{m}{2}+1}$	$I_{L\frac{m}{2}+1}$	$N_{S\frac{m}{2}} = N_{\frac{m}{2}}$	$\frac{N_{S\frac{m}{2}}}{N_P} I_{dc}$
...	...	...	...
S_{pjm-1} and S_{njm-1}	I_{Lm-1}	$N_{S2} = N_2 + N_3 + \cdots + N_{\frac{m}{2}}$	$\frac{N_{S2}}{N_P} I_{dc}$
S_{pjm} and S_{njm}	I_{Lm}	$N_{S1} = N_1 + N_2 + \cdots + N_{\frac{m}{2}}$	$\frac{N_{S1}}{N_P} I_{dc}$

level ESEDS or Linear reinjection alternatives with zero current switching condition.

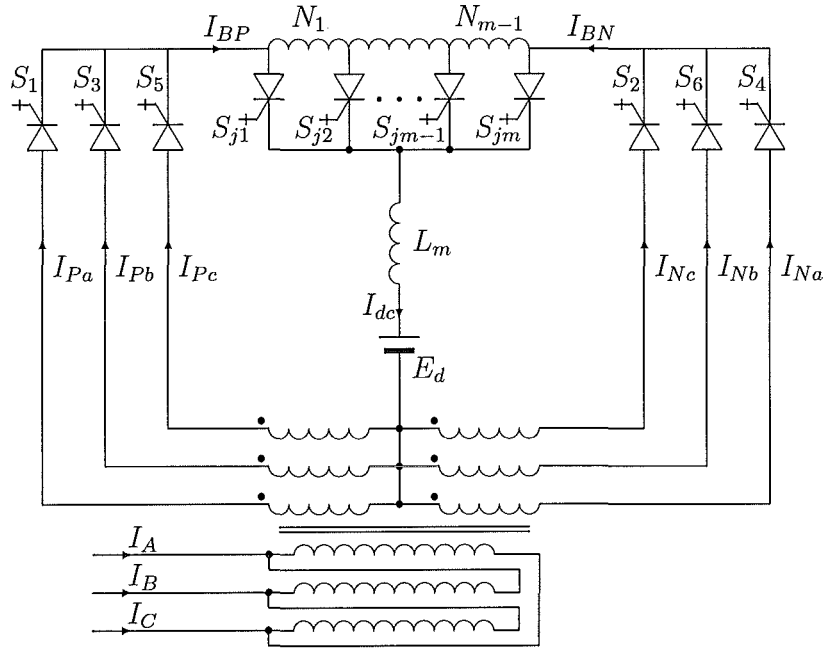


Figure 8.2 The Topological Structures of MLCR-CSC Based on 6-Pulse System

In Figure 8.2 the multi-tapped balancing reactor assisted by the reinjection switches, functions as a controllable dc current distributor in a similar way as the series connected capacitors of the controllable voltage divider in MLVR-VSC. In the presence of a sufficient large inductance of the multi-tapped reactor, when the k^{th} tap of the reactor is connected to the load (consisting of L_m and E_d) by the reinjection switch S_{jk}, the following ampere-turns balance results:

$$I_{BP}(N_1 + N_2 + \cdots + N_{k-1}) = I_{BN}(N_k + N_{k+1} + \cdots + N_m) \tag{8.1}$$

From the circuit in Figure 8.2 the relation between the currents I_{dc}, I_{BP} and I_{BN} can be directly written as $I_{BP} + I_{BN} = I_{dc}$, and combining this expression with Equations 8.1, then I_{BP} and I_{BN} can be expressed as follows

$$I_{BP} = \frac{(N_k + N_{k+1} + \cdots + N_m)}{(N_1 + N_2 + \cdots + N_m)} I_{dc} \tag{8.2}$$

$$I_{BN} = \frac{(N_1 + N_2 + \cdots + N_{k-1})}{(N_1 + N_2 + \cdots + N_m)} I_{dc} \tag{8.3}$$

These two equations indicate that by proper selection of the tap positions and control of the reinjection switches to on-state at the appropriate time intervals, the dc current I_{dc} can be distributed to the two bridges with the required waveforms.

Figures 2.17 and 2.18 illustrate the current waveforms and output current spectrum of a 5-level MLCR-CSC example based on 6-pulse systems for ESEDS and Linear

reinjection respectively.

8.2.2 MLCR-CSC Based on 12-Pulse System

The 12-pulse line-commutated current source thyristor converters are widely used for different applications. The natural commutation requirement makes them consume large reactive power and operate improperly when they are connected to a weak ac system. Current source converters based on self-commutation offer many advantages for a variety of applications.

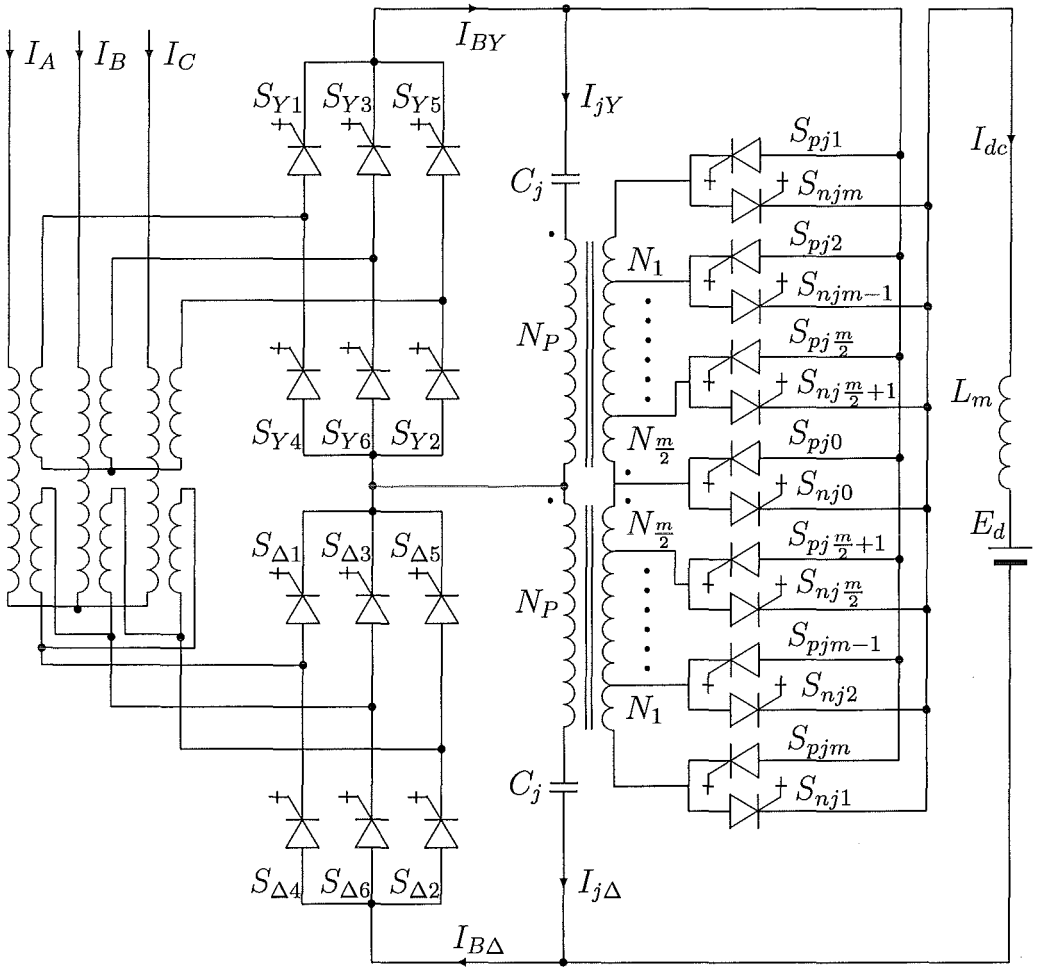


Figure 8.3 The Topological Structures of MLCR-CSC Based on 12-Pulse System

Figure 8.3 shows the (m+1)-level MLCR-CSC configuration based on the 12-pulse series connected converter. The two bridge output currents I_{BY} and $I_{B\Delta}$ (normally constant dc currents) are shaped by the reinjection currents I_{jY} and $I_{j\Delta}$ into (m+1)-level current waveforms and to produce 12m-pulse equivalent output current waveforms at the interface transformer primary (source side) terminals. The operating principle of the reinjection circuit is almost the same as that of the 6-pulse full-bridge configuration,

except that the reinjection switching frequency is increased from 6 to 12 times the source fundamental frequency.

Figure 8.4 shows the (m+1)-level MLCR-CSC configuration based on the 12-pulse parallel connected converter. The multi-tapped reactor assisted by the switching action of the reinjection switches, distributes the dc current I_{dc} to the two bridges in (m+1)-level waveforms as described in chapter 2.

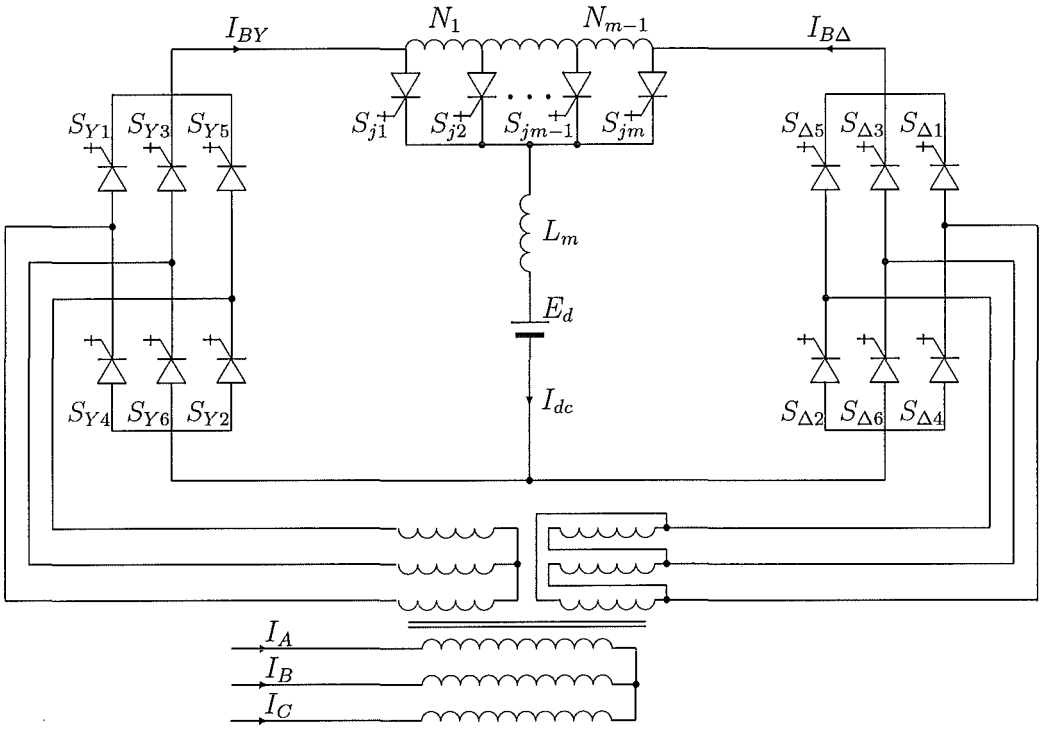


Figure 8.4 The Topological Structures of MLCR-CSC Based on 12-Pulse System

This is almost the same as the 6-pulse two half-bridge configuration in Figure 8.2, except in that the reinjection switching frequency is now increased from 6 to 12 times the source fundamental frequency.

Although the waveforms and the output spectra in Figures 2.10 and 2.11 (for an example of 21-level MLVR-VSC) refer to voltage, using the duality relation between the MLVR-VSC and MLCR-CSC in terms of voltage and current waveforms, they can also be treated as current waveforms and output current spectra; hence waveforms of MLCR-CSC, based on the 12-pulse systems for multi-level ESEDS and Linear reinjection approximations respectively.

8.3 MLCR-CSC STATCOM

Although current source converters based on line-commutated thyristors are used extensively, the self-commutated current source converter has not been adequately inves-

tigated. Most FACTS devices use voltage source converters. The MLCR-CSC concept overcomes the main disadvantages of present self-commutated current source converters. Moreover the direct current control, flexible power-factor adjustment and zero current switching features make the MLCR-CSC a suitable alternative for STATCOM application.

This section uses EMTDC simulation to investigate the potential of a 5-level MLCR-CSC (shown in Figure 8.5) to function as a STATCOM.

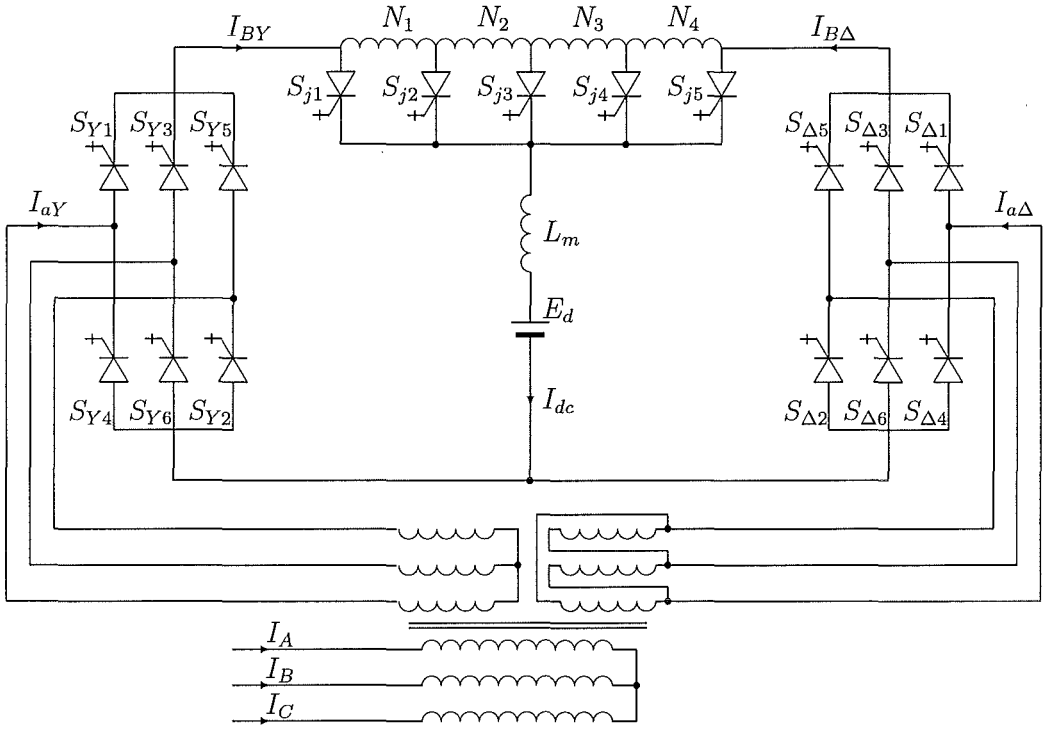


Figure 8.5 The 5-level MLCR-CSC for STATCOM application

The configuration in Figure 8.5 uses a multi-tapped reactor to distribute the dc current and produce the reinjection current waveforms for the two main bridges. To achieve the zero current switching condition, based on the linear reinjection waveforms derived in chapter 2, the taps of the multi-tapped reactor are arranged as $N_1 = N_2 = N_3 = N_4$. With sufficient inductance of the multi-tapped reactor the excitation current can be limited to a very low level; thus when the S_{j1} is fired to on state (all other reinjection switches being off state), the load current I_{dc} is supplied by the Y connection bridge and only a very small excitation current will flow through the Δ connection bridge. Vice versa when only the S_{j5} is fired to on state, practically no dc current passes through the Y connection bridge. These near zero current conditions are provided to the Y or Δ connection bridge switches to achieve the zero current switching.

Unlike Voltage Source Conversion, where equal size capacitors are required to share the dc voltage, the taps of the reactor can be arranged more flexibly to improve the

ac output current waveforms. For the 5-level case under the symmetrical reinjection waveform restriction and zero current switching requirement only the taps connected to S_{j2} and S_{j4} can be adjusted and $N_1 = N_4$ must be satisfied to ensure that the two bridge dc side currents are the same in shape but with a 30^o phase displacement. Because the linear reinjection waveform is very closed to the optimized ESEDS reinjection waveform for the 12-pulse reinjection configuration, in practice there is no need to modify the linear reinjection waveform, and thus the multi-tapped reactor remains an equal turns arrangement.

The configuration in Figure 8.5 has no any special requirement for the interface transformer, which is a common power transformer with three windings per phase and approximately 5% nominal leakage reactance. As for the conventional 12-pulse converters the turns ratio of the interface transformer are: $k_n : 1$ (primary to secondary) for the Y connection and $k_n : \sqrt{3}$ (primary to secondary) for the Δ connection.

A dc source E_d is added to the load branch for simulation flexibility, to permit real power transfer from the dc side to the ac source. For the STATCOM application, however, E_d is set to zero.

The dc reactor L_m in the load branch is needed to limit the fluctuation of the dc current I_{dc}. The dc output voltage of the 5-level MLCR-CSC in Figure 8.5 is equivalent to that of a 48-pulse converter. Under symmetrical source voltage conditions, as the dc voltage ripple is of low amplitude and high frequency the required inductance L_m is very low to suppress the dc current fluctuation; under asymmetrical source conditions, however a relatively large inductance L_m is required to limit the dc current ripple and achieve sufficient ac current waveform quality. With reference to the dynamic performance, a higher reactor inductance will reduce the current over-shoot when the converter system changes its operating condition from inductive to capacitive or vice versa.

As the switches in the two main bridges of the 5-level MLCR-CSC are fired under Zero Current Switching (ZCS) conditions, the techniques used in thyristor based converters for ensuring steady and dynamic voltage balancing can also be applied to the MLCR-CSC. Also the unidirectional nature of the current in every arm simplifies the snubber circuit design. Thus the direct series connection of power switches can be used without difficulties to construct reliable high voltage valves as required in the high power MLCR-CSC.

The reinjection switches S_{j1} to S_{j5} in Figure 8.5 are used to control the dc current distribution and the dc output current waveforms of the two main bridges. As the ZCS condition does not apply to them, a snubber circuit has to be used for each switch. However because only unidirectional currents pass through these switches, the snubbers can be of the simple and effective RCD (Resistor, Capacitor and Diode) type.

To verify the MLCR-CSC theoretical waveforms and investigate its use as a STATCOM, a EMTDC model is constructed and tested for the configuration in Figure 8.5 under

the following conditions: rated at 100MVA (each main bridge rating being 50MVA) and 100kV voltage; the interface transformer nominal impedance k_s is 10%; the multi-tapped reactor ratings are 25MVA and 68kV, its basic operation frequency being 300Hz (i.e. 6 times of the source fundamental frequency); the load branch inductance L_m is set to 2 Henry and the dc source E_d to 0V and 1Ω.

8.3.1 MLCR-CSC Waveform Verification

Figures 8.6 and 8.7 show the simulated waveforms corresponding to the generation of 1pu inductive and capacitive reactive powers respectively. The current waveforms in Figures 8.6 and 8.7 are

- (a) I_{BY} is the Y connection bridge dc output current, the nominal base being the dc current I_{dc}.
- (b) $I_{B\Delta}$ is the Δ connection bridge dc output current, the nominal base being the dc current I_{dc}.
- (c) I_{aY} is the normalized ac output current of the Y connection bridge, the nominal base being the dc current I_{dc}.
- (d) $I_{a\Delta}$ is the normalized ac output current of the Y connection bridge, the nominal base being the dc current I_{dc}.
- (e) I_A is the normalized ac output current of the MLCR-CSC, the nominal base being the primary side reflection $k_n I_{dc}$ of the dc current from the secondary side.
- (f) I_{An}/I_{A1} is the output current spectrum of the MLCR-CSC.

These waveforms are almost identical to the previously derived theoretical waveforms in chapter 2. The simulated output current THD is 4.05% and 4.29% for the capacitive and inductive operation respectively, while the theoretical value was 3.99% for the 5-level linear reinjection CSC (listed in Table 2.1). These differences are mainly caused by the snubber circuits of the reinjection switches, because these circuits absorb the leakage inductance energy and turn it into capacitive energy during switching transition. Thus the current waveforms in Figures 8.6 and 8.7 are slightly different from the theoretical step waveforms.

The waveforms of the two main bridge dc output currents I_{BY} and $I_{B\Delta}$ in Figures 8.6 and 8.7 clearly show that they vary with a frequency 6 times the source fundamental frequency, and that the commutations of the main bridge switches occur in the middle of the 6 zero current periods of about 416μs duration. Thus no switching disturbances are observed either in the source voltage V_{As} or current waveforms shown in Figures 8.6 (e) and 8.7 (e).

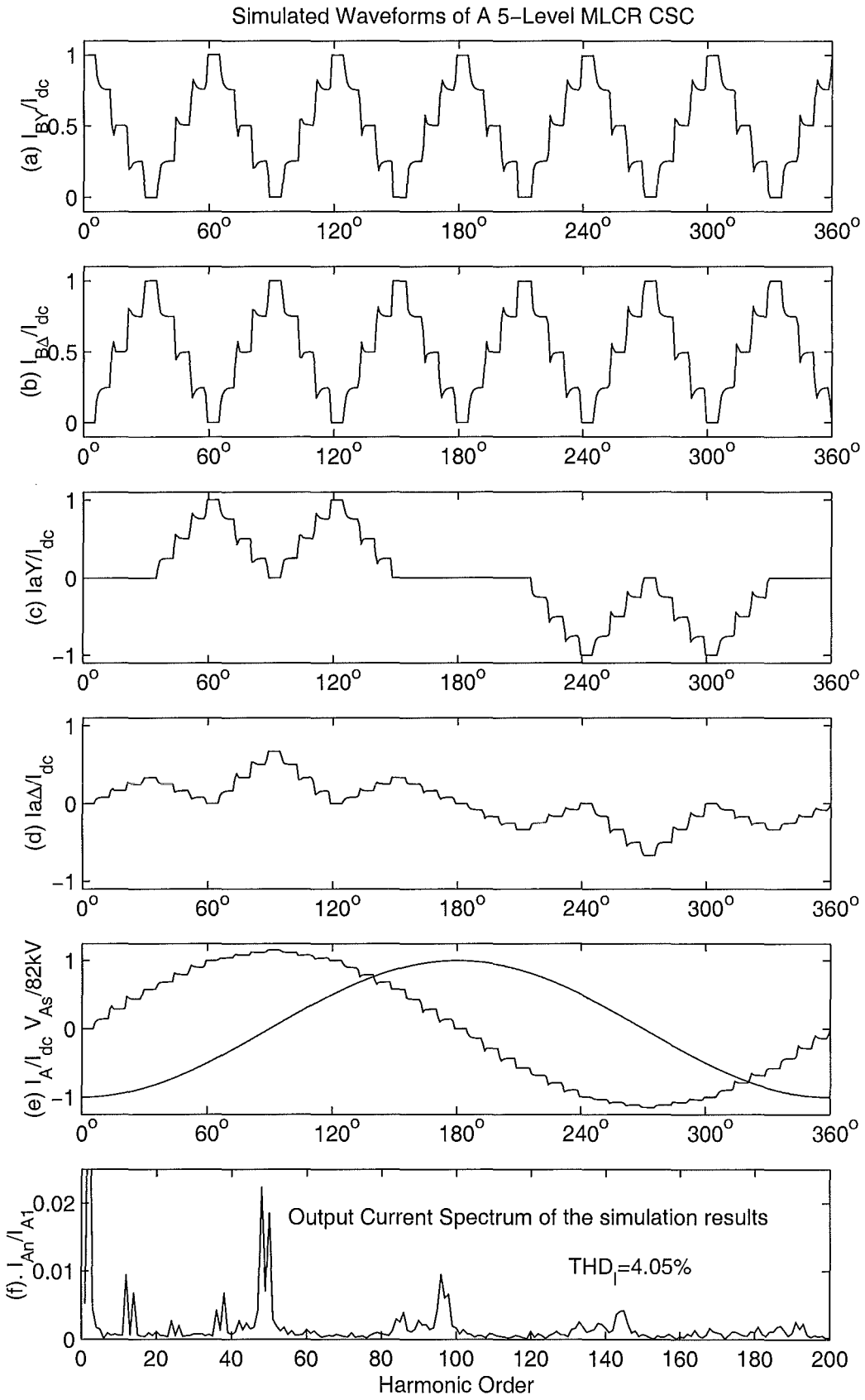


Figure 8.6 The Simulated Waveforms of The 5-Level MLCR-CSC (leading)

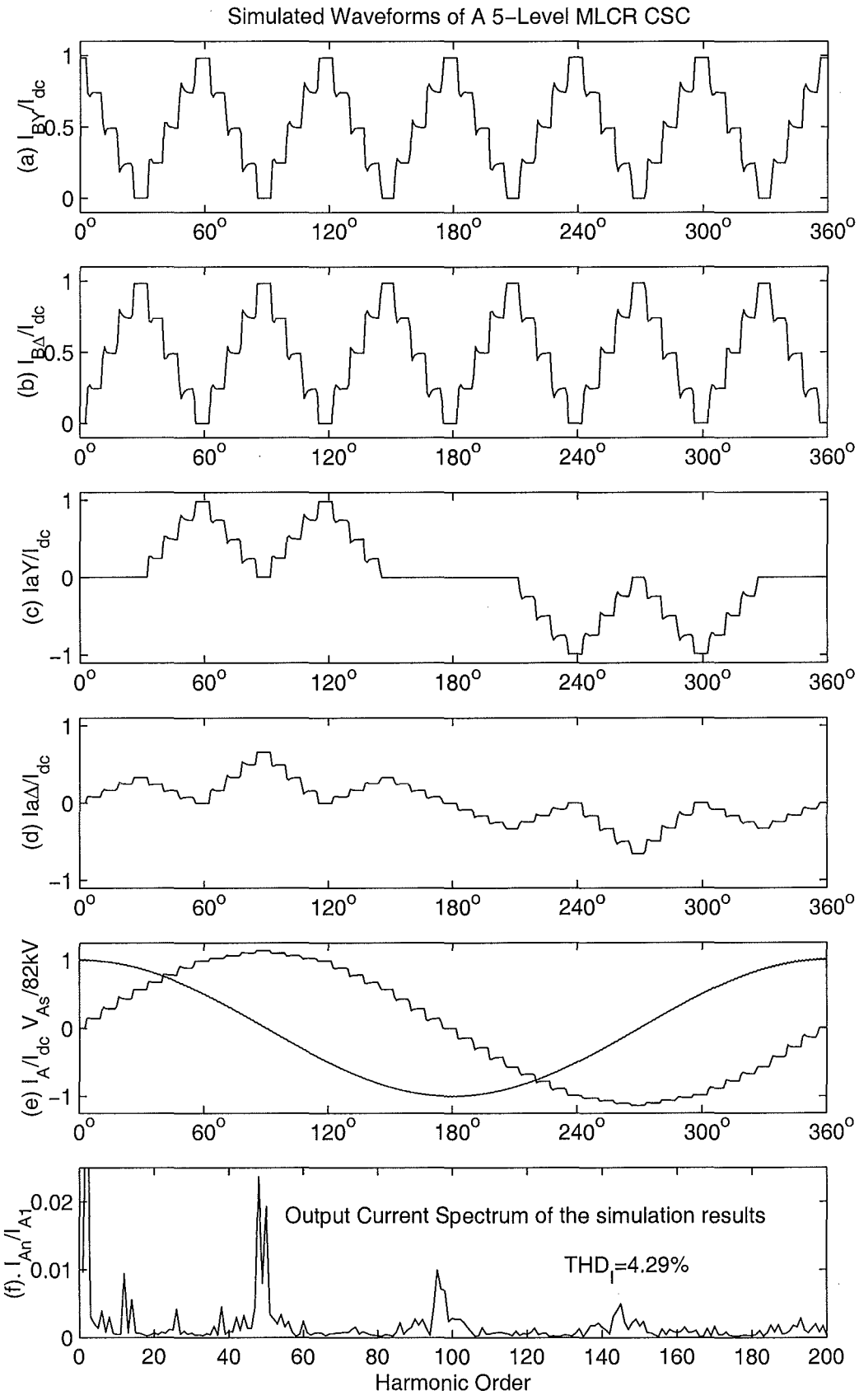


Figure 8.7 The Simulated Waveforms of The 5-Level MLCR-CSC (lagging)

8.3.2 STATCOM Operation

The basic control structures of the MLCR-CSC for the control of real-reactive power and real-imaginary current components are shown by the block diagrams of Figures 8.8 and 8.9 respectively. Unlike the case of PWM firing control, due to the fundamental frequency switching nature of the MLCR-CSC there is no independent amplitude and power angle control. There are only two control parameters in the MLCR-CSC case, i.e. I_{dc}, the dc load branch current and θ, the power angle of the MLCR-CSC system.

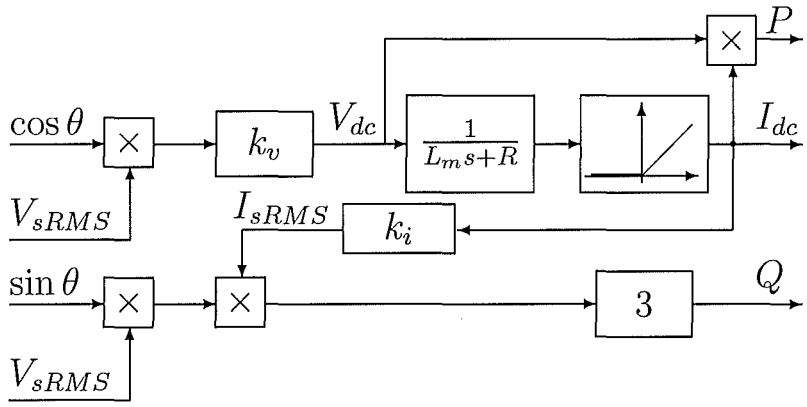


Figure 8.8 MLCR-CSC Block Diagram for Control of Real & Reactive Power

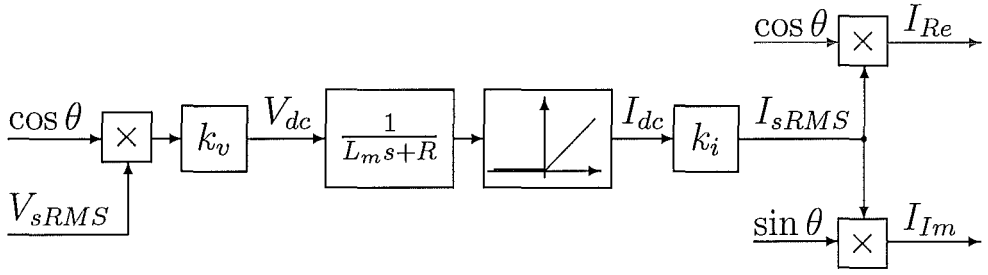


Figure 8.9 MLCR-CSC Block Diagram for Control Real & Imaginary Current

For many practical applications the real and reactive power or real and imaginary components of the ac output current can be thought of as the variables to be controlled, but the only variable that controls MLCR-CSC operation is the power angle θ; this is similar to the case of the MLVR-VSC, where ϕ, the phase angle differences between the converter output voltages and the source voltage, is the unique control variable. To obtain four quadrant operation the power angle θ has to vary in the range of $-180^o < \theta < 180^o$ while in the MLVR-VSC case ϕ can only be varied within a very small range. Therefore it is much more difficult for the MLCR-CSC to achieve four quadrant operation than in the MLVR-VSC, due to the large range of power angle variation, thus making the MLCR-CSC a very nonlinear system. The nonlinearities between θ and $[P \;\; Q]$ or $[I_{Re} \;\; I_{Im}]$ can be derived from the block diagrams in Figures 8.8 and 8.9:

In the MLCR-CSC case

$$P = V_{dc}I_{dc} = \frac{k_v^2 V_{sRMS}^2 \cos(\theta)|\cos(\theta)|}{L_m s + R} \tag{8.4}$$

$$Q = -3V_{sRMS}\sin(\theta) \cdot k_i I_{dc} = -\frac{3k_v k_i V_{sRMS}^2 \sin(\theta)|\cos(\theta)|}{L_m s + R} \tag{8.5}$$

$$I_{Re} = \frac{k_v k_i V_{sRMS}\cos(\theta)|\cos(\theta)|}{L_m s + R} \tag{8.6}$$

$$I_{IM} = -\frac{k_v k_i V_{sRMS}\sin(\theta)|\cos(\theta)|}{L_m s + R} \tag{8.7}$$

To overcome the difficulty of controlling the nonlinear MLCR-CSC for STATCOM application, a small variation of power angle $\Delta\theta$ from $\pm 90^o$ is used to control the dc current I_{dc}; thus the absolute amplitude of the reactive power is determined by the small change of the power angle increment $\Delta\theta$ around $\pm 90^o$. A reactive order either 90^o or -90^o is set to force the MLCR-CSC operating under the inductive or capacitive condition.

The amplitude increment or decrement of the dc load branch current I_{dc} depends on the polarity of the dc voltage across the load branch, which is proportional to the cosine function of the power angle ($V_{dc} = k_v V_{sRMS}\cos(\theta)$), if the source voltage V_{sRMS} is maintained constant and the losses in the smoothing reactor is ignored.

However the amplitude increment or decrement of the unidirectional dc current can not be solely determined by the polarity of the power angle increment around $\theta = \pm 90^o$, because around 90^o

$$dV_{dc} = d[k_v V_{sRMS}\cos(90^o + \Delta\theta)] = -k_v V_{sRMS} d\sin(\Delta\theta) \approx -k_v V_{sRMS} d\Delta\theta$$

and around -90^o

$$dV_{dc} = d[k_v V_{sRMS}\cos(-90^o + \Delta\theta)] = k_v V_{sRMS} d\sin(\Delta\theta) \approx k_v V_{sRMS} d\Delta\theta$$

The power angle increment $\Delta\theta$ around $\pm 90^o$ to control the dc current has to be coordinated with the converter operating condition to generate the appropriate polarity of $\Delta\theta$. Thus the closed-loop control structure of the MLCR-CSC STATCOM has been rearranged as shown in Figure 8.10.

An EMTDC model based on the 5-level MLCR-CSC of Figure 8.5 and the control structure of Figure 8.10 has been developed to investigate the use of the MLCR-CSC as a STATCOM. The following simulated waveforms are shown in Figure 8.11:

- (a) Q, Q_{ref}: generated reactive power and reactive power order
  (capacitive being set to positive and inductive to negative)
- (b) I_{dc}, U_{dc}: dc average current and voltage of the dc load branch

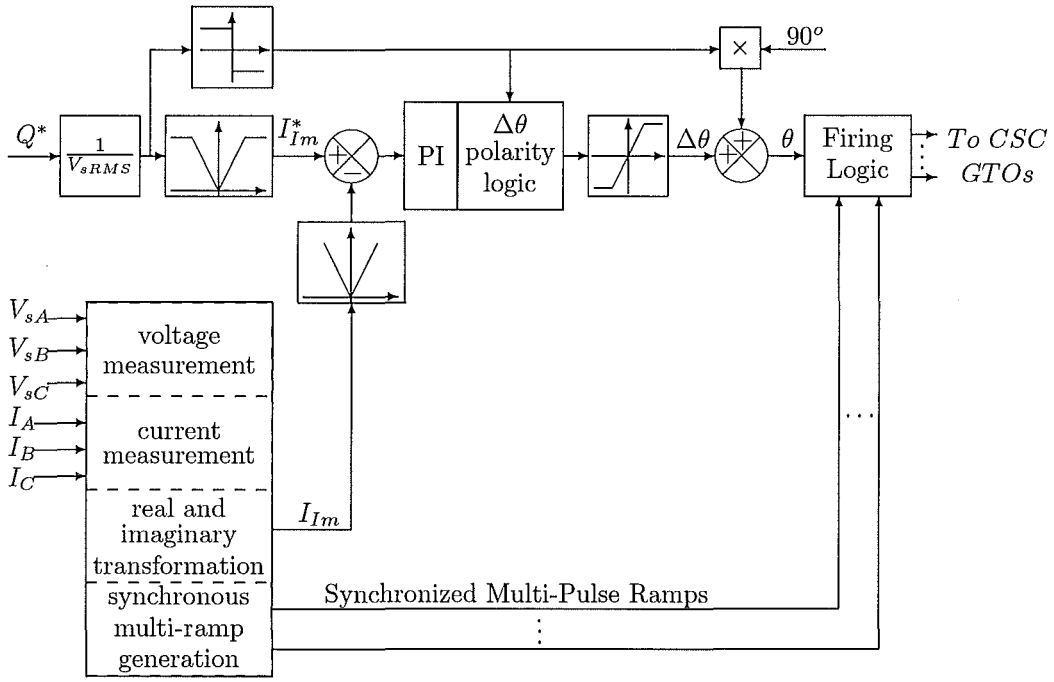


Figure 8.10 The MLCR-CSC Control Structure for STATCOM Application

- (c) V_A, I_A: phase 'A' voltage and current at the power source side
- (d) V_B, I_B: phase 'B' voltage and current at thc power source side
- (e) V_C, I_C: phase 'C' voltage and current at the power source side
- (f) U_{dc} and I_A, I_B, I_C: dc voltage and 3-phase currents in the dynamic period

The normalized bases for the waveforms in Figure 8.11 are

- $Q_{sR} = S_s = 100MVA$ for Q and Q_{ref}
- $V_{SR} = \frac{100\sqrt{2}}{\sqrt{3}}kV$ for U_{dc} and V_A, V_B, V_C
- $I_{dcR} = \frac{\sqrt{3}}{\sqrt{2}}I_{SR} = \frac{1}{\sqrt{2}}kA$ for I_{dc} and I_A, I_B, I_C

These waveforms show the steady and dynamic state performances of the 5-level MLCR-CSC functioning as a STATCOM under the closed loop control. In a period of 0.8 seconds the reactive power order is changed four times in full steps, both increasing and decreasing. By choosing the appropriate P and I parameters for the PI controller and a suitable control logic, the MLCR-CSC responds to these orders very well and generates the required reactive power without steady error.

Referring to Figure 8.11(a), the following dynamic performance is observed:

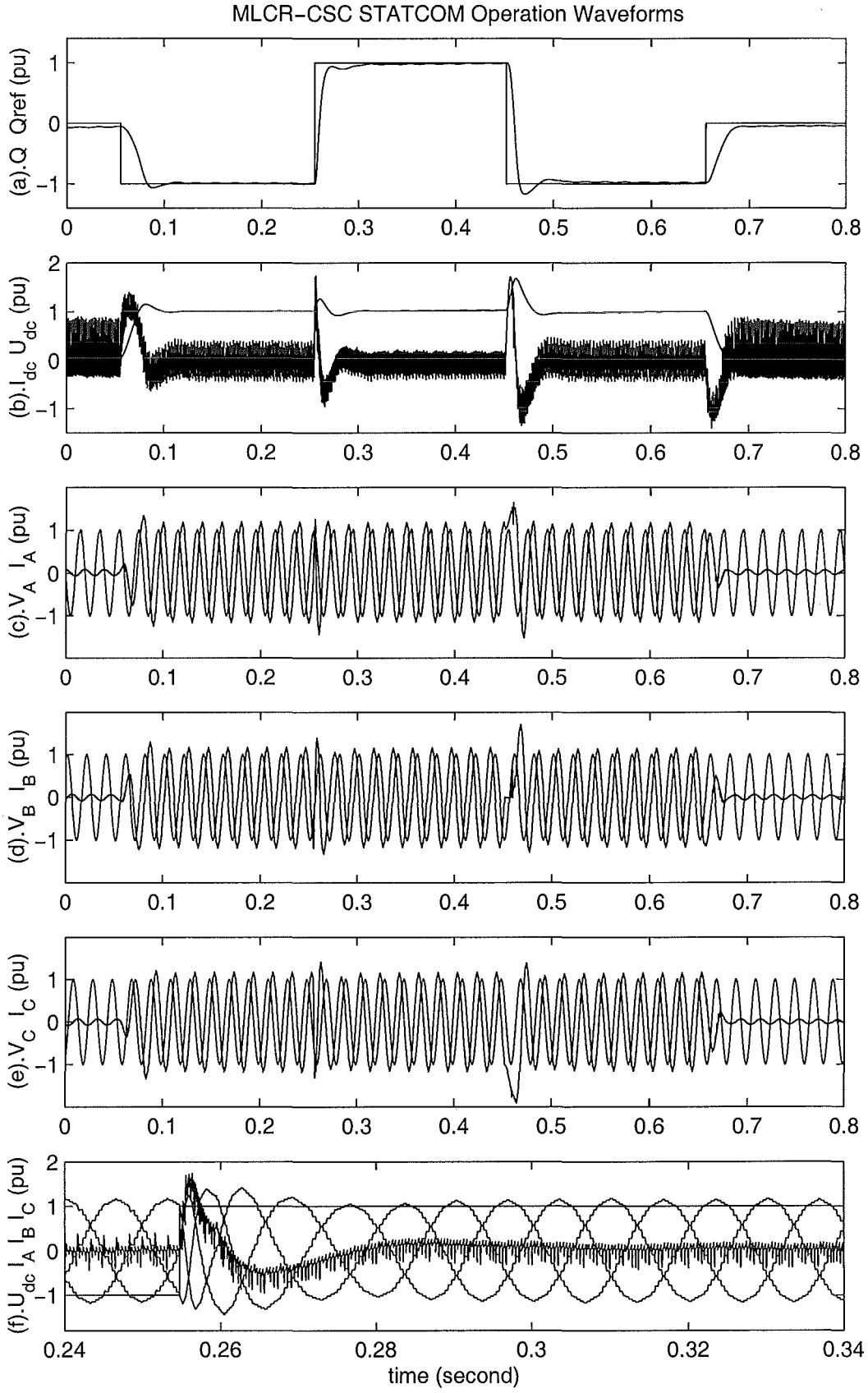


Figure 8.11 The Dynamic Responses of the MLCR-CSC STATCOM

1. the reactive power order Q_{ref} changes from 0 to $-1pu$ at 0.06 seconds, the generated reactive power Q reaches the required value at 0.09 seconds and the dynamic process finishes at 0.1 seconds with a maximum over-shoot under 10%.

2. Q_{ref} changes from $-1pu$ to $1pu$ at 0.254 seconds, Q reaches the required value at 0.27 seconds and the dynamic process finishes before the 0.3 second without observable shoot.

3. Q_{ref} changes from $1pu$ to $-1pu$ at 0.45 seconds, Q reaches the required value at 0.46 seconds and the dynamic process finishes before the 0.49 second with a maximum over shoot under 18%.

4. Q_{ref} changes from $-1pu$ to 0 at 0.65 seconds, Q drops to 0 value at 0.68 seconds and the dynamic process finishes without over-shoot.

The dynamic response indicates that the MLCR-CSC STATCOM can change operating states from inductive to capacitive or vice versa in a very short time. This is so because the operating state change only involves changing the gate control signal without altering the energy storage level; as well as with the bipolar and high range of dc output voltage the dc reactor can be charged or discharged quickly (note the dc current establishing and vanishing in Figure 8.11). Thus the MLCR-CSC STATCOM offers a fast dynamic performance. The waveforms in Figure 8.11 (b) illustrate the dc current I_{dc} and voltage U_{dc} under steady and dynamic operating conditions. The high pulse nature of the reinjection produces a dc voltage with high frequency ripple, this is better displayed in Figure 8.11 (f) for the period between 0.24 and 0.34 seconds.

The waveforms in Figures 8.11 (c), (d) and (e) illustrate the three phase ac output currents and their phase relationship with the source voltage waveforms during the dynamic and steady processes. This information is expanded in Figure 8.11 (f) for the period between 0.24 and 0.34 seconds to demonstrate the dynamic response process of the three phase output currents and dc voltage in detail. Figure 8.11 (f) shows that the dc voltage and three phase currents respond to the reactive power order quickly; thus the MLCR-CSC test system can change its operating state from full scale inductive operation to full scale capacitive operation in approximately one cycle. Figure 8.11(f) also shows that the harmonic distortion of the ac output current is very low.

The simulation results verify that the 5-level MLCR-CSC under closed loop control has fast dynamic performances and no steady-state error, with very low harmonic distortion, and is thus suited to the high power STATCOM application.

8.3.3 Operation under Asymmetrical Source

In practice the power system voltage will always contain some asymmetry, particularly under fault conditions, and thus further simulation is needed to verify that the MLCR-

CSC under closed-loop control can supply balanced ac output currents and that the basic function of a STATCOM can be maintained for serious asymmetrical source conditions.

The dc voltage across the load branch is strongly dependent on the source voltage symmetry; with a symmetrical source voltage the dc voltage ripple is of low amplitude and high frequency (48 times the source fundamental), while for asymmetrical conditions the dc voltage contains a lower frequency ripple of amplitude related to the level of asymmetry. The dc current ripple in turn depends on the dc voltage ripple and the load branch inductance, thus to reduce the dc current fluctuation the load branch inductance has to be increased.

With a sufficiently large inductance the dc current can be maintained constant for symmetrical conditions and will have a relatively low amplitude ripple under serious asymmetrical conditions. Thus the three phase ac output currents of the MLCR-CSC can be kept symmetrical even under severe source voltage asymmetry, because the three phase output currents of the MLCR-CSC are solely determined by the dc current. This performance is verified by the simulation results shown below.

The asymmetrical source voltage conditions of the test system are:

1. A 20% drop in phase 'A' for a period from 0.05sec to 0.35sec;

2. A 20% increase in phase 'A' and a 80% drop in phase 'B' for a period from 0.35sec to 0.75sec

The simulations are performed from inductive to capacitive and then return to inductive operating conditions under the above asymmetrical source conditions.

The simulated waveforms in Figure 8.12 are arranged and normalized as those in Figure 8.11.

The waveforms shown in Figure 8.12 verify that the MLCR-CSC can operate normally under the asymmetrical and even seriously asymmetrical source conditions; however, the dc voltage contains ripple of high amplitude and of low frequency; if these are to be kept within small margins for a large range of asymmetrical level, a larger inductance will be required.

The time interval used for waveforms from (a) to (e) is 0.8 seconds, while that of (f) is 0.1 seconds in order to display the balanced three phase currents in greater detail.

In the period from 0.05 to 0.35 seconds only the voltage of phase 'A' drops by 20%. Under this condition, shown in (b) of Figure 8.12, the dc current contains a ripple of low amplitude and of frequency twice the source fundamental; the reactive power and three phase output currents follow the imaginary current order with nearly the same steady and dynamic state performances as those of the symmetrical condition illustrated in Figure 8.11.

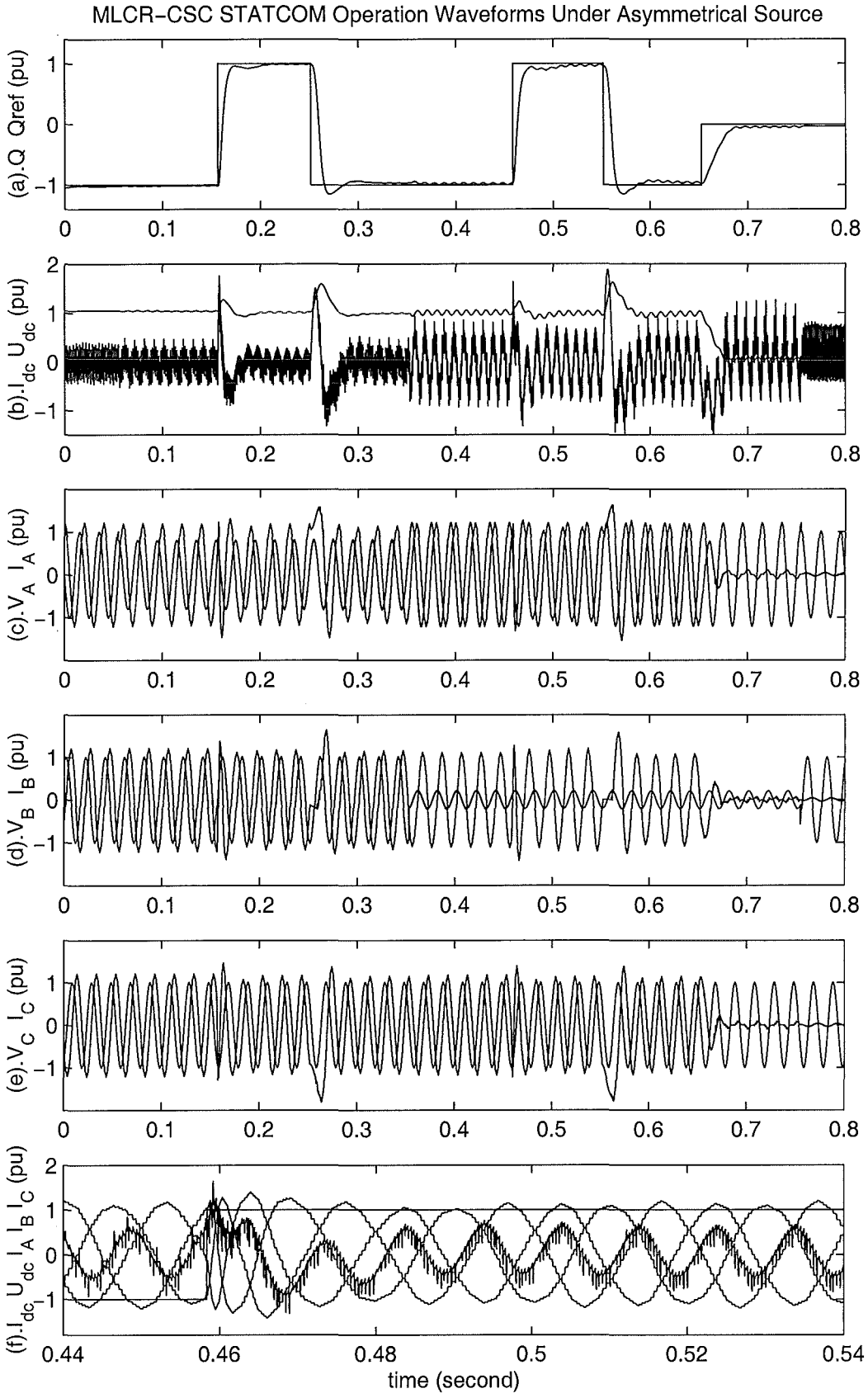


Figure 8.12 Asymmetrical Source Operation of 5-level MLCR-CSC

In the period from 0.35 to 0.75 seconds the voltage of phase 'A' increases by 20% and that of phase 'B' drops by 80%. Under this serious asymmetrical condition the peak to peak value of the dc current ripple is 10% of the average value; however, the dc voltage contains a ripple of very high amplitude and of frequency twice the source fundamental; the reactive power and three phase output currents also follow the imaginary current order with similar steady and dynamic performance as for the symmetrical condition performance illustrated in Figure 8.11.

The simulation results verify that even when the power source voltages are seriously asymmetrical, the MLCR-CSC under closed-loop control still provides balanced compensating currents. However higher inductance in the dc load side is required to reduce the dc current fluctuation and still generate high quality balanced compensation currents.

8.4 SUMMARY OF MLCR-CSC

On the basis of analysis and simulation carried out in this chapter the following conclusions are reached:

1. The currents supplied to the main bridges vary periodically step by step, and at all instants add to a constant dc current. These are different from the constant dc current supplied to each of the bridges in the conventional converters.

2. The ac output currents of the MLCR-CSC bridges are combined by the interface transformer to produce a converter system ac output current with very low harmonic distortion. Even with a few levels on the dc side current of the main bridges a high pulse number is achieved at the converter system ac output current.

3. The currents supplied to the main bridges are synchronized with the main bridge firing control, and a zero level current is produced when there are switches switching on or off.

4. The zero current switching condition enables the main bridge self-commutated valves to commutate under the same condition as the line commutated thyristors in the conventional current source converters. Therefore the successful techniques used by the high power current source thyristor converters can equally be applied to the MLCR-CSC, regardless of whether the operation condition is inductive or capacitive.

5. The provision of a controllable interval ZCS condition not only eliminates the switching losses, but also simplifies the snubber requirements and the interface between the converter and the power system. Snubber-less or very simple snubber structures can be used in the main bridge design, because the zero current

condition ensures that there is no inductive energy stored in the series connected inductor (including the stray inductance). The interface simplicity is a significant advantage of the MLCR-CSC; as it eliminates the need for a high capacitance on the ac side, a problem forced the use of current source conversion in the past for high power applications [79, 80].

6. The reinjection current generating system acts like a controllable current divider. Its voltage rating is low, because only the ac component of the dc output voltage will apply across it. The fact that the reinjection circuitry is involved in the main power flow is the main disadvantage as compared with the MLVR -VSC.

7. Because the currents supplied to the converter bridges are controlled to rise and fall step by step, very low dI/dt's will occur during the main bridge switchings. The lower dI/dt makes the use of the high power GTO or IGCT switches possible and reduces the electromagnetic interference (EMI).

The MLCR converters combine the concepts of multi-level conversion, soft switching and reinjection conversion to provide the advantages of lower harmonic distortion, lower switching frequency and higher reliability. Thus they are suitable for high voltage and high power application.

Compared to the MLVR-VSC an important advantage of the MLCR-CSC is its capability of maintaining balanced three phase current operation under the conditions of symmetrical and asymmetrical source voltages. The main disadvantage of the MLCR-CSC is the need to place the reinjection circuitry in the main power flow path.

Chapter 9

GENERAL CONCLUSIONS AND FURTHER WORK

9.1 GENERAL CONCLUSIONS

The proposed **multi-level reinjection ac-dc conversion** combines the multi-level conversion, soft switching and reinjection concepts. Based on the new concept this thesis has developed **multi-level voltage and current reinjection** converters with improved performance, enhanced reliability and increased efficiency. The subjects covered include topologies, firing sequences, waveform analysis, steady and dynamic state performances, closed-loop control strategies and particular applications, both for the multi-level voltage and current reinjection converters. General conclusions regarding the concept itself and the types of converters are presented in this section.

9.1.1 The Multi-Level Reinjection Waveforms

The 6-pulse converter can be thought of as the combination of two half-bridges and the 12-pulse converter the combination of two full-bridges. For a general description of the reinjection concept, the converter switching circuits connected to the dc sources are considered as two subsystems, which can be connected in series and parallel.

In the conventional converters the two subsystems are directly connected to a dc source or the dc source is equally shared by the two subsystems; in other words, the dc sides of the two subsystems are supplied by dc voltage or current waveforms. By the converter switching actions these dc waveforms are chopped and distributed to three ac phases. The chopping action causes harmonic distortion, high dv/dt or di/dt and high switching losses. The ideal (optimal) reinjection waveform and its approximations are derived to overcome these problems.

To achieve perfect harmonic cancellation on the ac side the **ideal reinjection waveform** to be supplied to the two subsystems must contain, as well as a dc component, even and odd harmonics of the subsystem commutation frequency (the commutation frequencies of the 3-phase half bridge and full-bridge are 3 and 6-times the ac power source fundamental frequency respectively). Resulting from this requirement the addition of the waveforms supplied to the two subsystems is not a constant dc level,

i.e. the dc source must contain ripple. Finally the ideal reinjection waveform varies periodically and continuously with limited time derivatives ($|di/dt|_{max}$ or $|dv/dt|_{max}$ being under some level) and also contains periodical zero value points. With the ideal reinjection waveform the switches in the two subsystems are always change their state under zero current (for CSC) or zero voltage (for VSC) dc supply, thus they are used only to distribute the dc side waveform to the three phases, unlike conventional converters to chop the dc voltage or current and distribute the chopped dc waveform to the ac phases.

A possible symmetrical approximation to the ideal reinjection, **the ESEDS-reinjection waveform**, still produces a high quality ac output, but without the need for a dc source with (controllable) ripple. In this alternative the reinjection waveforms of the two subsystems consist of a dc component and the odd harmonics of the subsystem commutation frequency (i.e. the even harmonics are absent), and the addition of the waveforms supplied to the two subsystems is a constant dc level. Although the ESEDS alternative does not produce exact zero points, these points are very close to zero.

An alternative approximation is the **linear-reinjection waveform**, which also produces a high quality output (although the distortion is slightly higher than in the ESEDS case). It shares with the ideal solution the appearance of periodical zero value points. Like in the ESEDS alternative, the reinjection waveforms of the two subsystems contain only odd harmonics of the subsystem commutation frequency and they add to a constant dc level.

Further approximation to the ideal is the **multi-level reinjection waveform**. The **ESEDS multi-level reinjection** produces a better waveform but does not benefit from the exact soft switching condition. The **linear multi-level reinjection** waveform, with soft switching conditions, is more suited to high voltage and power applications.

Six and Twelve pulse configurations:

The reinjection waveform, in the 6-pulse case, is applied to the two (half-bridge) subsystems, which both produce waveforms with harmonics of odd triple orders and in phase, however the triple harmonics do not penetrate the ac system if the interface transformer primary (ac source side) windings are connected either in Δ or Y connection without neutral.

When applied to the 12-pulse configuration the reinjection waveform shapes the output of the two (bridge) subsystems producing the same harmonic spectra of orders $[6(2k-1) \pm 1 \quad (k = 1, 2, \cdots)]$ but out of phase by 180^o for all orders, so that harmonic cancellation is achieved at the interface transformer primary side.

9.1.2 The Generation of the Reinjection Waveforms

In the ac-dc conversion systems the dc source can be directly connected to the two subsystems (i.e. in parallel for the VSC or in series for the CSC); alternatively the dc source can be shared by the two subsystems (in parallel for the CSC or in series for the VSC).

As the reinjection waveform can be decomposed into dc and ac components, and the fully symmetrical reinjection waveforms of the two subsystems combine into a perfect dc level, the generation of the reinjection waveforms can be implemented in two ways, referred to below as Combination and Distribution.

Combination: In this case an ac component adds to and subtracts from the dc components of the two subsystems. To maintain coordination between the dc source and the generated ac component, the later is derived from the dc source; consequently a reinjection transformer is required, both, for isolation from the dc source and for the implementation of the required additions and subtractions. This solution can be used with the common direct supply and share connection alternatives. However, the need for a reinjection transformer somewhat reduces its attraction.

For a VSC (voltage source converter) to generate an m-level reinjection waveform by the combination method, $(m-1)/2$ reinjection transformers are needed. Thus to reduce the number of the reinjection transformers, while obtaining a reasonable waveform, the ESEDS-reinjection solution is the preferred option. On the other hand in the CSC case a higher level reinjection waveform can be derived by increasing the number of windings of the reinjection transformers.

Distribution: When the two subsystems are connected to share the dc source, their corresponding fully symmetrical reinjection waveforms can be generated by appropriately distributing the dc source between them. For this purpose, controllable dc voltage or current dividers can be used to generate the reinjection waveforms. This solution, however, can not be used when the dc source is directly supplied to the two subsystems (like paralleled bridges for VSC or series connected bridges for CSC).

The distribution alternative is better suited for high level numbers with correspondingly lower dV/dt or di/dt stresses; moreover, with the assistance of the inherent soft switching the dynamic voltage balance presents no problem and is, therefore, perfectly suited to high voltage applications.

In this case the linear reinjection alternatives is the most cost effective solution for generating the reinjection waveforms.

For the MLVR the controllable voltage divider is a single phase multi-level VSC with three terminals. The reinjection circuit does not involve the dc current (and

therefore the main power flow). The criteria for the selection of the topological structure is the number of switching devices and the implementation of capacitor voltage balancing.

For the MLCR the controllable current divider is a multi-tapped reactor and self-commutated switching devices. This case presents no capacitor voltage balancing problems, but the dc current flows through the reinjection circuit; on the other hand the voltage rating of the reinjection switches is low.

9.1.3 The Multi-Level Voltage Reinjection VSC

The 6-pulse reinjection VSC is not suitable for practical application because of the need to provide the interface transformer with an extra path for the triple flux components. A practical alternative is the Multi-Level ESEDS-Reinjection VSC, implemented by adding a separate single-phase reinjection self-commutated bridge and a reinjection transformer to the conventional 12-pulse VSC configuration (either the parallel or series connection). Its main advantages are the absence of capacitor voltage balancing problems and the capability of four quadrant operation (i.e. independent control of active and reactive powers); the main disadvantage is the cost and losses of the reinjection transformer.

The MLVR-VSC provides an effective solution for high power and high voltage applications. The two main bridges are series connected and supplied by a controllable dc voltage divider with the voltage waveform increasing and decreasing periodically in equal steps. Its main features are:

1. **High quality voltage and current waveforms**: The m-level reinjection waveform produces an ac output waveform equivalent to a $12(m-1)$-pulse conversion system.

2. **High voltage rating**: The multi-level reinjection voltage waveforms with zero levels enable an effective direct series connection of the main bridge switching devices with reduced dv/dt stress and without dynamic voltage balance problem in the switching devices.

3. **High efficiency**: The fundamental frequency related switching and the soft switching for the main bridges greatly reduces the switching losses in switching devices and snubber circuits. Also as the dc current does not flow through the reinjection circuit, the low current rating of this circuit causes insignificant power losses.

4. **High reliability**: The main bridge switching devices have the same rating due to the synchronous control, and the valve structure can be provided with redundant devices in the series connection; also the forced clamping soft switching condition

ensures that the main bridges switching occur without the risk of short-circuiting the dc source. Thus the MLVR-VSC operates with high reliability.

5. **Cost effectiveness**: The main bridges in the MLVR-VSC are structured and controlled as the conventional six-pulse pulse converter, and the voltage rating depends on the number of the direct series connected switches without concern for dynamic voltage balance and without complicated snubber circuits. The low current rating and the same size of reinjection components add a insignificant portion to the converter cost, but eliminate the need of expensive filters. Thus the simpler structure and control requirements make the converter system more compact and cost effective.

6. **Four quadrant operation**: Unlike the multi-level diode clamped VSC (level number greater than 3) without the capability to control real power [13, 20], the MLVR-VSC can be used to control real and reactive power with four quadrant operation capability, although its use in the pure real power transfer is prohibited if the capacitor voltage balance is to be maintained (refer to chapter 6). There is no difficulty for the MLVR-VSC to operate under the conditions of power factor in the range of $|\cos\theta| < 0.96$ while maintaining the capacitor voltage in balanced state.

7. **Indirect Amplitude Control**: There is no independent control of the individual phase voltage amplitude, since the amplitude control can only be achieved by changing the dc voltage via phase angle control; thus the MLVR-VSC is sensitive to ac source voltage imbalance.

9.1.4 The Multi-Level Current Reinjection CSC

The MLCR-CSC based on the 6-pulse conversion system generates triplen harmonic currents but no triplen harmonic voltages; therefore, there is no special requirement regarding the interface transformer. Thus both the 6-pulse and 12-pulse reinjection conversion can be implemented with conventional transformers.

The MLCR-CSC presents no problem with capacitor voltage balancing; and the interface with the ac system presents no difficulty due to the zero current soft switching condition.

The Multi-Level Current Reinjection CSC with the ZCS condition has the following characteristics:

1. **High quality voltage and current waveforms**: The m-level reinjection schemes produce an ac output waveform equivalent to a $6(m-1)$-pulse (for 6-pulse system) or $12(m-1)$-pulse (for 12-pulse system) conversion system.

2. **High voltage rating**: The MLCR-CSC permits an effective direct series connection of the switching devices in the main bridges, with limited di/dt stress and simplifies the dynamic voltage balance of the switching devices.

3. **High efficiency**: The use of fundamental related switching and of soft switching for the main bridges reduces the switching losses and simplifies the snubber circuit; however the over all losses are still higher than those of the MLVR-VSC.

4. **High reliability**: The main bridge switches have the same rating due to the synchronous control, and the valves can be provided with redundant devices in the series connection; also the forced blocking soft switching condition eliminates commutation overlap and prevents over voltage caused by the high di/dt during the commutation. Thus the MLCR-CSC operates with high reliability.

5. **Cost effectiveness**: The main bridges in the MLCR-CSC are structured and controlled as the conventional six-pulse pulse converter; the ZCS condition simplifies the circuit for ensuring the steady and dynamic voltage balance, also the ZCS eliminates the requirement of expensive large size of interfacing ac capacitors. Thus the converter system is compact and cost effective.

6. **Control Flexibility**: The MLCR-CSC can be used to control real and reactive power with four quadrant operation capability. It is also capable of controlling the dc output current from zero to full scale, and the dc voltage from full positive to full negative levels.

7. **Symmetrical output Waveforms**: As the ac output current amplitude is determined by the stable dc current, the MLCR-CSC is insensitive to the source voltage asymmetry and produces symmetrical ac currents even during serious source voltage asymmetry.

9.2 FURTHER WORK

The multi-level reinjection concept has been developed for the VSC and CSC alternatives and the theoretical analysis has been verified by simulation. The experimental verification needs to be carried out.

The following topics need to be investigated to extend the application of the MLVR-VSC and MLCR-CSC.

A. Simplification and Improvement of the Reinjection Circuit:

1. **Topological Structure**: The concept of the multi-level voltage and current reinjection simplifies the structure and control of the main bridges, the complexity of the systems depending on the the reinjection circuit and particularly on the multi-level controllable voltage and current dividers.

In the design of the voltage divider for very high voltage applications, a difficult compromise has to be made between the level number m and the level voltage $V_L(= U_{dc}/m)$, because low m and high V_L lead to fewer groups of reinjection switches, but every group has a large number of switches in series with complicated circuits to maintain steady and dynamic voltage balance. This difficulty is caused by the nonlinear relationship between the level number and the total number of reinjection switches required by the available topologies. Further work is needed to develop an ideal topology for the reinjection voltage divider where the total number of switches required is proportional to the level number and the proportional factor is low.

Although the total reinjection switches required by the H-Bridge structure is proportional to the level number m $[8(m-1)]$, the proportional factor (8) is still too high. Thus further work is needed to improve the reinjection circuit for very high voltage applications.

2. **Capacitor Voltage Balance**: This is an important limitation for the use of high level numbers in the case of the MLVR-VSC. The conditions leading to imbalance in this case are very different from those of the MLDC-VSC, there are possibilities to achieve self-balance or using very simple circuit without the need of control loop. Further research is needed to achieve self-balanced reinjection, such as obtained by the capacitor clamping and H-Bridge topological structures.

B. Control Flexibility of the MLVR-VSC and MLCR-CSC

The proposed control strategies for the MLVR-VSC and MLCR-CSC are based on fundamental frequency switching, and they do not provide independent amplitude control. This reduces their applicability to some applications such as BTB-VSC-Links; in this case the common shared capacitor voltage determines the ac output voltage amplitudes of the two MLVR-VSCs, and therefore the reactive powers can not be controlled independently. The availability of independent amplitude control capability in a BTB-VSC-Link would control the active powers and reactive powers on both sides independently, thus making the link operate like two STATCOMs as well as control of active power transfer.

Independent phase amplitude control is also needed to improve the operation under voltage source asymmetry. To provide individual phase voltage amplitude control, the coordinated control of the main and reinjection switches needs to be investigated.

The MLCR-CSC is capable of controlling the dc current and voltage for the full scale range. The additional provision of independent amplitude control capability would permit the MLCR-CSC to control the magnetic energy of a super-conducting magnetic energy storage system as well as operate as a STATCOM; otherwise the ac side reactive power will depend on the level of the stored magnetic energy.

The by-passing function of the main bridge switching devices may be used to obtain independent amplitude control in the case of the MLCR-CSC. However the by-passing states of the main bridges need to be coordinated with the reinjection circuit, so that the ZCS soft switching condition for the main bridge is maintained.

C. Possible elimination of the interface transformer

All the configurations proposed in this thesis for the MLVR-VSC and MLCR-CSC contain interface transformers, because the interface transformer plays a important role in the harmonic cancellation. If the output voltages of the two subsystems could be synthesized to generate the required ac output waveform for harmonics cancellation without the assistant of a interface transformer, the MLVR-VSC and MLCR-CSC could be made more attractive.

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Appendix C

PUBLICATIONS

The following is a list of publications resulting from the work described within this thesis.

1. Y.H. Liu, J. Arrillaga, N.R. Watson; "*Multi-level voltage sourced conversion by voltage reinjection at six times the fundamental frequency*". *IEE Proc.-Electr. Power Appl.*, Vol. 149, No. 3, pp. 201–207, May 2002.
2. Y.H. Liu, J. Arrillaga, N.R. Watson; "*A four quadrant multi-level back-to-back HVdc interconnector*". *International Conference on Power System Technology*, PowerCon 2002 Proceedings, Volume: 1, Page(s): 510–514, 13-17 Oct. 2002.
3. Y.H. Liu, J. Arrillaga, N.R. Watson; "*A New High-Pulse Voltage-Source Converter For HVdc Transmission*". *IEEE Transaction on Power Delivery.* vol. 18, No. 4, Oct. 2003.
4. Y.H. Liu, J. Arrillaga, N.R. Watson; "*A New STATCOM Configuration Using Multi-Level D.C. Voltage Reinjection for High Power Application*". Accepted to be published for *IEEE Transaction on Power Delivery.*
5. Y.H. Liu, J. Arrillaga, N.R. Watson;"*Multi-Level Voltage Reinjection (MLVR)- A New Concept in High Voltage Source Conversion*". Submitted to *IEE Proc.-Gener. Trans. Distr.*
6. Y.H. Liu, N.R. Watson, J. Arrillaga; "*A New Concept for the Control of the Harmonic Content of Voltage Source Converters*". Accepted for *the IEEE International Conference on Power Electronics and Drive Systems*
7. Y.H. Liu, N.R. Watson, J. Arrillaga; "*EMTDC Assessment of a New Type of VSC for Back to Back HVdc Interconnection*"; Accepted for *The International Conference on Power System Transients* IPST 2003
8. Y.H. Liu, J. Arrillaga, N.R. Watson; " *Alternative Switching Configuration for Multi-Level Voltage Sourced Converters*"; *Australasian Universities Power Engineering Conference* AUPEC 2002, 29/Sep.–2/Oct. Melbourne
9. Y.H. Liu, J. Arrillaga, N.R. Watson; "*Neutral Point Reinjection for a Low Distortion Three Phase Bridge Voltage Source Converter*"; *Australasian Universities Power Engineering Conference* AUPEC 2003, 28/Sep.–1/Oct. Christchurch
10. Y.H. Liu, J. Arrillaga, N.R. Watson; "*A STATCOM Configuration For Very Low Voltage Distortion*" *Australasian Universities Power Engineering Conference* AUPEC 2003, 28/Sep.–1/Oct. Christchurch

REFERENCES

[1] S. Bernet, "Recent Development of High Power Converters for Industry and Traction Applications," *IEEE Trans. on Power Electronics*, vol. 15, No. 6, pp. 1102–1117, Nov. 2000.

[2] S. Kaufmann and F. Zwick, "10 kV IGBT press pack modules with series connected chips," *Proceedings of the 14th International Symposium on Power Semiconductor Devices and ICs*, vol. IEEE ISPSD '02, pp. 89–92, 2002.

[3] S. Kaufmann, T. Lang, and R. Chokhawala, "Innovative press pack modules for high power IGBTs," *Proceedings of the 13th International Symposium on Power Semiconductor Devices and ICs*, vol. IEEE ISPSD'01, pp. 59–62, 2001.

[4] T. Fujii, K. Yoshikawa, T. Koga, Y. Takahashi, H. Kakiki, M. Ichijyou, and Y. Seki, "4.5 kV-2000 A Power Pack IGBT (ultra high power flat-packaged PT type RC-IGBT)," *Proceedings of the 12th International Symposium on Power Semiconductor Devices and ICs*, vol. IEEE ISPSD'00, 2000.

[5] C. Schauder and et al., "Development of $\pm 100 MVAR$ Static Condenser for Voltage control of Transmission System," *IEEE Transactions On Power Delivery*, vol. 10, No. 3, pp. 1486–1493, July, 1995.

[6] S. Mori, T. Hasegawa, K. Matsuno, S. Ohnishi, M. Takeda, and M. Seto, "Development of A Large Static VAR Generator Using Self-Commutated Inverter for Improving Power System Stability," *IEEE Trans. on power system*, vol. 8, No. 1, pp. 371–377, Feb. 1993.

[7] C. Schauder, M.Gernhardt, E. Stacey, T.Lemark, L. Gyugyi, T.W. Cease, and A. Edris, "Operation of 100 MVAr TVA STATCON," *IEEE Transactions on Power Delivery*, vol. 12, Issue: 4, pp. 1805 –1811, Oct. 1997.

[8] C. Schauder, E. Stacey, M. Lund, L. Gyugyi, L. Kovalsky, A. Keri, and A. Mehraban A. Edris, "AEP UPFC project: installation, commissioning and operation of the 160 MVA STATCOM (phase I)," *IEEE Transactions on Power Delivery*, vol. 13, Issue: 4, pp. 1530–1535, Oct 1998.

[9] Tatsuhito Nakajima and et al., "A Converter Transformer with Series-Connected Line-Side Windings for a DC Link Using Voltage Source Converters," *Power Enginering Society Winter Meeting*, vol. 2, pp. 1073–1078, 1999.

[10] B.A. Renz, A. Keri, A.S. Mehraban, C. Schauder, E. Stacey, L. Kovalsky, L. Gyugyi, and A. Edris, "AEP unified power flow controller performance," *IEEE Transactions on Power Delivery*, vol. 14, Issue: 4, pp. 1374–1381, Oct 1999.

[11] S. Zelinger, B. Fardanesh, B. Sherling, S. Dave, L. Kovalsky, C. Schauder, and A. Edris, "Convertible static compensator project-hardware overview," *IEEE Power Engineering Society Winter Meeting*, vol. 4, pp. 2511–2517, 2000.

[12] I. Takahashi A. Nabae and H. Akagi, "A new neutral-point-clamped PWM inverter," *IEEE Trans. on Industry Application*, vol. IA-17(5), pp. 518–523, 1981.

[13] Jung G. Cho Nam S. Choi and Gyu H. Cho, "A General Circuit Topology of Multilevel Inverter," *IEEE Power Electronics Specialist Conference, MIT, USA*, vol. PESC 91 Record, pp. 96–103, 1991.

[14] X. Yuan and et al., "Fundamentals of a New Diode Clamping Multilevel Inverter," *IEEE Trans. on Power Electronics*, vol. 15, No. 4, pp. 711–718, July, 2000.

[15] T. Meynard and H. Foch, "Imbricated cell multi-level voltage source inverters for high voltage applications," *European Power Electronics Journal*, vol. 3(2), pp. 99–106, 1993.

[16] Y. Chen and et al., "Regulating and Equalizing DC Capacitance Voltages in Multi-Level STATCOM," *IEEE Trans. on Power Delivery*, vol. 12, NO. 2, pp. 901–906, Apr. 1997.

[17] B.T. Ooi and et al., "Operating Principle Of Shunt STATCOM Based on 3-Level Diode-Clamped Converters," *IEEE Trans. on Power Delivery*, vol. 4, No. 4, pp. 1504–1510, Oct. 1999.

[18] F.S. Shyu and Y.S. Lai, "Virtual Stage Pulse-Width Mondulation Technique for Multilevel Inverter/Converter," *IEEE Trans. on Power Electronics*, vol. 17, No. 3, pp. 332–341, May, 2002.

[19] Fang Zheng Peng, "A generalized multilevel inverter topology with self voltage balancing," *IEEE Transactions on Industry Applications*, vol. 37, Issue: 2, pp. 611–618, Mar/Apr. 2001.

[20] J.S. Lai and F.Z. Peng, "Multilevel converters-a new breed of power converters," *IEEE Trans. on Industry Applications*, vol. 32, No. 3, pp. 509–517, May/Jun. 1996.

[21] Y. Shakweh, "MV inverter stack topologies," *Power Engineering Journal*, vol. 15, Issue: 3, pp. 139–149, Jun 2001.

[22] J. Rodriguez, Jih-Sheng Lai, and Fang Zheng Peng, "Multilevel inverters: a survey of topologies, controls, and applications," *IEEE Transactions on Industrial Electronics*, vol. 49, Issue: 4, pp. 724–738, Aug 2002.

[23] T.A. Meynard and H. Foch, "Multi-level conversion: high voltage choppers and voltage-source inverters," *23rd Annual Power Electronics Specialists Conference*, vol. 1, IEEE PESC '92 Record., 29 Jun-3 Jul 1992.

[24] Xiaomin Kou and K. A. Corzine andY. L. Familiant, "Full binary combination schema for floating voltage source multilevel inverters," *IEEE Transactions on Power Electronics*, vol. 17, No. 6, pp. 891–897, Nov. 2002.

[25] P.W. Hammond, "A new approach to enhance power quality for medium voltage AC drives," *IEEE Transactions on Industry Applications*, vol. 33, Issue: 1, pp. 202–208, Jan/Feb 1997.

[26] E. Cengelci, S.U. Sulistijo, B.O. Woo, P. Enjeti, R. Teoderescu, and F. Blaabjerg, "A new medium-voltage PWM inverter topology for adjustable-speed drives," *IEEE Transactions on Industry Applications*, vol. 35, Issue: 3, pp. 628–637, May/Jun 1999.

[27] S. Daher, R. Silva, and F. Antunes, "Multilevel current source inverter-the switching control strategy for high power application," *Proceedings of the 22nd International Conference on Industrial Electronics, Control, and Instrumentation*, vol. 3, IEEE IECON'96, pp. 1752–1757, Aug 1996.

[28] H.A.C. Braga and I. Barbi, "A new technique for parallel connection of commutation cells: analysis, design, and experimentation," *IEEE Transactions on Power Electronics*, vol. 12, Issue: 2, pp. 387–395, Mar. 1997.

[29] K. Oguchi, H. Hama, and T. Kubota, "Multilevel current-source and voltage-source converter systems coupled with harmonic cancelling reactors," *Conference Record of the IEEE Industry Applications Society Annual Meeting*, vol. 2, IAS'97, pp. 1300–1308, Oct. 1997.

[30] Xiaofen Shi and Chok-You Chan, "Analysis and Passivity-Based Control of Zero-Voltage-Transition PWM Converters," *IEEE Transactions on Power Electronics*, vol. 17, No. 5, pp. 633–640, 2002.

[31] Jr. K. Mark Smith and Keyue Ma Smedley, "Properties and Synthesis of Passive Lossless Soft-Switching PWM Converters," *IEEE Transactions on Power Electronics*, vol. 14, pp. 890–899, Sep. 1999.

[32] Jr. K. Mark Smith and Keyue Ma Smedley, "Engineering Design of Lossless Passive Soft Switching Methods for PWM Converters–Part I: With Minimum Voltage Stress Circuit Cells," *IEEE Transactions on Power Electronics*, vol. 16, No. 3, pp. 336–344, May 2001.

[33] Jr. K. Mark Smith and Keyue Ma Smedley, "Engineering Design of Lossless Passive Soft Switching Methods for PWM Converters–Part II: With Non-Minimum Voltage Stress Circuit Cells," *IEEE Transactions on Power Electronics*, vol. 17, No. 6, pp. 864–873, Nov. 2002.

[34] M. Nakamura, T. Yamazaki, M. Shimada, Md. Rukonuzzaman, H. Iyomori, E. Hiraki, and M. Nakaoka, "A novel pulse regenerative active auxiliary edge resonant bridge leg link soft commutation snubber and resonant snubber-assisted three phase soft switching sinewave PWM inverter," *IEEE Power Electronics Specialists Conference*, vol. 4, PESC'02, pp. 1935–1940, 2002.

[35] I. Husain and M. Ehsani, "Analysis of high power soft-switching DC-DC converters using basic three-terminal structures," *Proceedings of the IEEE International Conference on Industrial Electronics, Control, and Instrumentation*, vol. 1, IECON'95, pp. 252–257, Nov. 1995.

[36] R. D. Monteiro and A. V. A. Anunciada, "Design principles of a soft-switching cell usable in bridge DC-DC and DC-AC converters," *IEEE Power Electronics Specialists Conference*, vol. 4, PESC'02, pp. 1861–1866, 2002.

[37] R.L. Steigerwald, "A review of soft-switching techniques in high performance DC power supplies," *Proceedings of the International Conference on Industrial Electronics, Control, and Instrumentation*, vol. 1, IECON'95, pp. 1–7, Nov. 1995.

[38] D. Divan, "Lower-stress switching for efficiency," *IEEE SPECTRUM*, vol. 33 Issue: 12, pp. 33–39, Dec. 1996.

[39] D.M. Divan, "The resonant DC link converter-a new concept in static power conversion," *IEEE Transactions on Industry Applications*, vol. 25, No. 2, pp. 317–325, March/April 1989.

[40] M. Kurokawa, Y. Konishi, and M. Nakaoka, "Evaluations of voltage-source soft-switching inverter with single auxiliary resonant snubber," *IEE Proceedings of Electric Power Applications*, vol. 148, No. 2, pp. 207–213, 2001.

[41] Shaotang Chen and Thomas A. Lipo, "A Novel Soft-Switched PWM Inverter for AC Motor Drives," *IEEE Transactions on Power Electronics*, vol. 11, No. 4, pp. 653–659, July 1996.

[42] Jung G. Cho, Ju W. Baek, Dong W. Yoo, and Chung Y. Won, "Three level auxiliary resonant commutated pole inverter for high power applications," *IEEE Power Electronics Specialists Conference Record.*, vol. 2, PESC'96, pp. 1019–1026, Jun. 1996.

[43] H. Yamamoto, M. Kaneda, and Mutsuo Nakaoka, "Three-phase Soft-Switching Inverter Resonant with Unique Resonant Snubber," *IEEE International Conference on Power Electronics and Drive Systems*, vol. PEDS'99, pp. 1078–1083, July 1999.

[44] Deepak Divan and Ian Wallace, "New developments in resonant DC link inverters," *Proceedings of the Power Conversion Conference*, vol. 1, pp. 311 –318, Aug 1997.

[45] Fang Z.Peng, Gui-Jia Su, and Leo M. Tolbert, "A passive soft-switching snubber for PWM inverters," *Power Electronics Specialists Conference*, vol. 1, PESC'02, pp. 129–134, 2002.

[46] M. Matsui, "Bidirectional soft switching arm topology for a nonresonant HF link converter," *Conference Record of the Industry Applications Conference, IEEE Thirty-First IAS Annual Meeting*, vol. 2, IAS'96, pp. 1153–1160, Oct 1996.

[47] A. Bendre, I. Wallace, G. A. Luckjiff, S. Norris, R. W. Gascoigne, D. Divan, and R. A. Cuzner, "Design considerations for a soft-switched modular 2.4-MVA medium-voltage drive," *IEEE Transactions on Industry Applications*, vol. 38, Issue: 5, pp. 1400–1411, 2002.

[48] G. L. Skibinski and D. M. Divan, "Design integration of a 200 kW GTO RDCL converter," *Conference Record of the IEEE Industry Applications Society Annual Meeting*, vol. 2, IAS'93, pp. 1029–1040, Oct 1993.

[49] Xiaoming Yuan, Herbert Stemmler, and Ivo Barbi, "Evaluation of Soft Switching Techniques for Neutral clamped (NPC) Inverters," *Power Electronics Specialists Conference*, vol. 2, PESC'99, pp. 659–664, 1999.

[50] M. Yamamoto, S. Sato, E. Hiraki, and M. Nakaoka, "Auxiliary active resonant commutated snubber-assisted 3-level 3-phase voltage source soft-switching inverter," *Proceedings of the Power Conversion Conference*, vol. 3, PCC'02, pp. 1245 –1250, Osaka 2002.

[51] C. Turpin, L. Deprez, F. Forest, F. Richardeau, and T. A. Meynard, "A ZVS imbricated cell multilevel inverter with auxiliary resonant commutated poles," *IEEE Transactions on Power Electronics*, vol. 17, Issue: 6, pp. 874–882, Nov. 2002.

[52] R. Teichmann and S. Bernet, "A multi-level ARCP voltage source converter topology," *Proceedings of The 25th Annual Conference of the IEEE Industrial Electronics Society*, vol. 2, IECON'99, pp. 602–607, 1999.

[53] J. G. Cho, J. W. Baek, D. W. Yoo, C. Y. Won, and G. H. Rim, "Zero-voltage-switching three-level auxiliary resonant commutated pole inverter for high-power applications," *IEE Proceedings-Electric Power Applications*, vol. 145 Issue: 1, pp. 25–32, Jan. 1998.

[54] F.R. Dijkhuizen, J. L. Duarte, and W. D. H. van Groningen, "Multi-level converter with auxiliary resonant-commutated pole," *Conference Record of the IEEE Industry Applications Society Annual Meeting*, vol. 2, pp. 1440–1446, Oct. 1998.

[55] Xiaoming Yuan, G. Orglmeister, and I. Barbi, "ARCPI Resonant Snubber for the Neutral-Point-Clamped Inverter," *IEEE Transactions on Industry Applications*, vol. 36, No. 2, pp. 586–595, Mar/Apr 2000.

[56] M. Yamamoto, E. Hiraki, H. Iwamoto, S. Sugimoto, I. Kouda, and M. Nakaoka, "Voltage-fed NPC soft-switching inverter with new space voltage vector modulation scheme," *Conference Record of the IEEE Industry Applications Society Annual Meeting*, vol. 2, IAS'99, pp. 1178–1185, 1999.

[57] B.M. Bird, J. F. Marsh, and P. R. Mclellan, "Harmonic Reduction in Multiplex Converters by Triple-frequency current injection," *Proc. IEE*, vol. 116, No. 10, pp. 1739–1734, October, 1969.

[58] A. Ametani, "Generalized Method of Harmonic Reduction in a.c.-d.c. converters by Harmonic Current Injection," *Proc. IEE*, vol. 119, No. 7, pp. 857–864, July, 1972.

[59] J.F. Baird and J. Arrillaga, "Harmonic Reduction in dc-Ripple Reinjection," *Proc. IEE, Part-C*, vol. 127, pp. 294–303, 1980.

[60] J.Arrilaga and M. Villablanca, "24-pulse HVDC conversion," *IEE Proceedings Part-C*, vol. 138, No. 1, pp. 57–64, Jan. 1991.

[61] J. Arrillaga and M. E. Villablanca, "A modified parallel HVDC convertor for 24 pulse operation," *IEEE Transactions on Power Delivery*, vol. 6, Issue: 1, pp. 231–237, Jan 1991.

[62] J. Arrillaga and M. E. Villablanca, "Pulse doubling in parallel convertor configurations with interphase reactors," *IEE Proceedings-Electric Power Applications*, vol. 138, Issue: 1, pp. 15–20, Jan. 1991.

[63] J. Arrillaga, Yonghe Liu, C.S. Crimp, and M. Villablanca, "Harmonic Reduction In Group-Connected Generators-HVDC Convertor," *International Conference on Harmonics in Power Systems*, vol. ICHPS V, pp. 202–207, Sep. 1992.

[64] M. Villablanca and J. Arrillaga, "Single-bridge unit-connected HVDC generation with increased pulse number," *IEEE Transactions on Power Delivery*, vol. 8, Issue: 2, pp. 681–688, Apr. 1993.

[65] M. E. Villablanca and J. Arrillaga, "Pulse multiplication in parallel convertors by multitap control of interphase reactor," *IEE Proceedings B [see also IEE Proceedings-Electric Power Applications]*, vol. 139, Issue: 1, pp. 13–20, Jan 1992.

[66] M. Villablanca, J. del Valle, C. Urrea, and W. Rojas, "36-pulse HVDC transmission for remotely sited generation," *IEEE Transactions on Power Delivery*, vol. 16, No. 4, pp. 462–467, Oct. 2001.

[67] M. Villablanca, M. Arias, and C. Acevedo, "High-pulse series converters for HVDC systems," *IEEE Transactions on Power Delivery*, vol. 16, Issue: 4, pp. 766–774, Oct. 2001.

[68] J. Arrillaga, R. D. Brough, and R. M. Duke, "Naturally commutated thyristor-controlled high-pulse VAR compensator," *IEE Proc. on Gen. Transm. & Distrib.*, vol. 2, pp. 219–224, March 1995.

[69] N.R. Watson, N.D. Smith, and J. Arrillaga, "A high-pulse constant frequency inverter for DC and variable frequency generation sources," *Proceedings of International Conference on Power Electronics and Drive Systems*, vol. 1, PEDS 1995, pp. 358–363, Feb. 1995.

[70] K. Oguchi, G. Maeda, N. Hoshi, and T. Kubata, "Coupling rectifier systems with harmonic cancelling reactors," *IEEE Industry Applications Magazine*, vol. 7, Issue: 4, pp. 53–63, Jul/Aug 2001.

[71] K. Oguchi and T. Yamada, "Novel 18-step diode rectifier circuit with nonisolated phase shifting transformers," *IEE Proceedings-Electric Power Applications*, vol. 144, Issue: 1, pp. 1–5, Jan. 1997.

[72] K. Oguchi, "Three-phase 36-step voltage converter system with an additional single-phase converter for voltage shaping," *Proceedings of IEEE Transmission and Distribution Conference*, pp. 326–331, 15-20 Sep. 1996.

[73] K. Oguchi, T. A. Kawaguchi, Kubota, and N. Hoshi, "A novel six-phase inverter system with sixty-step output voltages for high-power motor drives," *Industry Applications Conference of The IEEE IAS Annual Meeting*, vol. 2, IAS'98, pp. 1408–1415, Oct. 1998.

[74] K. Oguchi, H. Hama, and T. Kubota, "48/72-step voltage double three-level converters coupled with line-side reactors," *Proceedings of the Annual Conference of the IEEE Industrial Electronics Society*, vol. 2, IECON'98, pp. 602–606, Sep. 1998.

[75] Y.H. Liu, N.R. Watson, and J. Arrillaga, "Multi-level voltage sourced conversion by voltage reinjection at six times the fundamental frequency," *IEE Proc. Power Appl.*, vol. 149, No. 3, pp. 201–207, May 2002.

[76] Tatsuhito Nakajima and Shoichi Irokawa, "A Control System for HVDC Transmission by Voltage Sourced Converters," *Power Enginering Society Summer Meeting*, vol. 2, 1999.

[77] N.R. Watson, J. Arrillaga, and Y.H. Liu, "A Four Quadrant Multi-Level Back-TO-Back HVdc Interconnector," *Inernational Conference ON Power System Technology*, vol. 1, PowerCon 2002, pp. 510–514, 13-17 Oct. 2002.

[78] N.R. Watson, J. Arrillaga, and Y.H. Liu, "EMTDC Assessment of a New Type of VSC for Back to Back HVdc Interconnection," *International Conference on Power System Transients*, IPST 2003.

[79] Yong-Hua Song and Allan T. Johns, *Flexible A.C. transmission systems (FACTS)*, London: Institution of Electrical Engineers, 1999.

[80] Narain G. Hingorani and Laszlo Gyugyi, *Understanding FACTS : concepts and technology of flexible AC transmission systems*, New York: IEEE Press, 2000.